INITIAL RELEASE
Final Electrical Specifications

LTC1655L

16-Bit Rail-to-Rail Micropower DAC in SO-8 Package

August 1999

FEATURES

- **16-Bit Monotonicity Over Temperature**
- **3V Single Supply Operation**
- **Deglitched Rail-to-Rail Voltage Output**
- **SO-8 Package**
- $I_{CC(TYP)}$: 600μA
- Internal 1.25V Reference or External Reference Override
- Maximum DNL Error: 1LSB
- Power-On Reset
- 3-Wire Cascadable Serial Interface
- Low Cost
- Pin Compatible Upgrade to 12-Bit LTC1453
- 5V Version Available (LTC1655)

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Smart Remote Transmitters

DESCRIPTION

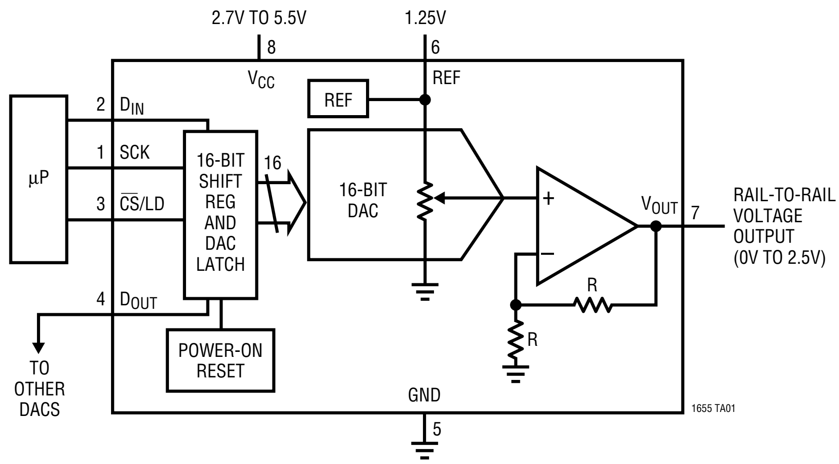
The LTC®1655L is a rail-to-rail voltage output, 16-bit digital-to-analog converter (DAC) in an SO-8 package. It includes an output buffer and a reference. The 3-wire serial interface is compatible with SPI/QSPI and MICROWIRE™ protocols. The SCK input has a Schmitt trigger that allows direct optocoupler interface.

The LTC1655L has an onboard 1.25V reference that can be overdriven to a higher voltage. The output swings from 0V to 2.5V when using the internal reference. The typical power dissipation is 1.6mW on a single 3V supply.

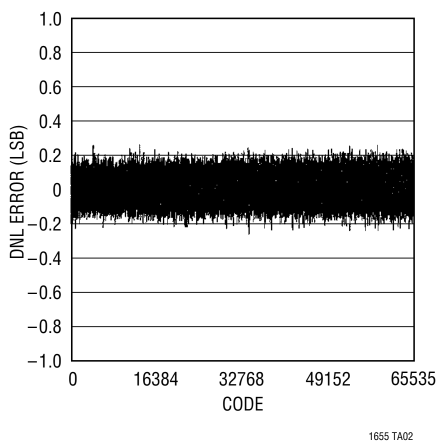
The LTC1655L is pin compatible with Linear Technology's 12-bit V_{OUT} DAC family, allowing an easy upgrade path. It is the only buffered 16-bit DAC in an SO-8 package and it includes an onboard reference for stand alone performance.

BLOCK DIAGRAM

A 16-Bit Rail-to-Rail V_{OUT} DAC



Differential Nonlinearity vs Input Code

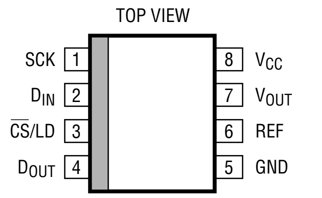


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .... −0.5V to 7.5V
TTL Input Voltage .... −0.5V to 7.5V
V_{OUT}, REF .... −0.5V to V_{CC} + 0.5V
Maximum Junction Temperature .... 125°C
Operating Temperature Range
  LTC1655LC .... 0°C to 70°C
  LTC1655LI .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PDIP   S8 PACKAGE 8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LTC1655LCN8 LTC1655LIN8 LTC1655LCS8 LTC1655LIS8
S8 PART MARKING
1655L 1655LI

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF unloaded.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	16			Bits
	Monotonicity		●	16			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●		±0.3	±1.0	LSB
INL	Integral Nonlinearity	REF = 1.3V (External) (Note 2)	●		±8	±20	LSB
ZSE	Zero-Scale Error		●	0		3.5	mV
V_{OS}	Offset Error	Measured at Code 200	●		±0.5	±3.5	mV
V_{OS}TC	Offset Error Tempco				±5		µV/°C
	Gain Error	REF = 2.2V (External)	●		±5	±16	LSB
	Gain Error Drift				0.5		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	2.7V ≤ V_{CC} ≤ 5.5V (Note 4)	●		600	1200	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		70	140	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		80	150	mA
	Output Impedance to GND	Input Code = 0	●		80	160	Ω
	Output Line Regulation	Input Code = 65535, V_{CC} = 2.7V to 5.5V, with Internal Reference	●			±3	mV/V
AC Performance							
	Voltage Output Slew Rate	(Note 3)	●	±0.3	±0.7		V/µs
	Voltage Output Settling Time	(Note 3) to 0.0015% (16-Bit Settling Time) (Note 3) to 0.012% (13-Bit Settling Time)			20 10		µs µs
	Digital Feedthrough				0.3		nV•s
	Midscale Glitch Impulse	DAC Switched Between 8000 and 7FFF			12		nV•s

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF unloaded.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 3V	●	2			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V	●			0.6	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA, D_{OUT} Only, V_{CC} = 3V	●	V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA, D_{OUT} Only, V_{CC} = 3V	●			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}, V_{CC} = 3V	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)				10	pF
Timing Characteristics							
t_1	D_{IN} Valid to SCK Setup	V_{CC} = 3V	●	60			ns
t_2	D_{IN} Valid to SCK Hold	V_{CC} = 3V	●	0			ns
t_3	SCK High Time	V_{CC} = 3V (Note 6)	●	60			ns
t_4	SCK Low Time	V_{CC} = 3V (Note 6)	●	60			ns
t_5	$\overline{CS}$/LD Pulse Width	V_{CC} = 3V (Note 6)	●	80			ns
t_6	LSB SCK to $\overline{CS}$/LD	V_{CC} = 3V (Note 6)	●	60			ns
t_7	$\overline{CS}$/LD Low to SCK	V_{CC} = 3V (Note 6)	●	30			ns
t_8	D_{OUT} Output Delay	V_{CC} = 3V, C_{LOAD} = 100pF	●	20		300	ns
t_9	SCK Low to $\overline{CS}$/LD Low	V_{CC} = 3V (Note 6)	●	30			ns
Reference Output							
	Reference Output Voltage		●	1.24	1.25	1.26	V
	Reference Input Range	(Notes 5, 6)		1.3		V_{CC}/2	V
	Reference Output Tempco				5		ppm/°C
	Reference Input Resistance	REF Overdriven to 1.3V	●	7	13		kΩ
	Reference Short-Circuit Current		●		40	100	mA
	Reference Output Line Regulation	V_{CC} = 2.7V to 5.5V	●			±1.5	mV/V
	Reference Load Regulation	I_{OUT} = 100µA	●			0.5	mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity is defined from code 128 to code 65535 (full scale). See Applications Information.

Note 3: DAC switched between all 1s and code 400, slew rate is measured from 0.75V to 1.75V.

Note 4: Digital inputs at 0V or V_{CC}.

Note 5: Reference can be overdriven (see Applications Information).

Note 6: Guaranteed by design. Not subject to test.

PIN FUNCTIONS

SCK (Pin 1): The TTL Level Input for the Serial Interface Clock.

D_{IN} (Pin 2): The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock and is loaded MSB first. The LTC1655L requires a 16-bit word.

$\overline{CS}$/LD (Pin 3): The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the SCK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT} (Pin 4): Output of the Shift Register. Becomes valid on the rising edge of the serial clock and swings from GND to V_{CC}.

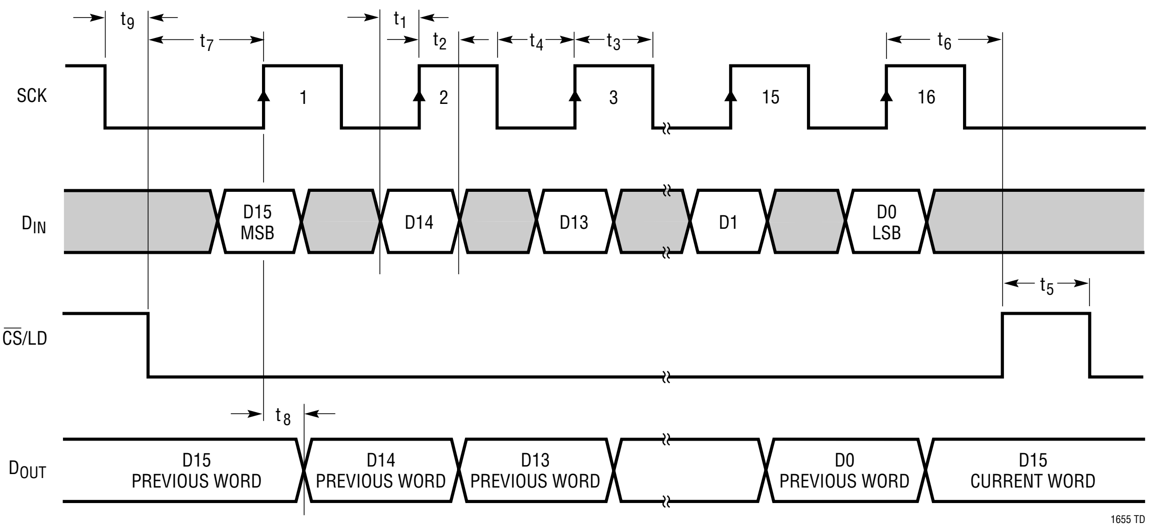
GND (Pin 5): Ground.

REF (Pin 6): Reference. Output of the internal reference is 1.25V. There is a gain of two from this pin to the output. The reference can be overdriven from 1.3V to $V_{CC}/2$. When tied to $V_{CC}/2$, the output will swing from GND to V_{CC}. The output can only swing to within its offset specification of V_{CC} (see Applications Information).

V_{OUT} (Pin 7): Deglitched Rail-to-Rail Voltage Output. V_{OUT} clears to 0V on power-up.

V_{CC} (Pin 8): Positive Supply Input. $2.7V \le V_{CC} \le 5.5V$. Requires a bypass capacitor to ground.

TIMING DIAGRAM



DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

Where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Gain Error (GE): The difference between the full-scale output of a DAC from its ideal full-scale value after offset error has been adjusted.

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code that guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/65535)]/LSB$$

Where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

$$LSB = 2V_{REF}/65536$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The clock is disabled internally when $\overline{CS}$/LD is high. Note: SCK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse. The input word must be 16 bits wide.

The buffered output of the 16-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}.

Multiple LTC1655Ls may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip while the clock and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously. The shift register and DAC register are cleared to all 0s on power-up.

Voltage Output

The LTC1655L rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 400mV of the positive supply voltage or ground. The output stage is equipped with a deglitcher that gives a midscale glitch impulse of 12nV•s. At power-up, the output clears to 0V.

The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full-scale when the REF pin is tied to $V_{CC}/2$. If $V_{REF} = V_{CC}/2$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 1c. No full-scale limiting can occur if V_{REF} is less than (V_{CC} – FSE)/2.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

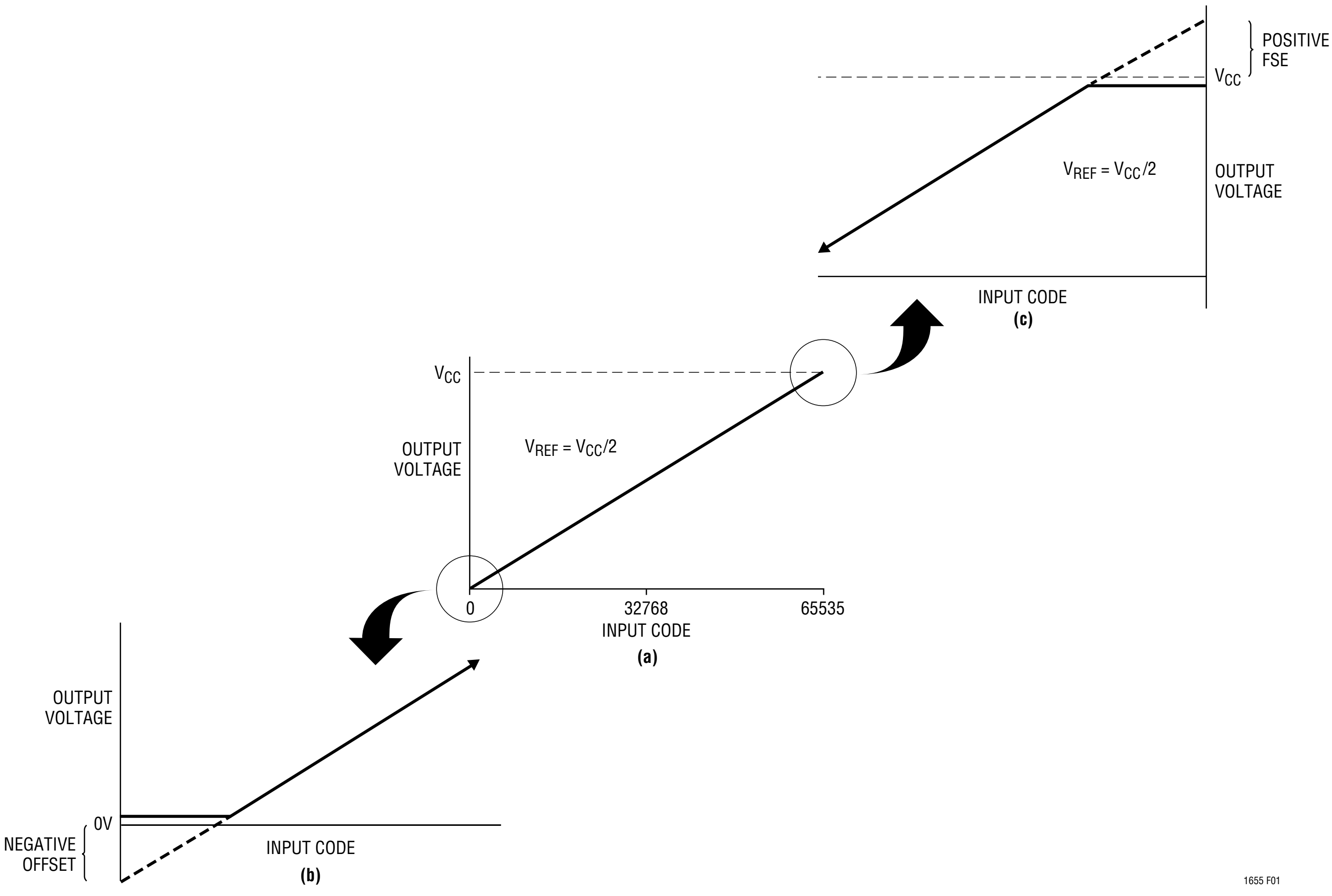
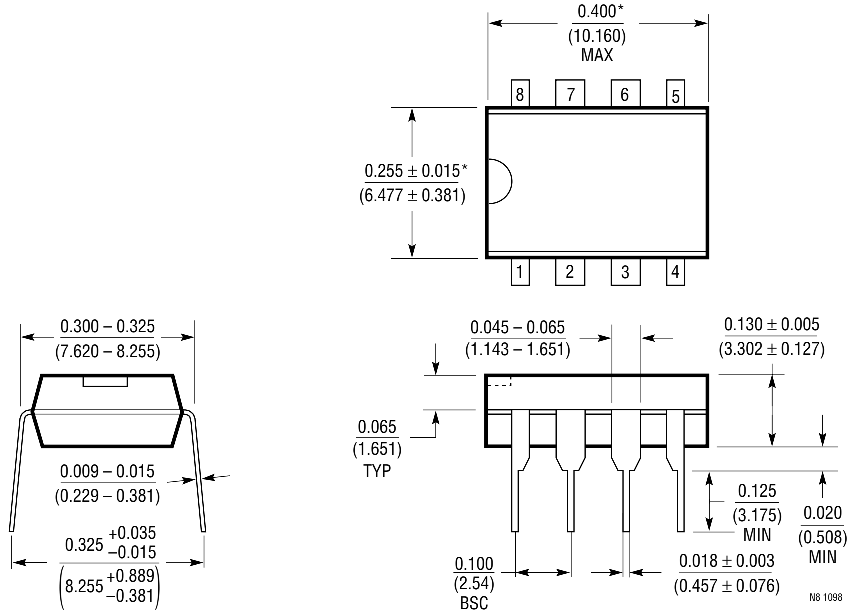


Figure 1. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero-Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full-Scale When $V_{REF} = V_{CC}/2$

PACKAGE DESCRIPTION

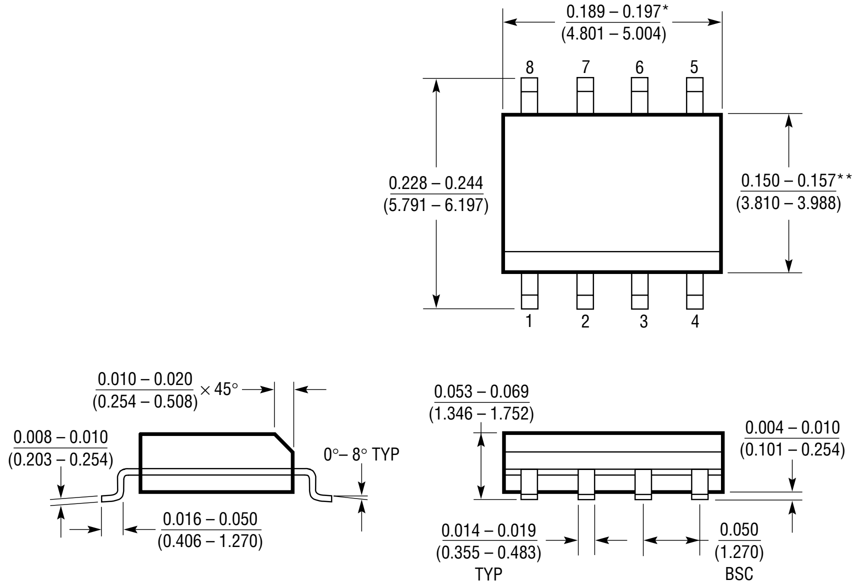
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/ LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC, V_{CC}: 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1450/ LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	5V, Low Power Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/ LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/ LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1650	Single 16-Bit V_{OUT} Industrial DAC in 16-Pin SO, V_{CC} = ±5V DAC, Output Swing ±4.5V	Low Power, Deglitched, 4-Quadrant Mulitplying V_{OUT}
LTC1655	Single Rail-to-Rail 16-Bit V_{OUT} DAC in SO-8 Package	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V, Internal 2048V Reference, Deglitched V_{OUT}
LTC1658	Single Rail-to-Rail 14-Bit V_{OUT} DAC in 8-Pin MSOP, V_{CC} = 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC in MS8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Pin MSOP, V_{CC} = 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC in MS8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}

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