

Constant Frequency Current Mode Step-Down DC/DC Controller in SOT-23

September 1999

FEATURES

- High Efficiency: Up to 94%
- High Output Currents Easily Achieved
- Wide V_{IN} Range: 2.5V to 9.8V
- Constant Frequency 550kHz Operation
- Burst Mode™ Operation at Light Load
- Low Dropout: 100% Duty Cycle
- 0.8V Reference Allows Low Output Voltages
- Current Mode Operation for Excellent Line and Load Transient Response
- Low Quiescent Current: 270 μ A
- Shutdown Mode Draws Only 8 μ A Supply Current
- $\pm 2.5\%$ Reference Accuracy
- Tiny 6-Lead SOT-23 Package

APPLICATIONS

- One or Two Lithium-Ion-Powered Applications
- Cellular Telephones
- Wireless Modems
- Portable Computers
- Distributed 3.3V, 2.5V or 1.8V Power Systems
- Scanners

DESCRIPTION

The LTC[®]1772 is a constant frequency current mode step-down DC/DC controller providing excellent AC and DC load and line regulation. The device incorporates an accurate undervoltage lockout feature that shuts down the LTC1772 when the input voltage falls below 2.0V.

The LTC1772 boasts a $\pm 2.5\%$ output voltage accuracy and consumes only 270 μ A of quiescent current. For applications where efficiency is a prime consideration, the LTC1772 is configured for Burst Mode operation, which enhances efficiency at low output current.

To further maximize the life of a battery source, the external P-channel MOSFET is turned on continuously in dropout (100% duty cycle). In shutdown, the device draws a mere 8 μ A. High constant operating frequency of 550kHz allows the use of a small external inductor.

The LTC1772 is available in a small footprint 6-lead SOT-23.

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 Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

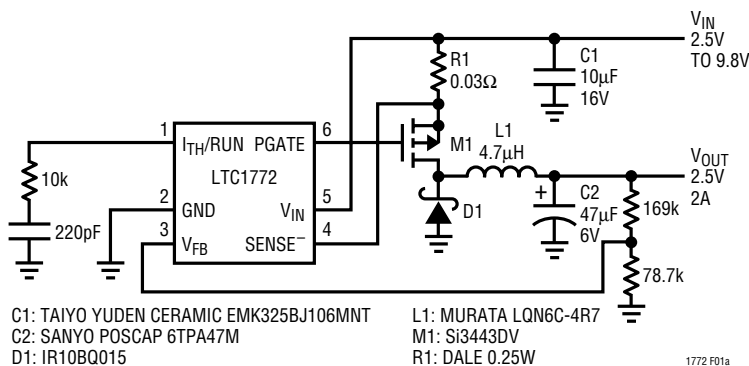
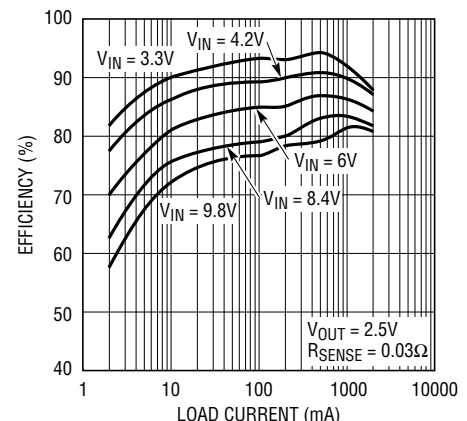


Figure 1. High Efficiency Step-Down Converter

Efficiency vs Load Current



1772 F01b

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN})	–0.3V to 10V
SENSE ⁻ , PGATE Voltages	–0.3V to ($V_{IN} + 0.3V$)
V_{FB} , I_{TH} /RUN Voltages	–0.3V to 2.4V
PGATE Peak Output Current (< 10 μ s)	1A
Storage Ambient Temperature Range	–65°C to 150°C
Operating Temperature Range (Note 2)	0°C to 70°C
Junction Temperature (Note 3)	150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC1772CS6
	S6 PART MARKING
	LTIL

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 4.2\text{V}$ unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS					
Input DC Supply Current	Typicals at $V_{IN} = 4.2\text{V}$ (Note 4)									
						Normal Operation	2.4V \leq $V_{IN} \leq$ 9.8V	270	420	μA
						Sleep Mode	2.4V \leq $V_{IN} \leq$ 9.8V	230	370	μA
						Shutdown	2.4V \leq $V_{IN} \leq$ 9.8V, $V_{ITH}/\text{RUN} = 0\text{V}$	8	22	μA
UVLO	$V_{IN} <$ UVLO Threshold	6	10	μA						
Undervoltage Lockout Threshold	V_{IN} Falling	● 1.6	2.0	2.3	V					
	V_{IN} Rising	1.85	2.3	2.5	V					
Shutdown Threshold (at I_{TH}/RUN)		● 0.2	0.35	0.5	V					
Start-Up Current Source	$V_{ITH}/\text{RUN} = 0\text{V}$	0.25	0.5	0.85	μA					
Regulated Feedback Voltage	(Note 5)	● 0.780	0.800	0.820	V					
Output Voltage Line Regulation	2.4V \leq $V_{IN} \leq$ 9.8V (Note 5)		0.05		mV/V					
Output Voltage Load Regulation	I_{TH}/RUN Sinking 5 μA (Note 5)		2.5		mV/ μA					
	I_{TH}/RUN Sourcing 5 μA (Note 5)		2.5		mV/ μA					
V_{FB} Input Current	(Note 5)		10	50	nA					
Overvoltage Protect Threshold	Measured at V_{FB}	0.820	0.860	0.895	V					
Overvoltage Protect Hysteresis			20		mV					
Oscillator Frequency	$V_{FB} = 0.8\text{V}$	500	550	650	kHz					
	$V_{FB} = 0\text{V}$		120		kHz					
Gate Drive Rise Time	$C_{LOAD} = 3000\text{pF}$		40		ns					
Gate Drive Fall Time	$C_{LOAD} = 3000\text{pF}$		40		ns					
Maximum Current Sense Voltage			120		mV					

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1772 is guaranteed to meet specified performance over the 0°C to 70°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

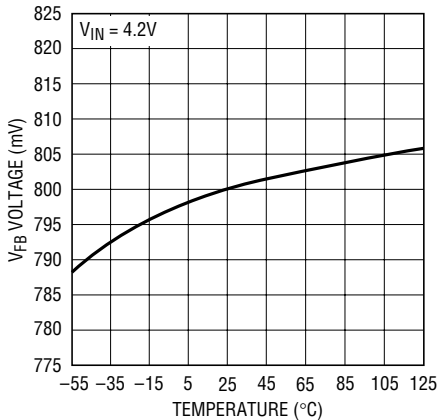
$$T_J = T_A + (P_D \cdot \theta_J^\circ\text{C}/\text{W})$$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC1772 is tested in a feedback loop that serves V_{FB} to the output of the error amplifier.

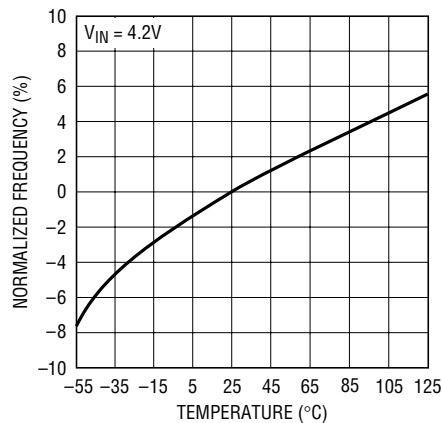
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature



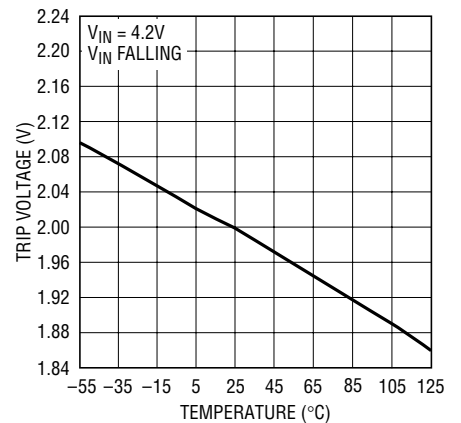
1772 G01

Normalized Oscillator Frequency vs Temperature



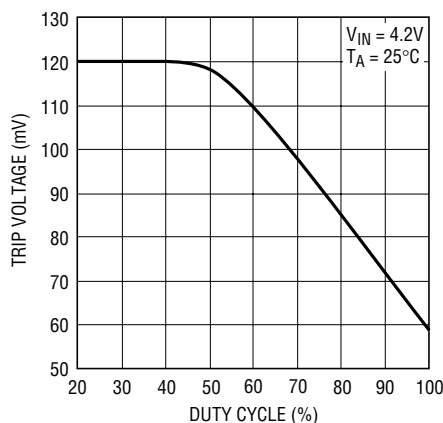
1772 G02

Undervoltage Lockout Trip Voltage vs Temperature



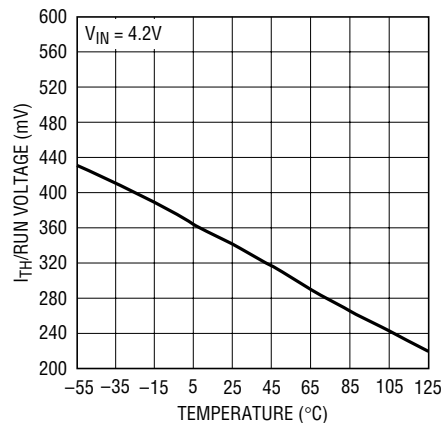
1772 G03

Maximum ($V_{IN} - SENSE^-$) Voltage vs Duty Cycle



1772 G04

Shutdown Threshold vs Temperature



1772 G05

PIN FUNCTIONS

I_{TH}/RUN (Pin 1): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.35V causes the device to be shut down. In shutdown all functions are disabled and the PGATE pin is held high.

GND (Pin 2): Ground Pin.

V_{FB} (Pin 3): Receives the feedback voltage from an external resistive divider across the output.

SENSE⁻ (Pin 4): The Negative Input to the Current Comparator.

V_{IN} (Pin 5): Supply Pin. Must be closely decoupled to GND Pin 2.

PGATE (Pin 6): Gate Drive for the External P-Channel MOSFET. This pin swings from 0V to V_{IN}.

OPERATION (Refer to Functional Diagram)

up, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient overshoots >7.5% by turning off the external P-channel power MOSFET and keeping it off until the fault is removed.

Burst Mode Operation

The LTC1772 enters Burst Mode operation at low load currents. In this mode, the peak current of the inductor is set as if $V_{ITH/RUN} = 1V$ (at low duty cycles) even though the voltage at the $I_{TH/RUN}$ pin is at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the $I_{TH/RUN}$ pin will drop. When the $I_{TH/RUN}$ voltage goes below 0.85V, the sleep signal goes high, turning off the external MOSFET. The sleep signal goes low when the $I_{TH/RUN}$ voltage goes above 0.925V and the LTC1772 resumes normal operation. The next oscillator cycle will turn the external MOSFET on and the switching cycle repeats.

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current during the ON cycle decreases. This reduction means that the external P-channel MOSFET will remain on for more than one oscillator cycle since the inductor current has not ramped up to the threshold set by EAMP. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the LTC1772. When the input supply voltage drops below approximately 2.0V, the P-channel MOSFET and all circuitry is turned off except the undervoltage block, which draws only several microamperes.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator will be reduced to about 120kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage again approaches 0.8V.

Overvoltage Protection

As a further protection, the overvoltage comparator in the LTC1772 will turn the external MOSFET off when the feedback voltage has risen 7.5% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

Slope Compensation and Inductor's Peak Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH}}{10(R_{SENSE})}$$

when the LTC1772 is operating below 40% duty cycle. However, once the duty cycle exceeds 40%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curves in Figure 2.

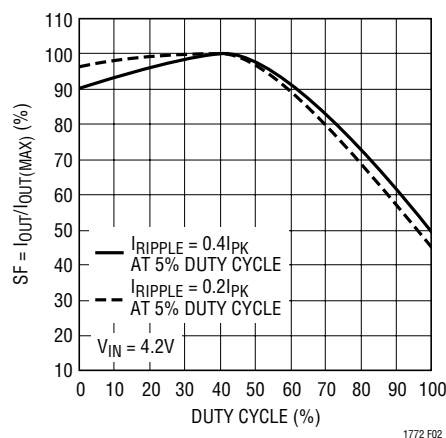


Figure 2. Maximum Output Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC1772 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L1 and R_{SENSE} (= R1). Next, the power MOSFET and the output diode D1 is selected followed by C_{IN} (= C1) and C_{OUT} (= C2).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE} , the threshold of the comparator determines the inductor's peak current. The output current the LTC1772 can provide is given by:

$$I_{OUT} = \frac{0.1}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation section).

A reasonable starting point for setting ripple current is $I_{RIPPLE} = (0.4)(I_{OUT})$. Rearranging the above equation, it becomes:

$$R_{SENSE} = \frac{1}{(12)(I_{OUT})} \text{ for Duty Cycle } < 40\%$$

However, for operation that is above 40% duty cycle, slope compensation effect has to be taken into consideration to select the appropriate value to provide the required amount of current. Using Figure 2, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(12)(I_{OUT})(100)}$$

Inductor Value Calculation

The operating frequency and inductor selection are inter-related in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE} , decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT} . The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f(L)} \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

where f is the operating frequency. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. Remember, the maximum I_{RIPPLE} occurs at the maximum input voltage.

In Burst Mode operation on the LTC1772, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \leq \frac{0.0288}{R_{SENSE}}$$

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f \left(\frac{0.0288}{R_{SENSE}} \right)} \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

$$\text{(Use } V_{IN(MAX)} = V_{IN})$$

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy

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or Kool Mu[®] cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mu. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount that do not increase the height significantly are available.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC1772. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the “on” resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the LTC1772 is designed for operation down to low input voltages, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at $V_{GS} = 2.5V$) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC1772 is less than the absolute maximum V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC1772 in dropout, i.e., 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)_{DC=100\%}} = \frac{P_P}{(I_{OUT(MAX)})^2 (1 + \delta p)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta p)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta p = 0.005/^\circ C$ can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC1772 is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC) I_{OUT}^2 (1 + \delta p)}$$

where DC is the maximum operating duty cycle of the LTC1772.

Output Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(MAX)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

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A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC1772, ceramic capacitors can also be used for C_{IN} . Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \left(ESR + \frac{1}{4fC_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Panasonic SP.

Low Supply Operation

Although the LTC1772 can function down to approximately 2.0V, the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 3 shows the amount of change as the supply is reduced down to 2V. Also shown in Figure 3 is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

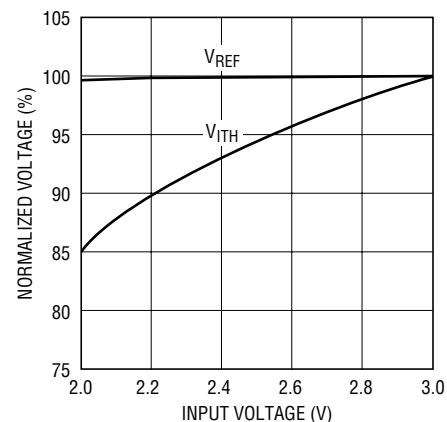


Figure 3. Line Regulation of V_{REF} and V_{ITH}

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Setting Output Voltage

The LTC1772 develops a 0.8V reference voltage between the feedback (Pin 3) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 0.8 \left(1 + \frac{R2}{R1} \right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to LTC1772.

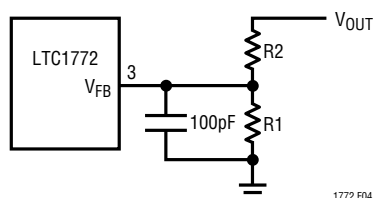


Figure 4. Setting Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (\eta_1 + \eta_2 + \eta_3 + \dots)$$

where η_1 , η_2 , etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1772 circuits: 1) LTC1772 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses and 4) voltage drop of the output diode.

1. The V_{IN} current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver and control currents. V_{IN} current results in a small loss which increases with V_{IN} .
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Qp)$.
3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L but is "chopped" between the P-channel MOSFET in series with R_{SENSE} and the output diode. The MOSFET $R_{DS(ON)}$ plus R_{SENSE} multiplied by duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses.
4. The output diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage times the diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A.
5. Transition losses apply to the external MOSFET and increase at higher operating frequencies and input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = 2(V_{IN})^2 I_{O(MAX)} C_{RSS}(f)$$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

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Foldback Current Limiting

As described in the Output Diode Selection, the worst-case dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously. To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 5. In a hard short ($V_{OUT} = 0V$), the current will be reduced to approximately 50% of the maximum output current.

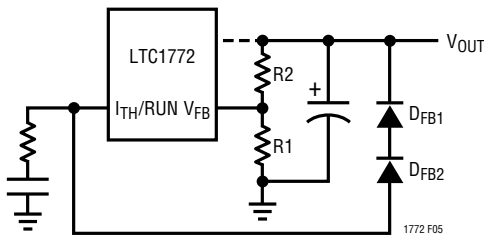


Figure 5. Foldback Current Limiting

Design Example

Assume the LTC1772 is used in a single Lithium-Ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to a minimum of 2.7V. Load current requirement is a maximum of 1.5A but most of the time it will be on standby mode, requiring only 2mA. Efficiency at both low and high load current is important. Output voltage is 2.5V.

$$\text{Maximum Duty Cycle} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_D} = 93\%$$

From Figure 2, SF = 57%.

$$R_{SENSE} = \frac{SF}{(12)(I_{OUT})(100)} = \frac{0.57}{(12)(1.5)} = 0.0317\Omega$$

In the application, a 0.03Ω resistor is used. For the inductor, the required value is:

$$L_{MIN} = \frac{4.2 - 2.5}{550\text{kHz} \left(\frac{0.0288}{0.03} \right)} \left(\frac{2.5 + 0.3}{4.2 + 0.3} \right) = 2.00\mu\text{H}$$

In the application, a $5.6\mu\text{H}$ inductor is used to reduce ripple current.

For the selection of the external MOSFET, the $R_{DS(ON)}$ must be guaranteed at 2.5V since the LTC1772 has to work down to 2.7V. Let's assume that the MOSFET dissipation is to be limited to $P_P = 250\text{mW}$ and its thermal resistance is $50^\circ\text{C}/\text{W}$. Hence the junction temperature at $T_A = 25^\circ\text{C}$ will be 37.5°C and $\delta p = 0.005$ ($37.5 - 25$) = 0.0625. The required $R_{DS(ON)}$ is then given by:

$$R_{DS(ON)} \cong \frac{P_P}{DC(I_{OUT})^2(1 + \delta p)} = 0.11\Omega$$

The P-channel MOSFET requirement can be met by an Si6433DQ.

The requirement for the Schottky diode is the most stringent when $V_{OUT} = 0V$, i.e., short circuit. With a 0.03Ω R_{SENSE} resistor, the short-circuit current through the Schottky is $0.1/0.03 = 3.3A$. An MBR340T3 Schottky diode is chosen. With 3.3A flowing through, the diode is rated with a forward voltage of 0.4V. Therefore, the worst-case power dissipated by the diode is 1.32W. The addition of D_{FB1} and D_{FB2} (Figure 5) will reduce the diode dissipation to approximately 0.66W.

The input capacitor requires an RMS current rating of at least 0.75A at temperature, and C_{OUT} will require an ESR of 0.1Ω for optimum efficiency.

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PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1772. These items are illustrated graphically in the layout diagram in Figure 6. Check the following in your layout:

1. Is the Schottky diode closely connected between ground (Pin 2) and drain of the external MOSFET?
2. Does the (+) plate of C_{IN} connect to the sense resistor as closely as possible? This capacitor provides AC current to the MOSFET.
3. Is the input decoupling capacitor ($0.1\mu\text{F}$) connected closely between V_{IN} (Pin 5) and ground (Pin 2)?
4. Connect the end of R_{SENSE} as close to V_{IN} (Pin 5) as possible. The V_{IN} pin is the SENSE^+ of the current comparator.
5. Is the trace from SENSE^- (Pin 4) to the Sense resistor kept short? Does the trace connect close to R_{SENSE} ?
6. Keep the switching node PGATE away from sensitive small signal nodes.
7. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider $R1$ and $R2$ must be connected between the (+) plate of C_{OUT} and signal ground. The 100pF capacitor should be as close as possible to the LTC1772.

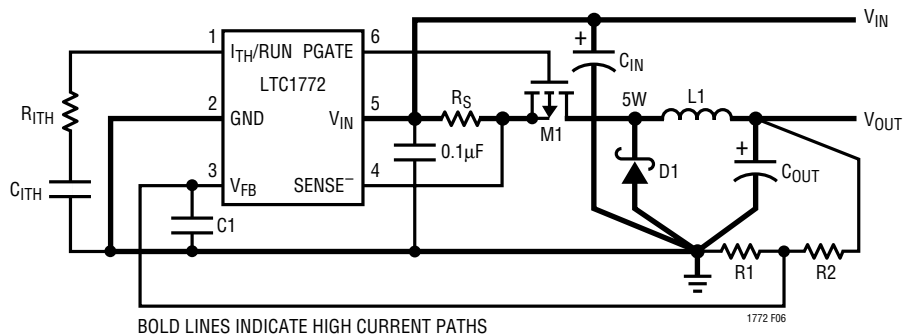
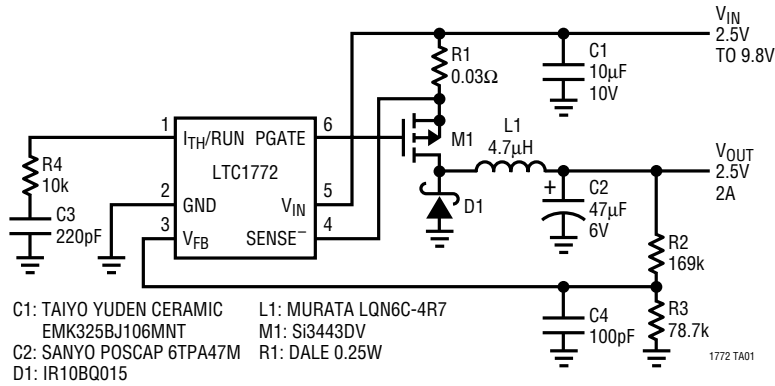


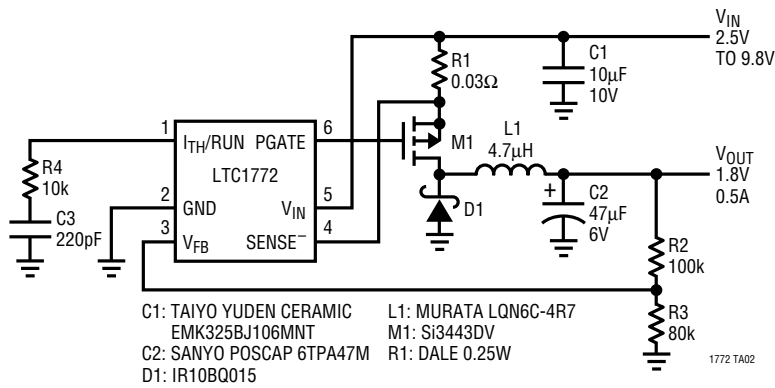
Figure 6. LTC1772 Layout Diagram (See PC Board Layout Checklist)

TYPICAL APPLICATIONS

LTC1772 High Efficiency, High Output Current 2.5V/2A Regulator

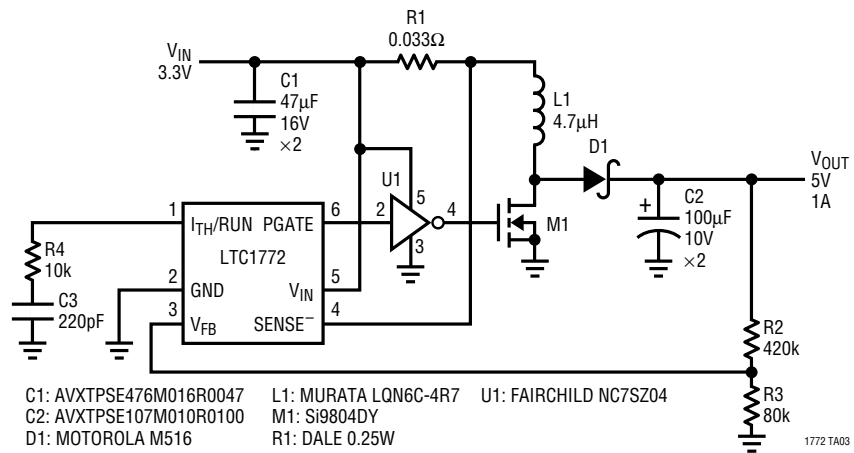


LTC1772 High Efficiency, Small Footprint 1.8V/0.5A Regulator



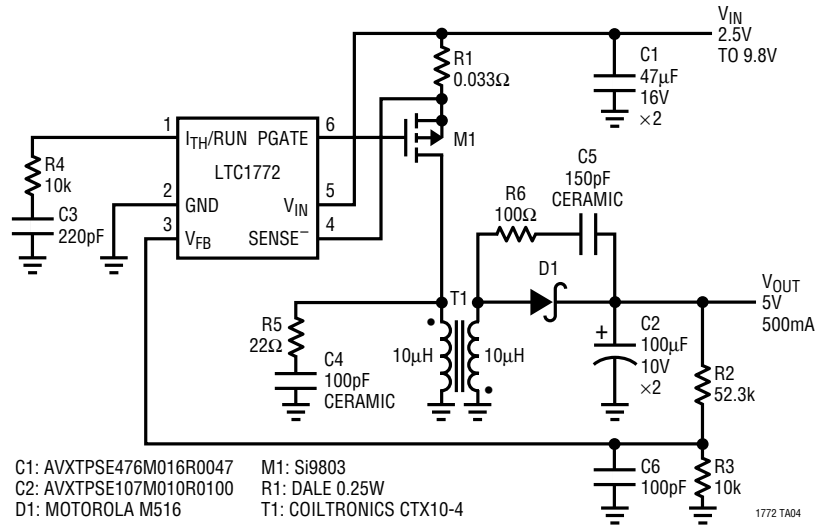
TYPICAL APPLICATIONS

LTC1772 3.3V to 5V/1A Boost Regulator



TYPICAL APPLICATIONS

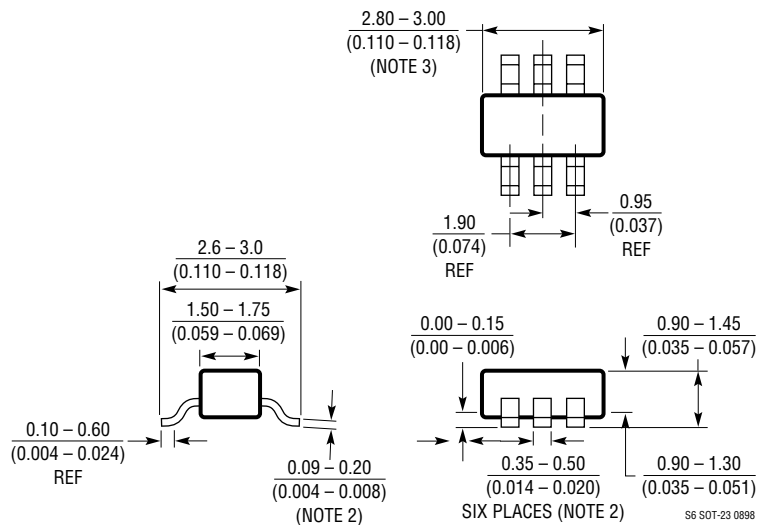
LTC1772 5V/500mA Flyback Regulator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S6 Package 6-Lead Plastic SOT-23 (LTC DWG # 05-08-16XX)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DIMENSIONS ARE INCLUSIVE OF PLATING
 3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 4. MOLD FLASH SHALL NOT EXCEED 0.254mm
 5. PACKAGE EIAJ REFERENCE IS SC-74 (EIAJ)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1147 Series	High Efficiency Step-Down Switching Regulator Controllers	100% Duty Cycle, $3.5V \leq V_{IN} \leq 16V$
LT1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency
LTC1436/LTC1436-PLL	High Efficiency, Low Noise, Synchronous Step-Down Converters	24-Pin Narrow SSOP, $3.5V \leq V_{IN} \leq 36V$
LTC1438/LTC1439	Dual, Low Noise, Synchronous Step-Down Converters	Multiple Output Capability, $3.5V \leq V_{IN} \leq 36V$
LTC1622	Low Input Voltage Current Mode Step-Down DC/DC Controller	V_{IN} 2V to 10V, I_{OUT} Up to 4.5A, Burst Mode Operation Optional, 8-Lead MSOP
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	8-Pin N-Channel Drive, $3.5V \leq V_{IN} \leq 36V$
LTC1625	No R_{SENSE}^{TM} Synchronous Step-Down Regulator	High Efficiency, No Sense Resistor
LTC1626	Low Voltage, High Efficiency Step-Down DC/DC Converter	Monolithic, Constant Off-Time, Low Voltage Range: 2.5V to 6V
LTC1627	Low Voltage, Monolithic Synchronous Step-Down Regulator	Low Supply Voltage Range: 2.65V to 8V, $I_{OUT} = 0.5A$
LTC1735	Single, High Efficiency, Low Noise Synchronous Switching Controller	High Efficiency 5V to 3.3V Conversion at up to 15A

No R_{SENSE} is a trademark of Linear Technology Corporation.