


## FEATURES

- UL Recognized 
- *Guaranteed* Reset Assertion at  $V_{CC} = 1V$
- 1.5mA Maximum Supply Current
- Fast (35ns Max.) On-Board Gating of RAM Chip Enable Signals
- SO8 and SO16 Packaging
- 4.40V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms or Adjustable
- Minimum External Component Count
- 1 $\mu$ A Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature
- Superior Upgrade for MAX690 Family

## APPLICATIONS

- Critical  $\mu$ P Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

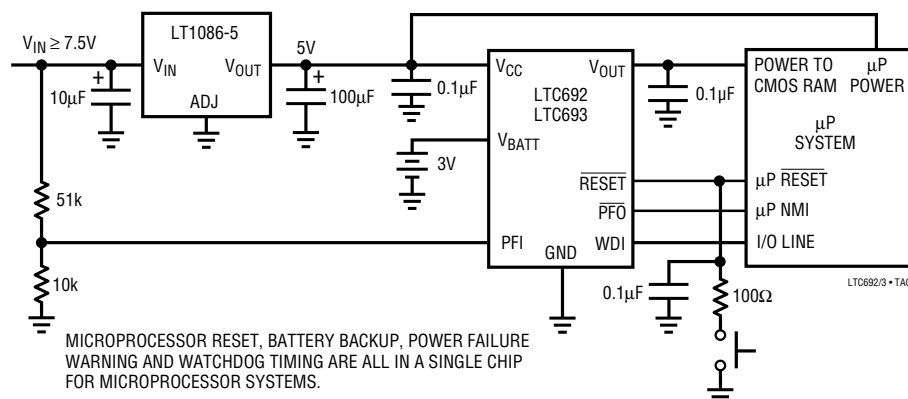
## DESCRIPTION

The LTC692/LTC693 provide complete power supply monitoring and battery control functions for microprocessor reset, battery backup, CMOS RAM write protection, power failure warning and watchdog timing. A precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the reset outputs are forced to active states and the Chip Enable output unconditionally write-protects external memory. In addition, the  $\overline{\text{RESET}}$  output is guaranteed to remain logic low even with  $V_{CC}$  as low as 1V.

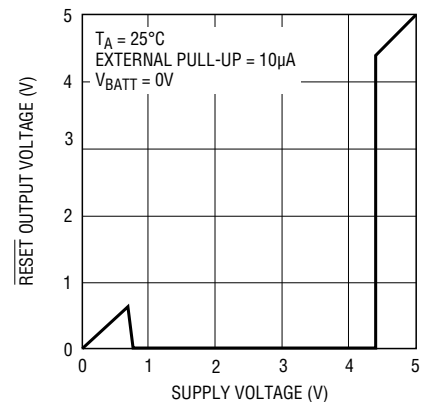
The LTC692/LTC693 power the active CMOS RAMs with a charge pumped NMOS power switch to achieve low drop-out and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, powers the RAMs in standby through an efficient PMOS switch.

For an early warning of impending power failure, the LTC692/LTC693 provide an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to a preset time-out period.

## TYPICAL APPLICATION



$\overline{\text{RESET}}$  Output Voltage vs Supply Voltage



## ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Terminal Voltage	$V_{OUT}$ Output Current ..... Short Circuit Protected
$V_{CC}$ ..... -0.3V to 6.0V	Power Dissipation ..... 500mW
$V_{BATT}$ ..... -0.3V to 6.0V	Operating Temperature Range
All Other Inputs ..... -0.3V to ( $V_{OUT} + 0.3V$ )	LTC692C/LTC693C ..... 0°C to 70°C
Input Current	LTC692I/LTC693I ..... -40°C to 85°C
$V_{CC}$ ..... 200mA	Storage Temperature Range ..... -65°C to 150°C
$V_{BATT}$ ..... 50mA	Lead Temperature (Soldering, 10 sec) ..... 300°C
GND ..... 20mA	

## PACKAGE/ORDER INFORMATION (Note 3)

<p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOL</p> <p><math>T_{JMAX} = 110^{\circ}C</math>, <math>\theta_{JA} = 130^{\circ}C/W</math> (N)  <math>T_{JMAX} = 110^{\circ}C</math>, <math>\theta_{JA} = 180^{\circ}C/W</math> (S)              S8 Package Conditions: PCB Mount on FR4 Material,              Still Air at 25°C, Copper Trace</p>	ORDER PART NUMBER	<p>N PACKAGE 16-LEAD PLASTIC DIP</p> <p>S PACKAGE 16-LEAD PLASTIC SOL</p> <p><math>T_{JMAX} = 110^{\circ}C</math>, <math>\theta_{JA} = 130^{\circ}C/W</math> (N, S)              S16 Package Conditions: PCB Mount on FR4 Material,              Still Air at 25°C, Copper Trace</p>	ORDER PART NUMBER
	LTC692CN8 LTC692IN8 LTC692CS8 LTC692IS8		LTC693CN LTC693IN LTC693CS LTC693IS
	S8 PART MARKING		
	692 692I		

## PRODUCT SELECTION GUIDE

	PINS	RESET THRESHOLD (V)	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSHBUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC692	8	4.40	X	X	X			
LTC693	16	4.40	X	X	X	X		
LTC690	8	4.65	X	X	X			
LTC691	16	4.65	X	X	X	X		
LTC694	8	4.65	X	X	X			
LTC695	16	4.65	X	X	X	X		
LTC699	8	4.65	X					
LTC1232	8	4.37/4.62	X				X	
LTC1235	16	4.65	X	X	X	X	X	X
LTC694-3.3	8	2.90	X	X	X			
LTC695-3.3	16	2.90	X	X	X	X		

## ELECTRICAL CHARACTERISTICS

$V_{CC}$  = Full Operating Range,  $V_{BATT} = 2.8V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITONS	MIN	TYP	MAX	UNITS	
<b>Battery Backup Switching</b>						
Operating Voltage Range $V_{CC}$ $V_{BATT}$		4.50		5.50	V	
		2.00		4.00	V	
$V_{OUT}$ Output Voltage	$I_{OUT} = 1mA$	$V_{CC} - 0.05$ $V_{CC} - 0.10$	$V_{CC} - 0.005$ $V_{CC} - 0.005$		V V	
	$I_{OUT} = 50mA$	$V_{CC} - 0.50$	$V_{CC} - 0.250$		V	
$V_{OUT}$ in Battery Backup Mode	$I_{OUT} = 250\mu A$ , $V_{CC} < V_{BATT}$	$V_{BATT} - 0.1$	$V_{BATT} - 0.02$		V	
Supply Current (Exclude $I_{OUT}$ )	$I_{OUT} \leq 50mA$		0.6	1.5	mA	
			0.6	2.5	mA	
Supply Current in Battery Backup Mode	$V_{CC} = 0V$ , $V_{BATT} = 2.8V$		0.04	1	$\mu A$	
			0.04	5	$\mu A$	
Battery Standby Current (+ = Discharge, - = Charge)	$5.5 > V_{CC} > V_{BATT} + 0.2V$		-0.1	0.02	$\mu A$	
			-1.0	0.10	$\mu A$	
Battery Switchover Threshold $V_{CC} - V_{BATT}$	Power Up		70		mV	
	Power Down		50		mV	
Battery Switchover Hysteresis			20		mV	
BATT ON Output Voltage (Note 4)	$I_{SINK} = 3.2mA$			0.4	V	
BATT ON Output Short-Circuit Current (Note 4)	BATT ON = $V_{OUT}$ Sink Current BATT ON = 0V Source Current		35		mA	
			0.5	1	25	$\mu A$
<b>Reset and Watchdog Timer</b>						
Reset Voltage Threshold		4.25	4.40	4.50	V	
Reset Threshold Hysteresis			40		mV	
Reset Active Time (Note 5)	OSC SEL HIGH, $V_{CC} = 5V$		160	200	240	ms
			140	200	280	ms
Watchdog Time-Out Period, Internal Oscillator	Long Period, $V_{CC} = 5V$		1.2	1.6	2.00	sec
			1.0	1.6	2.25	sec
	Short Period, $V_{CC} = 5V$		80	100	120	ms
			70	100	140	ms
Watchdog Time-Out Period, External Clock (Note 6)	Long Period		4032		Clock	
	Short Period		960		Cycles	
Reset Active Time PSRR			1		ms/V	
Watchdog Time-Out Period PSRR, Internal OSC			1		ms/V	
Minimum WDI Input Pulse Width	$V_{IL} = 0.4V$ , $V_{IH} = 3.5V$	200			ns	
$\overline{RESET}$ Output Voltage At $V_{CC} = 1V$	$I_{SINK} = 10\mu A$ , $V_{CC} = 1V$		4	200	mV	
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage (Note 4)	$I_{SINK} = 1.6mA$ , $V_{CC} = 4.25V$ $I_{SOURCE} = 1\mu A$ , $V_{CC} = 5V$			0.4	V	
			3.5		V	
$\overline{RESET}$ and $\overline{WDO}$ Output Voltage (Note 4)	$I_{SINK} = 1.6mA$ , $V_{CC} = 5V$ $I_{SOURCE} = 1\mu A$ , $V_{CC} = 4.25V$			0.4	V	
			3.5		V	

## ELECTRICAL CHARACTERISTICS

$V_{CC}$  = Full Operating Range,  $V_{BATT} = 2.8V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
RESET, $\overline{RESET}$ , $\overline{WDO}$ , $\overline{LOW LINE}$ Output Short-Circuit Current (Note 4)	Output Source Current Output Sink Current		1	3 25	25	$\mu A$ mA
WDI Input Threshold	Logic Low Logic High		3.5		0.8	V V
WDI Input Current	WDI = $V_{OUT}$ WDI = 0V	● ●	-50	4 -8	50	$\mu A$ $\mu A$
<b>Power Fail Detector</b>						
PFI Input Threshold	$V_{CC} = 5V$	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				$\pm 0.01$	$\pm 25$	nA
$\overline{PFO}$ Output Voltage (Note 4)	$I_{SINK} = 3.2mA$ $I_{SOURCE} = 1\mu A$		3.5		0.4	V V
$\overline{PFO}$ Short Circuit Source Current (Note 4)	PFI = HIGH, $\overline{PFO} = 0V$ PFI = LOW, $\overline{PFO} = V_{OUT}$		1	3 25	25	$\mu A$ mA
PFI Comparator Response Time (falling)	$\Delta V_{IN} = -20mV$ , $V_{OD} = 15mV$			2		$\mu s$
PFI Comparator Response Time (rising) (Note 4)	$\Delta V_{IN} = 20mV$ , $V_{OD} = 15mV$ with $10k\Omega$ Pull-Up			40 8		$\mu s$ $\mu s$
<b>Chip Enable Gating</b>						
$\overline{CE IN}$ Threshold	$V_{IL}$ $V_{IH}$		2.0		0.8	V V
$\overline{CE IN}$ Pullup Current (Note 7)				3		$\mu A$
$\overline{CE OUT}$ Output Voltage	$I_{SINK} = 3.2mA$ $I_{SOURCE} = 3.0mA$ $I_{SOURCE} = 1\mu A$ , $V_{CC} = 0V$		$V_{OUT} - 1.50$ $V_{OUT} - 0.05$		0.4	V V V
$\overline{CE}$ Propagation Delay	$V_{CC} = 5V$ , $C_L = 20pF$	●		20 20	35 45	ns ns
$\overline{CE OUT}$ Output Short Circuit Current	Output Source Current Output Sink Current			30 35		mA mA
<b>Oscillator</b>						
OSC IN Input Current (Note 7)				$\pm 2$		$\mu A$
OSC SEL Input Pull-Up Current (Note 7)				5		$\mu A$
OSC IN Frequency Range	OSC SEL = 0V	●	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, $C_{OSC} = 47pF$			4		kHz

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute maximum ratings are those values beyond which the life of the device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** For military temperature range, consult the factory.

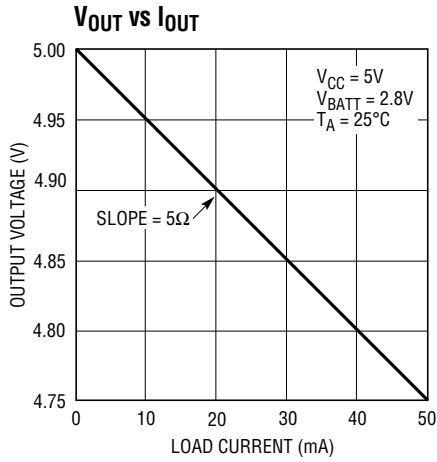
**Note 4:** The output pins of BATT ON,  $\overline{LOW LINE}$ ,  $\overline{PFO}$ ,  $\overline{WDO}$ ,  $\overline{RESET}$  and  $\overline{RESET}$  have weak internal pull-ups of typically  $3\mu A$ . However, external pull-up resistors may be used when higher speed is required.

**Note 5:** The LTC692/LTC693 have minimum reset active times of 140ms (200ms typically). The reset active time of the LTC693 can be adjusted (see Table 2 in Applications Information Section).

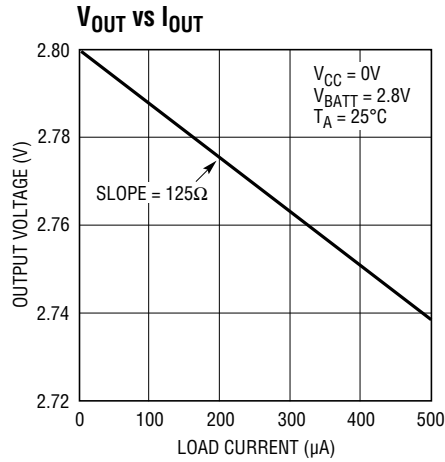
**Note 6:** The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer (See BLOCK DIAGRAM). Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 clocks plus one clock of jitter.

**Note 7:** The input pins of  $\overline{CE IN}$ , OSC IN and OSC SEL have weak internal pull-ups which pull to the supply when the input pins are floating.

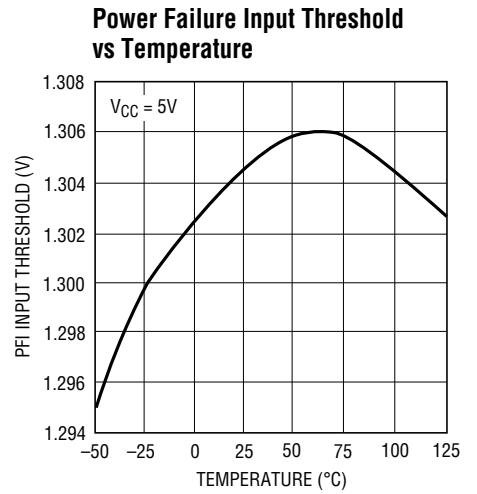
# TYPICAL PERFORMANCE CHARACTERISTICS



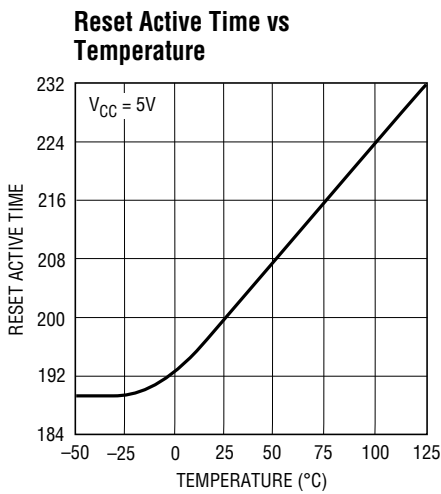
LTC692/3 • TPC01



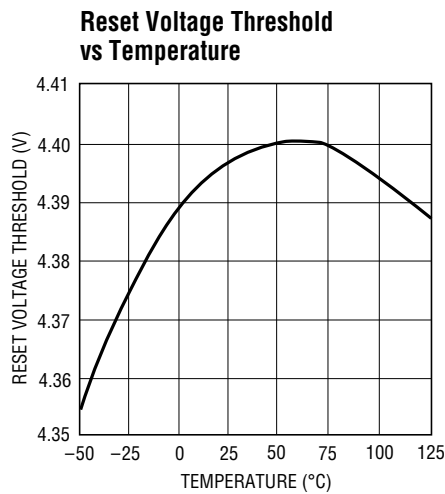
LTC692/3 • TPC02



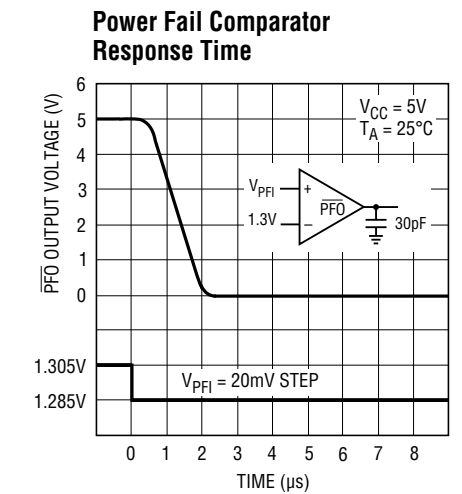
LTC692/3 • TPC03



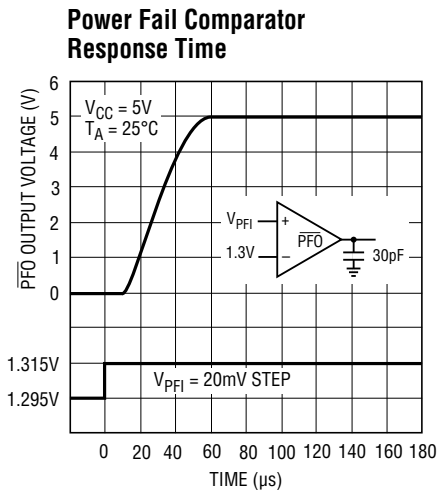
LTC692/3 • TPC04



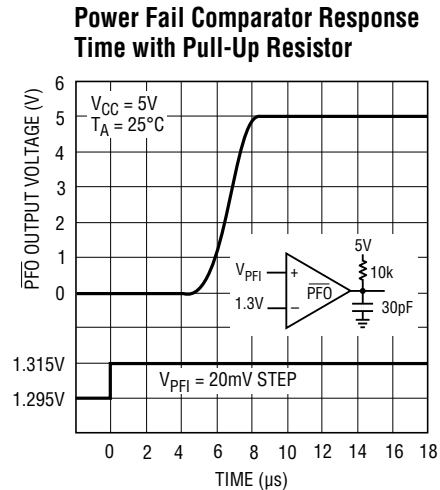
LTC692/3 • TPC05



LTC692/3 • TPC06



LTC692/3 • TPC07



LTC692/3 • TPC08

## PIN FUNCTIONS

**V<sub>CC</sub>**: 5V Supply Input. The V<sub>CC</sub> pin should be bypassed with a 0.1μF capacitor.

**V<sub>OUT</sub>**: Voltage Output for Backed Up Memory. Bypass with a capacitor of 0.1μF or greater. During normal operation, V<sub>OUT</sub> obtains power from V<sub>CC</sub> through an NMOS power switch, M1, which can deliver up to 50mA and has a typical ON resistance of 5Ω. When V<sub>CC</sub> is lower than V<sub>BATT</sub>, V<sub>OUT</sub> is internally switched to V<sub>BATT</sub>. If V<sub>OUT</sub> and V<sub>BATT</sub> are not used, connect V<sub>OUT</sub> to V<sub>CC</sub>.

**V<sub>BATT</sub>**: Backup Battery Input. When V<sub>CC</sub> falls below V<sub>BATT</sub>, auxiliary power connected to V<sub>BATT</sub>, is delivered to V<sub>OUT</sub> through PMOS switch, M2. If backup battery or auxiliary power is not used, V<sub>BATT</sub> should be connected to GND.

**GND**: Ground Pin.

**BATT ON**: Battery On Logic Output from Comparator C2. BATT ON goes low when V<sub>OUT</sub> is internally connected to V<sub>CC</sub>. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V<sub>OUT</sub>. BATT ON goes high when V<sub>OUT</sub> is internally switched to V<sub>BATT</sub>.

**PFI**: Power Failure Input. PFI is the noninverting input to the Power Fail Comparator, C3. The inverting input is internally connected to a 1.3V reference. The Power Failure Output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V<sub>OUT</sub> when C3 is not used.

**PFO**: Power Failure Output from C3. PFO remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V<sub>CC</sub> is lower than V<sub>BATT</sub>, C3 is shut down and PFO is forced low.

**RESET**: Logic Output for μP Reset Control. Whenever V<sub>CC</sub> falls below either the reset voltage threshold (4.40V typically) or V<sub>BATT</sub>, RESET goes active low. After V<sub>CC</sub> returns to 5V, reset pulse generator forces RESET to remain active low for a minimum of 140ms. When the watchdog timer is enabled but not serviced prior to a preset time-out period, reset pulse generator also forces RESET to active low for a minimum of 140ms for every preset

time-out period (see Figure 11). The reset active time is adjustable on the LTC693. An external pushbutton reset can be used in connection with the RESET output. See Pushbutton Reset in the Applications Information section.

**RESET**: RESET is an Active High Logic Output. It is the inverse of RESET.

**LOW LINE**: Logic Output from Comparator C1. LOW LINE indicates a low line condition at the V<sub>CC</sub> input. When V<sub>CC</sub> falls below the reset voltage threshold (4.40V typically), LOW LINE goes low. As soon as V<sub>CC</sub> rises above the reset voltage threshold, LOW LINE returns high (see Figure 1). LOW LINE goes low when V<sub>CC</sub> drops below V<sub>BATT</sub> (see Table 1).

**WDI**: Watchdog Input. WDI is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both RESET and WDO low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 11).

**WDO**: Watchdog Logic Output. When the watchdog input remains either high or low for longer than the watchdog time-out period, WDO goes low. WDO is set high whenever there is a transition on the WDI pin, or LOW LINE goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

**CE IN**: Logic Input to the Chip Enable Gating Circuit. CE IN can be derived from microprocessor's address line and/or decoder output. See Applications Information Section and Figure 5 for additional information.

**CE OUT**: Logic Output on the Chip Enable Gating Circuit. When V<sub>CC</sub> is above the reset voltage threshold, CE OUT is a buffered replica of CE IN. When V<sub>CC</sub> is below the reset voltage threshold CE OUT is forced high (see Figure 5).

**OSC SEL**: Oscillator Selection Input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low allows OSC IN to be driven from an external clock signal or an external capacitor to be connected between OSC IN and GND.



## APPLICATIONS INFORMATION

### Microprocessor Reset

The LTC692/LTC693 use a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on  $V_{CC}$  (see BLOCK DIAGRAM). When  $V_{CC}$  falls below the reset voltage threshold, the  $\overline{\text{RESET}}$  output is forced to active low state. The reset voltage threshold accounts for a 10% variation on  $V_{CC}$ , so the  $\overline{\text{RESET}}$  output becomes active low when  $V_{CC}$  falls below 4.50V (4.40V typical). On power-up, the  $\overline{\text{RESET}}$  signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. The reset active time is adjustable on the LTC693. On power-down, the  $\overline{\text{RESET}}$  signal remains active low even with  $V_{CC}$  as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the  $\overline{\text{RESET}}$  signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at the  $V_{CC}$  pin do not activate the  $\overline{\text{RESET}}$  output. Response time is typically 10 $\mu$ s. To help prevent mistripping due to transient loads,  $V_{CC}$  pin should be bypassed with a 0.1 $\mu$ F capacitor with the leads trimmed as short as possible.

The LTC693 has two additional outputs:  $\overline{\text{RESET}}$  and  $\overline{\text{LOW LINE}}$ .  $\overline{\text{RESET}}$  is an active high output and is the inverse of  $\overline{\text{RESET}}$ .  $\overline{\text{LOW LINE}}$  is the output of the precision voltage comparator C1. When  $V_{CC}$  falls below the reset voltage threshold,  $\overline{\text{LOW LINE}}$  goes low.  $\overline{\text{LOW LINE}}$  returns high as soon as  $V_{CC}$  rises above the reset voltage threshold.

### Battery Switchover

The battery switchover circuit compares  $V_{CC}$  to the  $V_{BATT}$  input, and connects  $V_{OUT}$  to whichever is higher. When  $V_{CC}$  rises to 70mV above  $V_{BATT}$ , the battery switchover comparator, C2, connects  $V_{OUT}$  to  $V_{CC}$  through a charge pumped NMOS power switch, M1. When  $V_{CC}$  falls to 50mV above  $V_{BATT}$ , C2 connects  $V_{OUT}$  to  $V_{BATT}$  through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when  $V_{CC}$  remains nearly equal to  $V_{BATT}$ . The response time of C2 is approximately 20 $\mu$ s.

During normal operation, the LTC692/LTC693 use a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to  $V_{OUT}$  from  $V_{CC}$  and has a typical “on” resistance of 5 $\Omega$ . The  $V_{OUT}$  pin should be bypassed with a capacitor of 0.1 $\mu$ F or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from  $V_{OUT}$ , or a lower dropout ( $V_{CC} - V_{OUT}$  voltage differential) is desired, the LTC693 should be used. This product provides BATT ON output to drive the base of the external PNP transistor (Figure 2). If higher currents are needed with the LTC692, a high current Schottky diode can be connected from the  $V_{CC}$  pin to the  $V_{OUT}$  pin to supply the extra current.

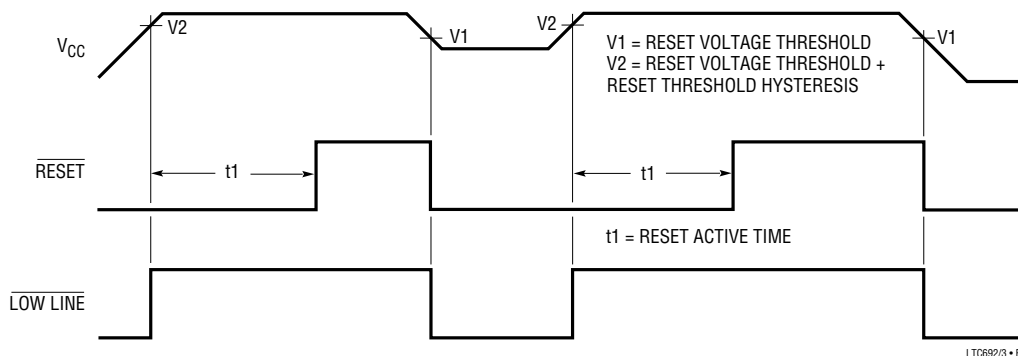


Figure 1. Reset Active Time



## APPLICATIONS INFORMATION

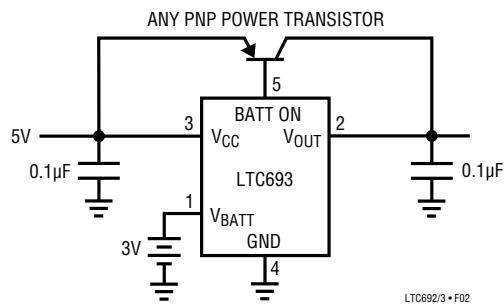


Figure 2. Using BATT ON to Drive External PNP Transistor

The LTC692/LTC693 are protected for safe area operation with a short circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for long periods of time, thermal shutdown turns the power switch off until the device cools down. The threshold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the  $V_{BATT}$  pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. The LTC692/LTC693 use a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by the  $V_{BATT}$  pin is strictly junction leakage.

A 125Ω PMOS switch connects the  $V_{BATT}$  input to  $V_{OUT}$  in battery backup mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. The supply current in battery backup mode is 1µA maximum.

The operating voltage at the  $V_{BATT}$  pin ranges from 2.0V to 4.0V. High value capacitors, such as electrolytic or farad-size double layer capacitors, can be used for short term

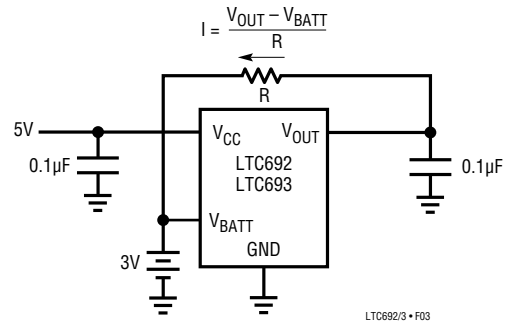


Figure 3. Charging External Battery Through  $V_{OUT}$

memory backup instead of a battery. The charging resistor for the rechargeable batteries should be connected to  $V_{OUT}$  since this eliminates the discharge path that exists when the resistor is connected to  $V_{CC}$  (Figure 3).

### Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur while the battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the  $V_{BATT}$  pin. The oscillation cycle is as follows: When  $V_{BATT}$  reaches within 50mV of  $V_{CC}$ , the LTC692/LTC693 switch to battery backup.  $V_{OUT}$  pulls  $V_{BATT}$  low and the devices go back to normal operation. The leakage current then charges up the  $V_{BATT}$  pin again and the cycle repeats.

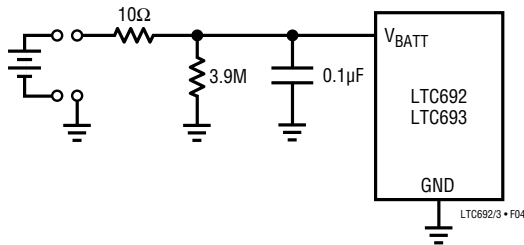
If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, a resistor from  $V_{BATT}$  to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature and the external resistor required to hold  $V_{BATT}$  below  $V_{CC}$  is:

$$R \leq \frac{V_{CC} - 50\text{mV}}{1\mu\text{A}}$$

With  $V_{CC} = 4.25\text{V}$ , a 3.9M resistor will work. With a 3V battery, this resistor will draw only 0.77µA from the battery, which is negligible in most cases.

## APPLICATIONS INFORMATION

If battery connections are made through long wires, a  $10\Omega$  to  $100\Omega$  series resistor and a  $0.1\mu\text{F}$  capacitor are recommended to prevent any overshoot beyond  $V_{\text{CC}}$  due to the lead inductance (Figure 4).



**Figure 4.**  $10\Omega/0.1\mu\text{F}$  combination eliminates inductive overshoot and prevents spurious resets during battery replacement.

Table 1 shows the state of each pin during battery backup. When the battery switchover section is not used, connect  $V_{\text{BATT}}$  to GND and  $V_{\text{OUT}}$  to  $V_{\text{CC}}$ .

### Memory Protection

The LTC693 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when  $V_{\text{CC}}$  is at an invalid level. Two additional pins,  $\overline{\text{CE IN}}$  and  $\overline{\text{CE OUT}}$ , control the Chip Enable or Write inputs of CMOS RAM. When  $V_{\text{CC}}$  is 5V,  $\overline{\text{CE OUT}}$  follows  $\overline{\text{CE IN}}$  with a typical propagation delay of 20ns. When  $V_{\text{CC}}$  falls below the reset voltage threshold or  $V_{\text{BATT}}$ ,  $\overline{\text{CE OUT}}$  is forced high, independent of  $\overline{\text{CE IN}}$ .  $\overline{\text{CE OUT}}$  is an

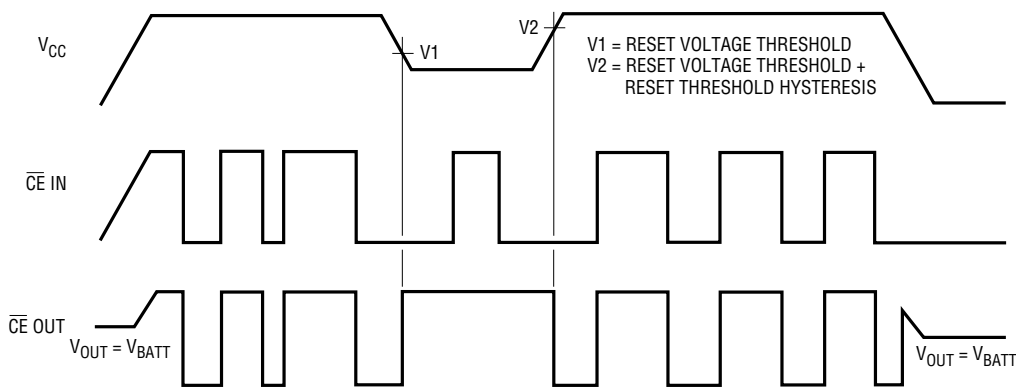
alternative signal to drive the  $\overline{\text{CE}}$ ,  $\overline{\text{CS}}$ , or  $\overline{\text{Write}}$  input of battery backed up CMOS RAM.  $\overline{\text{CE OUT}}$  can also be used to drive the Store or Write input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 5 shows the timing diagram of  $\overline{\text{CE IN}}$  and  $\overline{\text{CE OUT}}$ .

$\overline{\text{CE IN}}$  can be derived from the microprocessor's address decoder output. Figure 6 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC692 by using RESET as shown in Figure 7.

**Table 1.** Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
$V_{\text{CC}}$	C2 monitors $V_{\text{CC}}$ for active switchover.
$V_{\text{OUT}}$	$V_{\text{OUT}}$ is connected to $V_{\text{BATT}}$ through an internal PMOS switch.
$V_{\text{BATT}}$	The supply current is $1\mu\text{A}$ maximum.
BATT ON	Logic high. The open-circuit output voltage is equal to $V_{\text{OUT}}$ .
$\overline{\text{PFI}}$	Power Failure Input is ignored.
$\overline{\text{PFO}}$	Logic low
$\overline{\text{RESET}}$	Logic low
RESET	Logic high. The open-circuit output voltage is equal to $V_{\text{OUT}}$ .
$\overline{\text{LOW LINE}}$	Logic low
WDI	Watchdog Input is ignored.
$\overline{\text{WDO}}$	Logic high. The open-circuit output voltage is equal to $V_{\text{OUT}}$ .
$\overline{\text{CE IN}}$	Chip Enable Input is ignored.
$\overline{\text{CE OUT}}$	Logic high. The open-circuit output voltage is equal to $V_{\text{OUT}}$ .
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.



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**Figure 5.** Timing Diagram for  $\overline{\text{CE IN}}$  and  $\overline{\text{CE OUT}}$

## APPLICATIONS INFORMATION

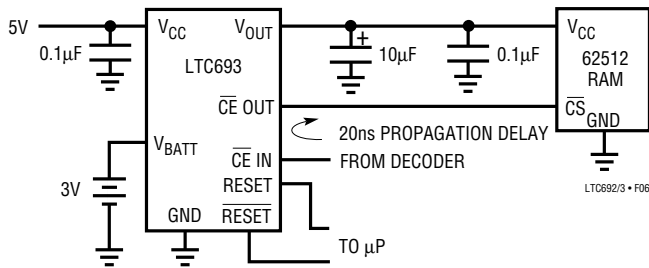


Figure 6. A Typical Nonvolatile CMOS RAM Application

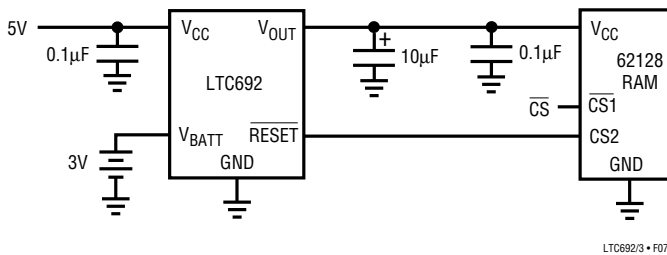
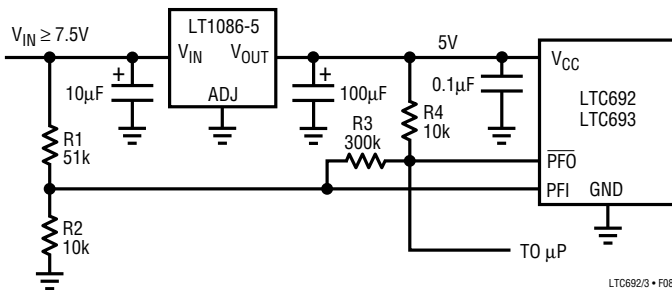
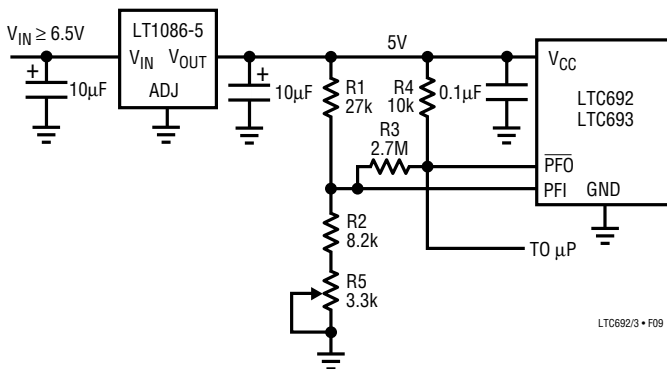


Figure 7. Write Protect for RAM with the LTC692

Figure 8. Monitoring *Unregulated* DC Supply with the LTC692/LTC693 Power Fail ComparatorFigure 9. Monitoring *Regulated* DC Supply with the LTC692/LTC693 Power Fail Comparator

## Power Fail Warning

The LTC692/LTC693 generate a Power Failure Output (PFO) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. PFO goes low when the voltage at the PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage at the PFI pin falls below 1.3V, several milliseconds before the 5V supply falls below the maximum reset voltage threshold of 4.50V. PFO is normally used to interrupt the microprocessor to execute shutdown procedure between PFO and RESET or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the PFO output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When PFO output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V \left( 1 + \frac{R1}{R2} + \frac{R1}{R3} \right)$$

When PFO output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V \left( 1 + \frac{R1}{R2} - \frac{(5V - 1.3V)R1}{1.3V(R3 + R4)} \right)$$

$$\text{Assuming } R4 \ll R3, V_{\text{HYSTERESIS}} = 5V \frac{R1}{R3}$$

**Example 1:** The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the rate of decay of the supply input  $V_{IN}$  is 100mV/ms and the total time to execute a shutdown procedure is 8ms. Also, the noise of  $V_{IN}$  is 200mV. With these assumptions in mind, we can reasonably set  $V_L = 7.25V$  which is 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage of LT1086-5 (4.5V + 1.5V) and  $V_{\text{HYSTERESIS}} = 850mV$ .



## APPLICATIONS INFORMATION

The LTC693 provides an additional output (Watchdog Output,  $\overline{WDO}$ ) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin.  $\overline{WDO}$  is also set high when  $V_{CC}$  falls below the reset voltage threshold or  $V_{BATT}$ .

The LTC693 has two additional pins OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 12.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and

GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 140ms minimum. OSC IN selects between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

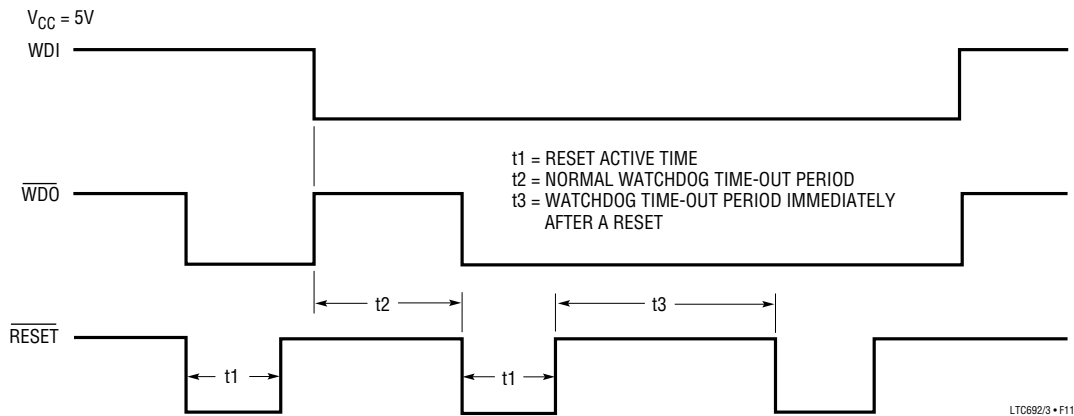


Figure 11. Watchdog Time-out Period and Reset Active Time

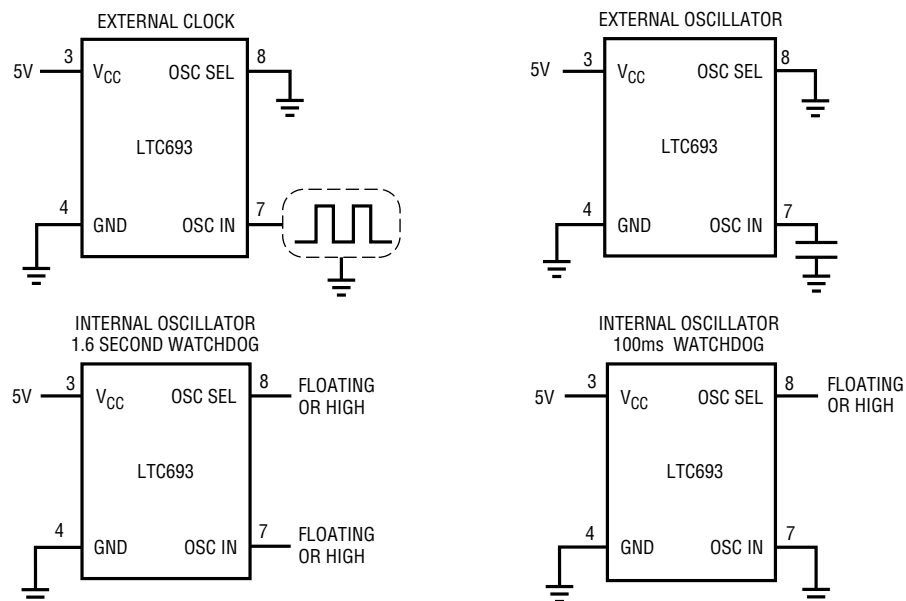


Figure 12. Oscillator Configurations

## APPLICATIONS INFORMATION

Table 2. LTC693 Reset Active Time and Watchdog Time-Out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC693
Low	External Clock Input	1024 clks	4096 clks	2048 clks
Low	External Capacitor*	$\frac{400\text{ms}}{47\text{pF}} \times C$	$\frac{1.6\text{ sec}}{47\text{pF}} \times C$	$\frac{800\text{ms}}{47\text{pF}} \times C$
Floating or High Floating or High	Low Floating or High	100ms 1.6 sec	1.6 sec 1.6 sec	200ms 200ms

\*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is  $F_{\text{OSC}} (\text{Hz}) = \frac{184,000}{C(\text{pF})}$

### Pushbutton Reset

The LTC692/LTC693 do not provide a logic input for direct connection to a pushbutton. However, a pushbutton in series with a 100Ω resistor connected to the RESET output pin (Figure 13) provides an alternative for manual reset. Connecting a 0.1μF capacitor to the RESET pin debounces the pushbutton input.

The 100Ω resistor in series with the pushbutton is required to prevent the ringing, due to the capacitance and lead inductance, from pulling the RESET pins of the MPU and LTC692/LT693 below ground.

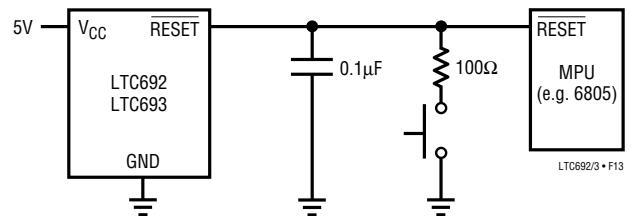
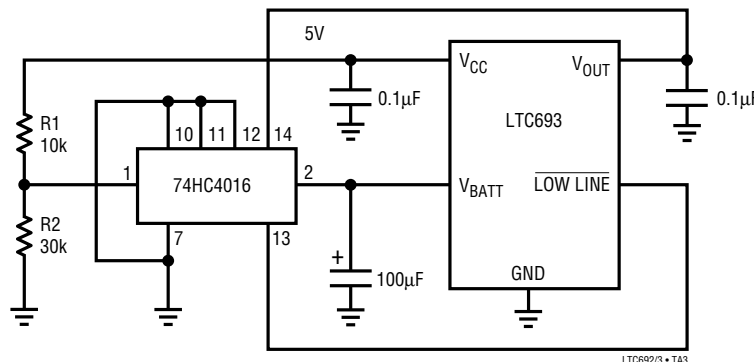


Figure 13. The External Pushbutton Reset

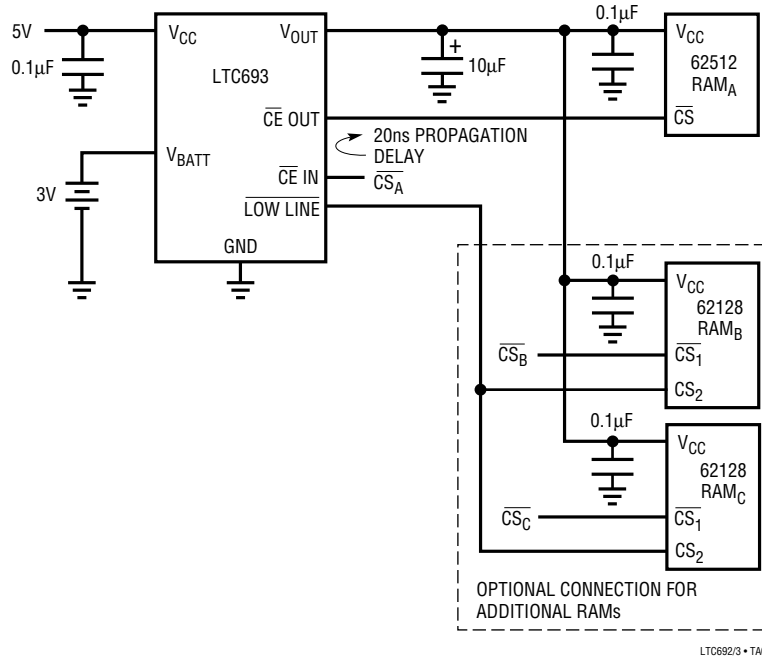
## TYPICAL APPLICATIONS

### Capacitor Backup with 74HC4016 Switch



# TYPICAL APPLICATIONS

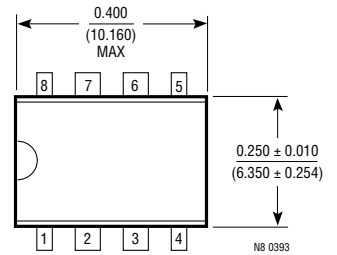
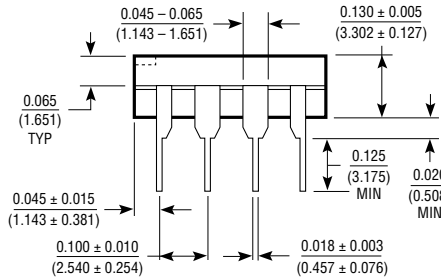
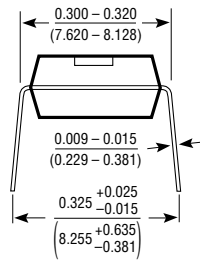
Write Protect for Additional RAMs



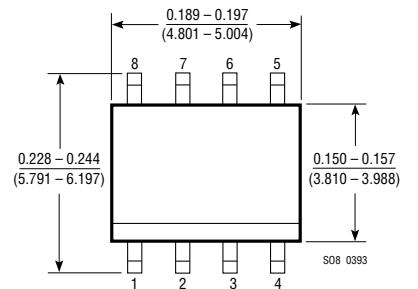
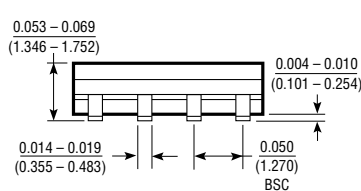
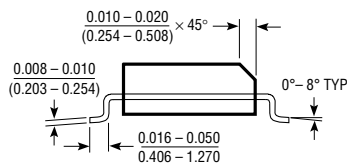
LTC692/3 • TA04

## PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**  
8-Lead Plastic DIP

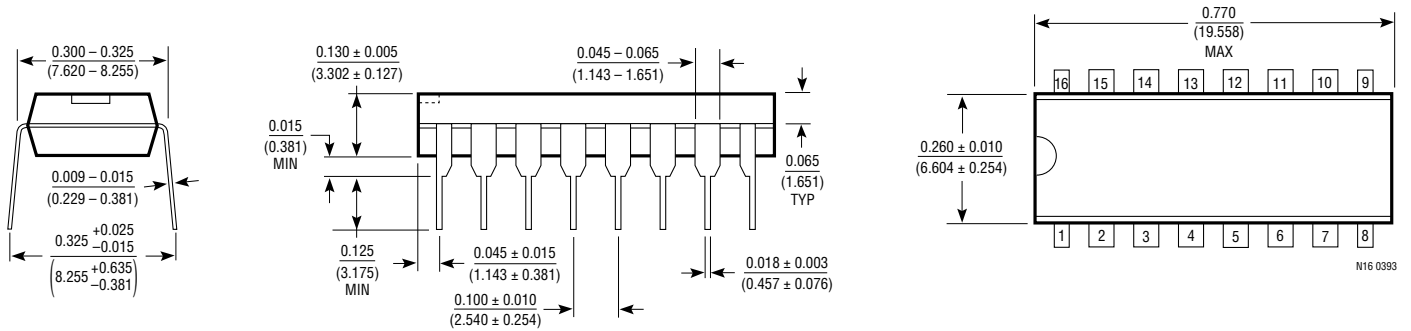


**S8 Package**  
8-Lead Plastic SOIC

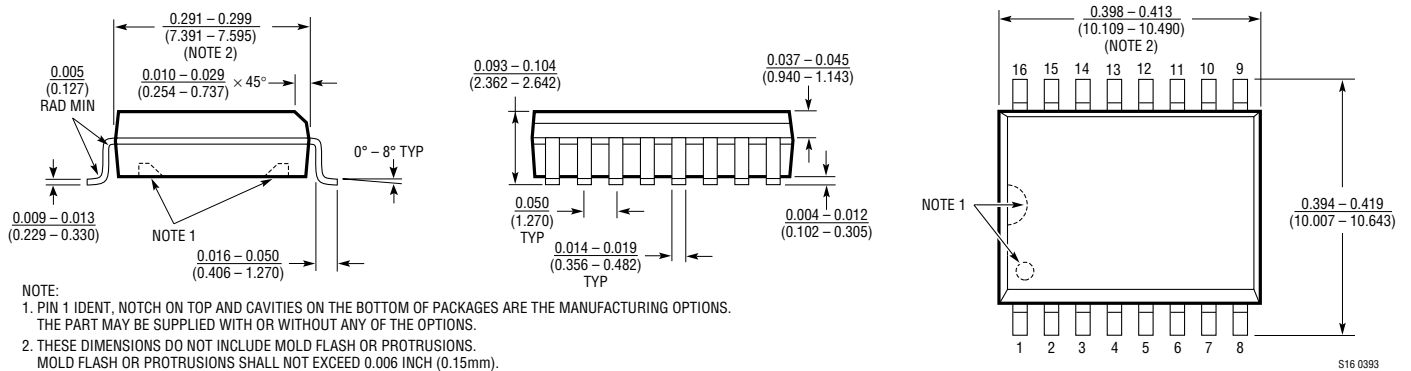


**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**N Package  
16-Lead Plastic DIP**



**S Package  
16-Lead SOL**



- NOTE:
- PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
  - THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).