LINEAR SYSTEMS

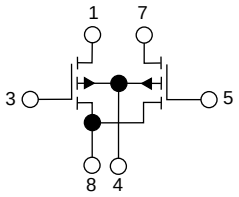
Linear Integrated Systems

3N165, 3N166

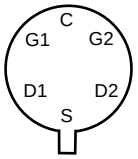
MONOLITHIC DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

FEATURES
VERY HIGH INPUT IMPEDANCE
HIGH GATE BREAKDOWN
ULTRA LOW LEAKAGE
LOW CAPACITANCE

ABSOLUTE MAXIMUM RATINGS (NOTE 1) (T_A= 25°C unless otherwise noted)	
Drain-Source or Drain-Gate Voltage **(NOTE 2)**	
3N165	40 V
3N166	30 V
Transient G-S Voltage **(NOTE 3)**	±125 V
Gate-Gate Voltage	±80 V
Drain Current **(NOTE 2)**	50 mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation (One Side)	300 mW
Total Derating above 25°C	4.2 mW/°C



Device Schematic



TO-99
Bottom View

ELECTRICAL CHARACTERISTICS (T_A=25°C and V_{BS}=0 unless otherwise specified)

SYMBOL	CHARACTERISTICS	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS		
I_{GSSR}	Gate Reverse Leakage Current	--	10	pA	V_{GS}= 40 V		
I_{GSSF}	Gate Forward Leakage Current	--	-10		V_{GS}= -40 V		
		--	-25		T_A=+125°C		
I_{DSS}	Drain to Source Leakage Current	--	-200		V_{DS}= -20 V		
I_{SDS}	Source to Drain Leakage Current	--	-400		V_{SD}= -20 V	V_{DB}= 0	
$I_{D(on)}$	On Drain Current	-5	-30	mA	V_{DS}= -15 V	V_{GS}= -10 V	
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	V_{DS}= -15 V	I_D= -10 µA	
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	V_{DS}= V_{GS}	I_D= -10 µA	
$r_{DS(on)}$	Drain Source ON Resistance	--	300	ohms	V_{GS}= -20 V	I_D= -100 µA	
g_{fs}	Forward Transconductance	1500	3000	µs	V_{DS}= -15V	I_D= -10mA	f=1kHz
g_{os}	Output Admittance	--	300	µs			
C_{iss}	Input Capacitance	--	3.0	pF			
C_{rss}	Reverse Transfer Capacitance	--	0.7		V_{DS}= -15V	I_D= -10mA	f=1MHz
C_{oss}	Output Capacitance	--	3.0		**(NOTE 4)**		
$R_E(Y_{fs})$	Common Source Forward Transconductance	1200	--	µs	V_{DS}= -15V **(NOTE 4)**	I_D= -10mA	f=100MHz

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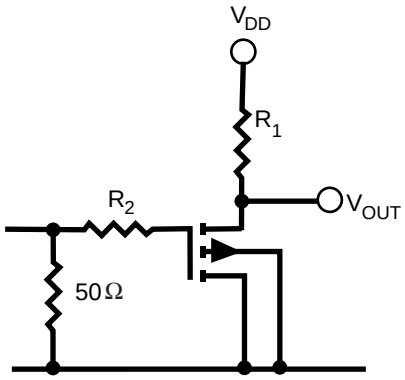
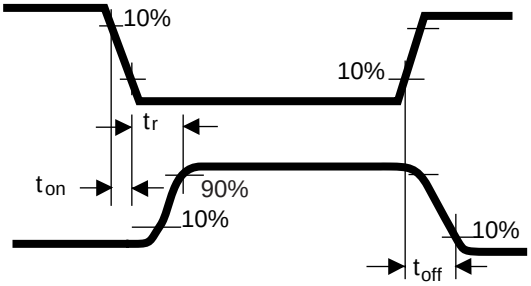
MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTICS	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS}= -15 V I_D= -500 µA f=1kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS}= -15 V I_D= -500 µA
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/°C	V_{DS}= -15 V I_A= -500 µA T_A= -55°C to = +25°C



TYPICAL SWITCHING WAVEFORM



INPUT PULSE

Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE

T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Switching Times Test Circuit

NOTES:

1. MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures: To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanant damage to the devices.
2. Per transistor.
3. Devices must mot be tested at ±125V more than once, nor for longer than 300ms.
4. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.