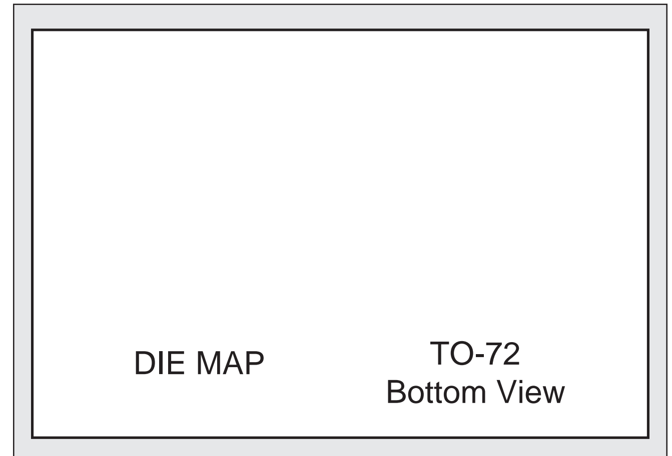
LINEAR SYSTEMS

Linear Integrated Systems

3N170, 3N171

N-CHANNEL ENHANCEMENT MODE
MOSFET

FEATURES	
VERY HIGH INPUT IMPEDANCE	
LOW SWITCHING VOLTAGES	
LOW DRAIN-SOURCE RESISTANCE	
LOW REVERSE TRANSFER CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS (NOTE 1) (T_A= 25°C unless otherwise noted)	
Drain-Gate Voltage	±35V
Drain-Source Voltage	25V
Gate-Gate Voltage	±35V
Drain Current	30mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +125°C
Power Dissipation	300 mW



ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise specified)

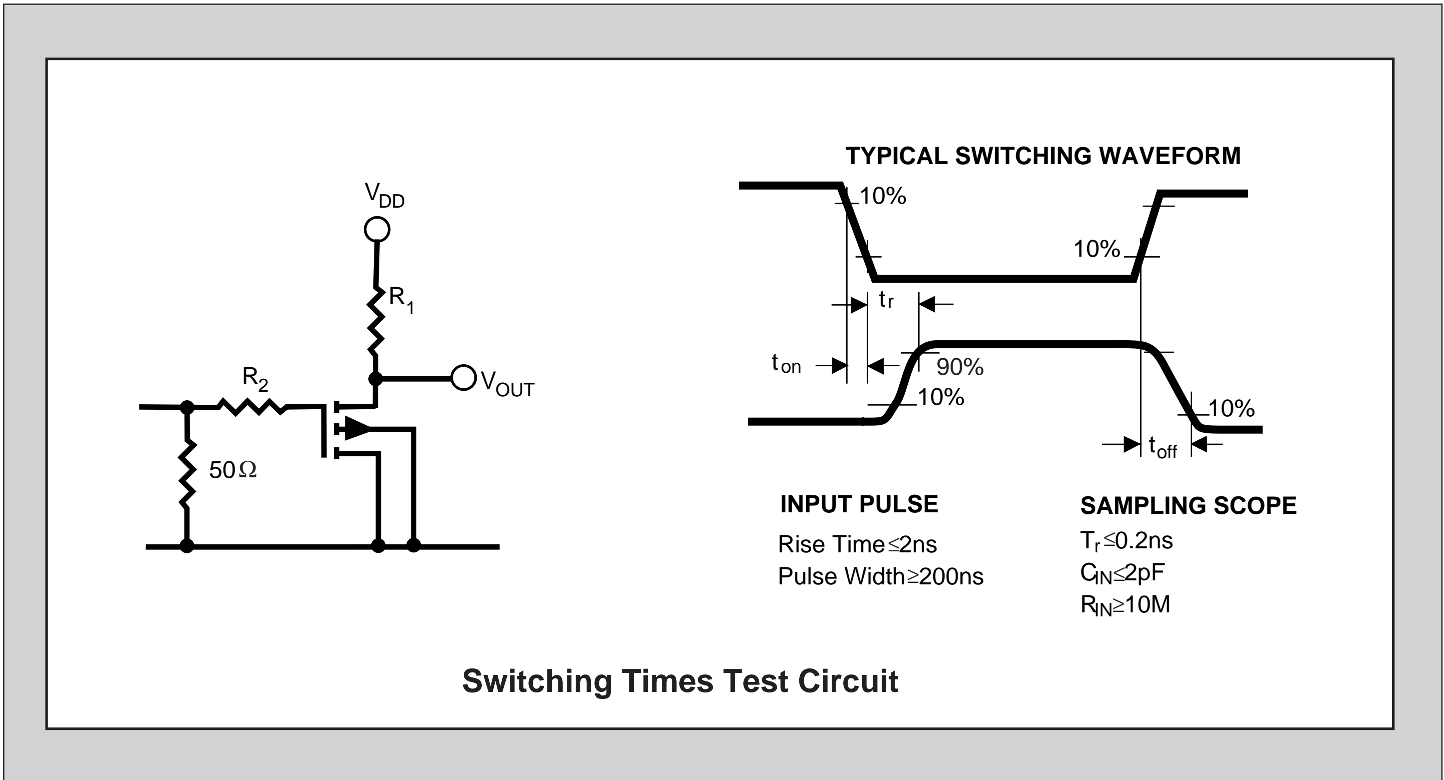
SYMBOL	CHARACTERISTICS		LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS		
I_{GSS}	Gate-Body Leakage Current		--	10	pA	V_{GS}= -35 V	V_{DS}= 0	
BV_{DSS}	Drain-Source Breakdown Voltage		25	--	V	V_{GS}= 0	I_D= 10 mA	
$V_{GS(th)}$	Threshold Voltage	3N170	1.0	2.0				
		3N171	1.5	3.0		V_{DS}= -10V	I_D= 10 µA	
I_{DSS}	Zero Gate Voltage Drain Current		--	10	nA	V_{DS}= -10 V	V_{GS}= 0	
$r_{DS(on)}$	Drain-Source ON Resistance		--	200	ohms	V_{GS}= -10 V	I_D= 0	f=1KHz
$I_{D(on)}$	ON Drain Current		10	--	mA	V_{GS}= -10 V	V_{DS}= -10 V	
$V_{DS(on)}$	Drain-Source ON Voltage		--	2.0	V	V_{GS}= -10 V	I_D= 10 mA	
$\|Y_{fs}\|$	Forward Transfer Admittance		1000	--	µs	V_{DS}= -10V	I_D= 2.0mA	f=1KHz
C_{rss}	Reverse Transfer Capacitance		--	1.3		V_{GS}= 0	V_{DS}= 0	f=1MHz
C_{iss}	Input Capacitance		--	5.0	pF	V_{GS}= 0	V_{DS}= -10V	f=1MHz
$C_{d(sub)}$	Drain Substrate Capacitance		--	5.0		$V_{D(SUB)}$=-10V	f=1MHz	
$td_{(on)}$	Turn-On Delay Time		--	3.0		V_{DD}= -10V	$I_{D(on)}$= 10mA	
t_r	Rise Time		--	10		$V_{GS(on)}$= -10V	$V_{GS(off)}$= of=1KHz	
$td_{(off)}$	Turn-Off Delay Time		--	3.0	ns	R_G= 50Ω		
t_f	Fall Time		--	15				

NOTES: 1. These ratings are limiting values above which the serviceability of the semiconductor may be impaired.

Linear Integrated Systems 4042 Clipper Ct., Fremont, CA 94538 TEL: (510) 490-9160 • FAX: (510) 353-0261

MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTICS	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS}= -15 V I_D= -500 µA f=1kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS}= -15 V I_D= -500 µA
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/°C	V_{DS}= -15 V I_A= -500 µA T_A= -55°C to = +25°C



Switching Times Test Circuit

NOTES:

1. MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
   To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanant damage to the devices.
2. Per transistor.
3. Devices must mot be tested at ±125V more than once, nor for longer than 300ms.
4. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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