DEVICES INCORPORATED

LF9501
Programmable Line Buffer

FEATURES

- 50 MHz Maximum Operating Frequency
- Programmable Buffer Length from 2 to 1281 Clock Cycles
- 10-bit Data Inputs and Outputs
- Data Delay and Data Recirculation Modes
- Supports Positive or Negative Edge System Clocks
- Expandable Data Word Width or Buffer Length
- Replaces Harris HSP9501
- 44-pin PLCC, J-Lead

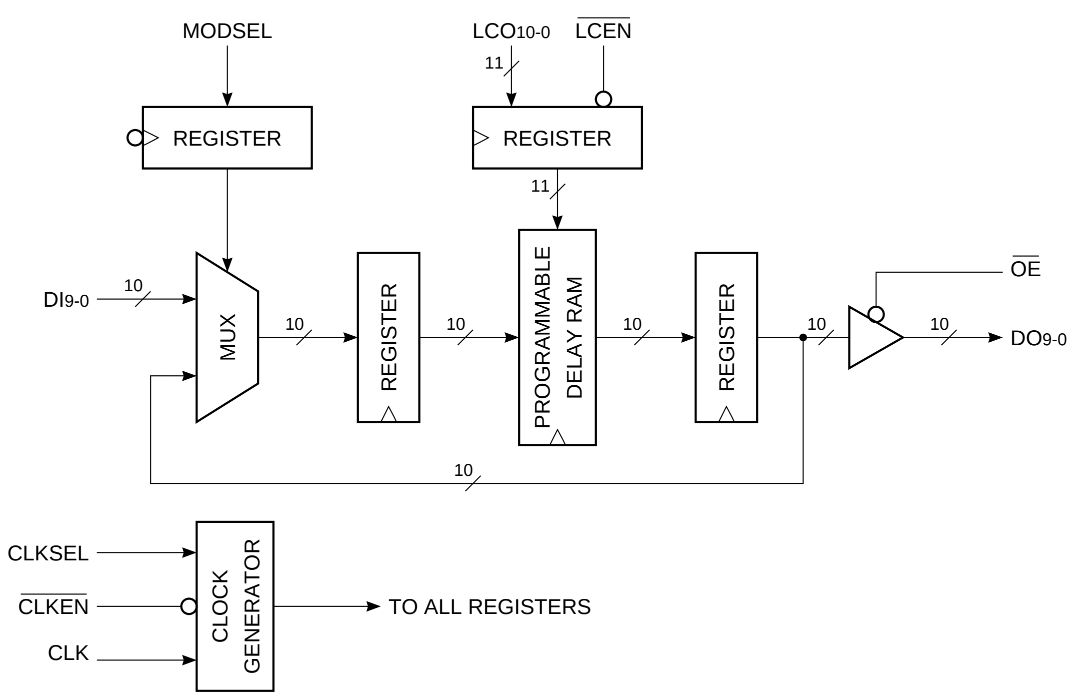
DESCRIPTION

The **LF9501** is a high-speed, 10-bit programmable line buffer. Some applications the LF9501 is useful for include sample rate conversion, data time compression / expansion, software controlled data alignment, and programmable serial data shifting. By using the MODSEL pin, two different modes of operation can be selected: delay mode and data recirculation mode. The delay mode provides a minimum of 2 to a maximum of 1281 clock cycles of delay between the input and output of the device. The data recirculation mode provides a feedback path from the data output to the data input for use as a programmable circular buffer.

By using the length control input (LC_{10-0}) and the length control enable ($\overline{LCEN}$) the length of the delay buffer or amount of recirculation delay can be programmed. Providing a delay value on the LC_{10-0} inputs and driving $\overline{LCEN}$ LOW will load the delay value into the length control register on the next selected clock edge. Two registers, one preceeding the programmable delay RAM and one following, are included in the delay path. Therefore, the programmed delay value should equal the desired delay minus 2. This consequently means that the value loaded into the length control register must range from 0 to 1279 (to provide an overall range of 2 to 1281).

The active edge of the clock input, either positive or negative edge, can be selected with the clock select (CLKSEL) input. All timing is based on the active clock edge selected by CLKSEL. Data can be held temporarily by using the clock enable ($\overline{CLKEN}$) input.

LF9501 Block Diagram



SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The active edge of CLK, selected by CLKSEL, strobes all registers. All timing specifications are referenced to the active edge of CLK.

Inputs

DI_{9-0} — Data Input

10-bit data, from the data input, is latched into the device on the active edge of CLK when MODSEL is LOW.

LC_{10-0} — Length Control Input

The 11-bit value is used to specify the length of the delay buffer, between DI_{9-0} and DO_{9-0}, or the amount of recirculation delay. An integer value ranging from 0 to 1279 is used to select a delay ranging from 2 to 1281 clock cycles. The value placed on the LC_{10-0} inputs is equal to the desired delay minus 2. The data presented on LC_{10-0} is loaded into the device on the active edge of CLK, selected by CLKSEL, in conjunction with $\overline{LCEN}$ being driven LOW.

Outputs

DO_{9-0} — Data Output

The 10-bit data output appears on DO_{9-0} on the Nth clock cycle, where N is the overall delay (desired delay).

Controls

$\overline{LCEN}$ — Length Control Enable

When $\overline{LCEN}$ is driven LOW, the next active clock edge will cause the loading of the delay value present at the LC_{10-0} input.

$\overline{OE}$ — Output Enable

The Output Enable controls the state of DO_{9-0}. Driving $\overline{OE}$ LOW enables the output port. When $\overline{OE}$ is HIGH, DO_{9-0} is placed in a high-impedance state. The internal transfer of data is not affected by this control.

MODSEL — Mode Select

The Mode Select pin is used to choose the desired mode of operation: data delay mode or data recirculation mode. Driving MODSEL LOW places the device in the delay mode. The device operates as a programmable pipeline register. New data from the DI_{9-0} input is loaded on every active edge of CLK. Driving MODSEL HIGH places the device in the data recirculation mode. The device operates as a programmable circular buffer. The output of the device is routed back to the input. MODSEL may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met.

CLKSEL — Clock Select

The CLKSEL control allows the selection of the active edge of CLK. A LOW on CLKSEL selects negative-edge triggering of the device. Driving CLKSEL HIGH selects positive-edge triggering. All timing specifications are referrenced to the selected active edge of CLK.

$\overline{CLKEN}$ — Clock Enable

The Clock Enable control enables and disables the CLK input. Driving $\overline{CLKEN}$ LOW enables CLK and causes the device to operate in a normal fashion. When $\overline{CLKEN}$ is HIGH, CLK is disabled and the device will hold all internal operations and data. $\overline{CLKEN}$ may be changed during device operation (synchronously), however, the required setup and hold times, with respect to CLK, must be met. The changing of $\overline{CLKEN}$ takes effect on the active edge of CLK following the edge in which it was latched.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature .... –65°C to +150°C
Operating ambient temperature .... –55°C to +125°C
V_{CC} supply voltage with respect to ground .... –0.5 V to +7.0 V
Input signal with respect to ground .... –0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output .... –0.5 V to V_{CC} + 0.5 V
Output current into low outputs .... 25 mA
Latchup current .... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

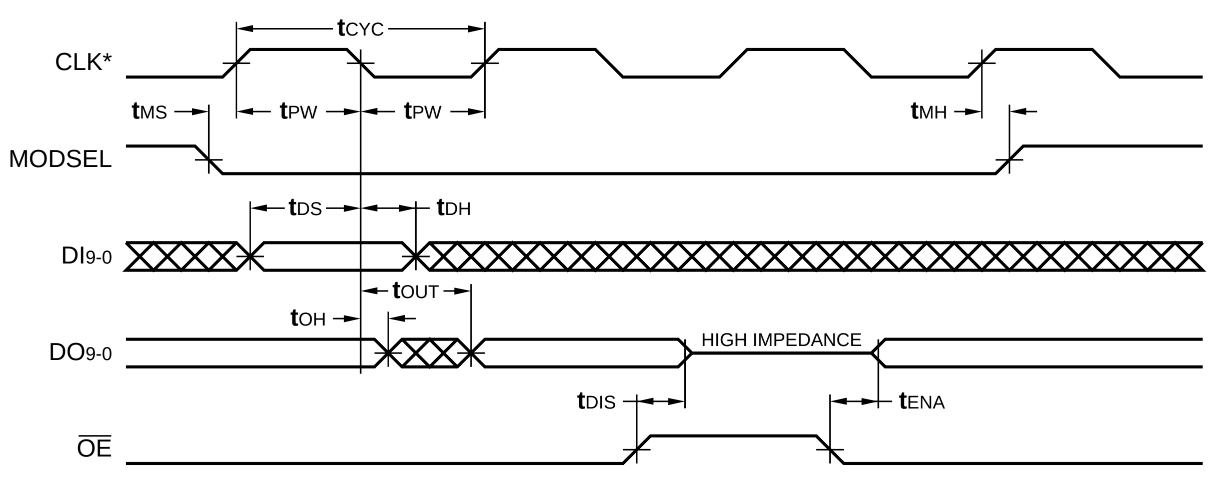
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			125	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF9501–									
		40*		31*		25		20		15*	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{CYC}	Cycle Time	40		31		25		20		15	
t_{PW}	Clock Pulse Width	15		12		10		8		6	
t_{DS}	Data Input Setup Time	12		10		8		6		5	
t_{DH}	Data Input Hold Time	2		2		2		2		0	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6		5	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2		0	
t_{LS}	Length Control Input Setup Time	13		10		8		6		5	
t_{LH}	Length Control Input Hold Time	2		2		2		2		0	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6		5	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2		0	
t_{MS}	Mode Select Setup Time	13		10		8		6		5	
t_{MH}	Mode Select Hold Time	2		2		2		2		0	
t_{OUT}	Clock to Data Out		22		16		15		14		10
t_{OH}	Output Hold Time (Note 8)	4		4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14		12

FUNCTIONAL TIMING — $\overline{\text{CLKSEL}}$ LOW



***When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.**

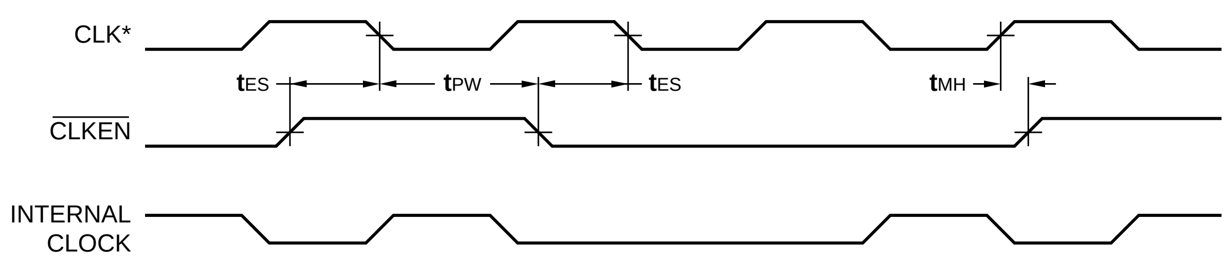
***DISCONTINUED SPEED GRADE**

SWITCHING CHARACTERISTICS

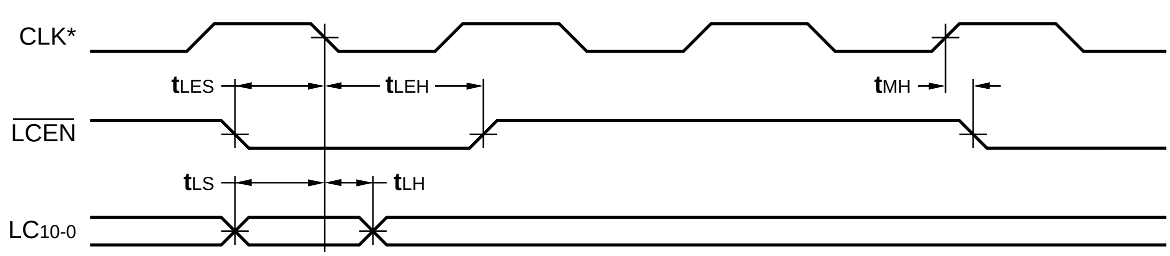
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF9501–									
		40*		31*		25		20		15*	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{CYC}	Cycle Time	40		31		25		20		15	
t_{PW}	Clock Pulse Width	15		12		10		8		6	
t_{DS}	Data Input Setup Time	12		10		8		6		5	
t_{DH}	Data Input Hold Time	2		2		2		2		0	
t_{ES}	Clock Enable to Clock Setup Time	12		10		8		6		5	
t_{EH}	Clock Enable to Clock Hold Time	2		2		2		2		0	
t_{LS}	Length Control Input Setup Time	13		10		8		6		5	
t_{LH}	Length Control Input Hold Time	2		2		2		2		0	
t_{LES}	Length Control Enable to Clock Setup Time	13		10		8		6		5	
t_{LEH}	Length Control Enable to Clock Hold Time	2		2		2		2		0	
t_{MS}	Mode Select Setup Time	13		10		8		6		5	
t_{MH}	Mode Select Hold Time	2		2		2		2		0	
t_{OUT}	Clock to Data Out		22		16		15		14		10
t_{OH}	Output Hold Time (Note 8)	4		4		4		4		4	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		15		14		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		24		15		14		12

CLOCK ENABLE TIMING — $\overline{\text{CLKSEL}}$ LOW



LENGTH CONTROL TIMING — $\overline{\text{CLKSEL}}$ LOW



***When $\overline{\text{CLKSEL}}$ is HIGH, assume CLK is inverted.**

***DISCONTINUED SPEED GRADE**

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

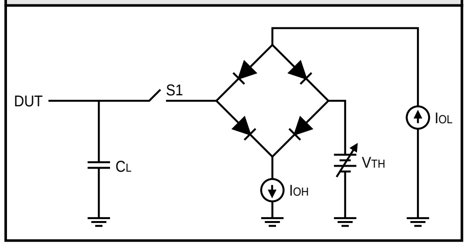
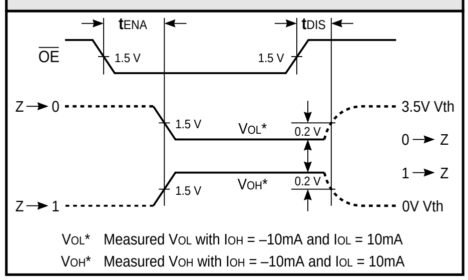
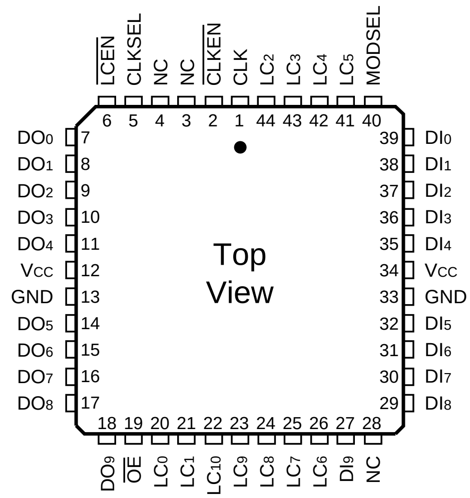


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

44-pin



Speed	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — Commercial Screening
25 ns	LF9501JC25
20 ns	LF9501JC20
	–40°C to +85°C — Commercial Screening