LMA1009/2009
12 x 12-bit Multiplier-Accumulator

LOGIC DEVICES INCORPORATED

FEATURES

- 20 ns Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces Fairchild TDC1009/TMC2009
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- 68-pin PLCC, J-Lead

DESCRIPTION

The **LMA1009** and **LMA2009** are high-speed, low power 12-bit multiplier-accumulators. They are pin-for-pin equivalent to the TRW TDC1009/TMC2009 multiplier-accumulators. The LMA1009 and LMA2009 are functionally identical; they differ only in packaging. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1009/2009 produces the 24-bit product of two 12-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 27-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

The ACC and SUB inputs control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW and SUB LOW, no accumulation occurs and the next product is loaded directly into the accumulator register. ACC LOW and SUB HIGH is undefined.

The LMA1009/2009 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 12 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

LMA1009/2009 BLOCK DIAGRAM

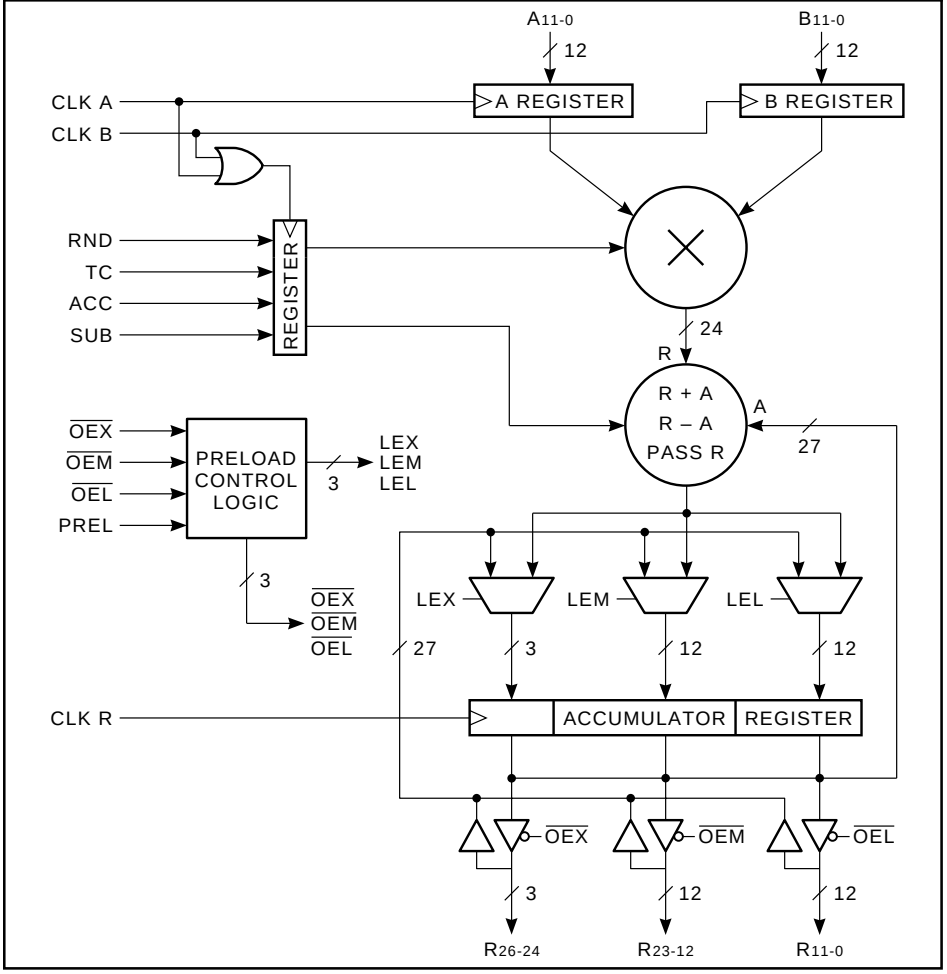


Table 1. Preload Truth Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

Figure 1a. Input Formats

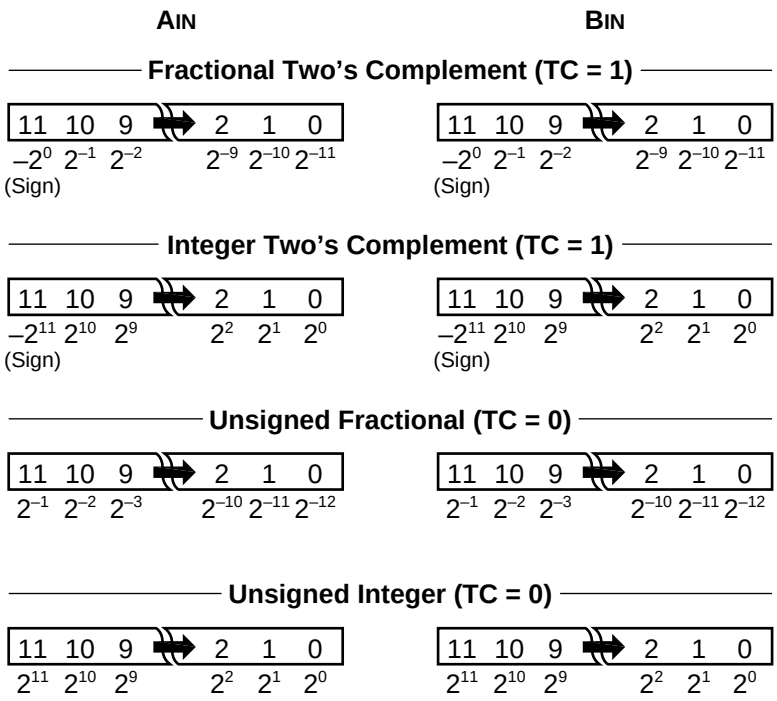
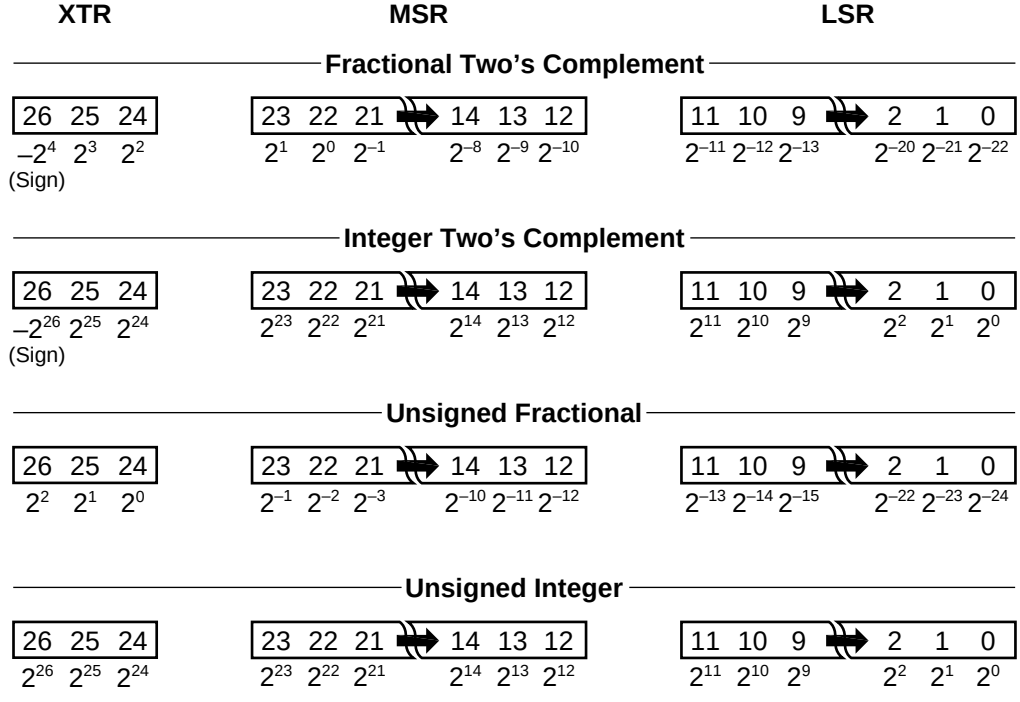


Figure 1b. Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 8.0 mA			0.5	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±20	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±20	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)		12	25	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

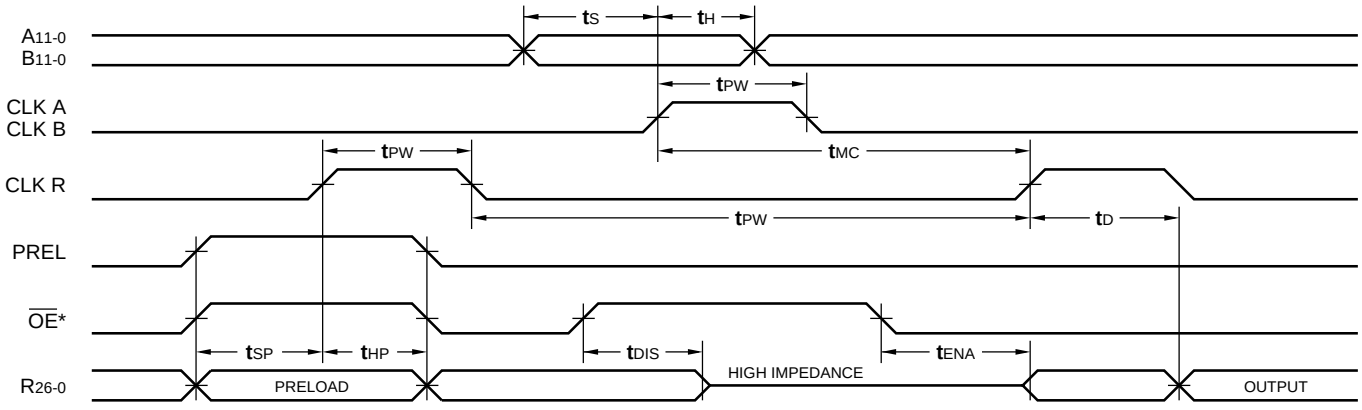
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1009/2009–							
		75*		55*		45		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45		20
t_{PW}	Clock Pulse Width	15		15		15		8	
t_S	Input Register Setup Time	15		15		12		10	
t_H	Input Register Hold Time	2		2		2		2	
t_{SP}	Preload Setup Time	15		15		12		10	
t_{HP}	Preload Hold Time	2		2		2		2	
t_D	Output Delay		30		25		25		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		25		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1009/2009–							
		95*		65*		55*		25*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		95		65		55		25
t_{PW}	Clock Pulse Width	20		20		15		10	
t_S	Input Register Setup Time	20		20		15		12	
t_H	Input Register Hold Time	2		2		2		2	
t_{SP}	Preload Setup Time	20		20		15		12	
t_{HP}	Preload Hold Time	2		2		2		2	
t_D	Output Delay		35		30		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		35		30		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		30		30		20

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

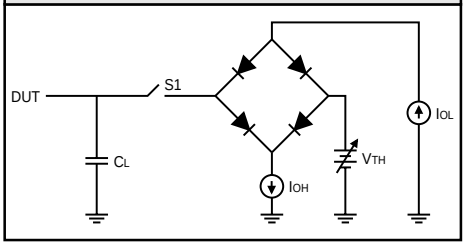
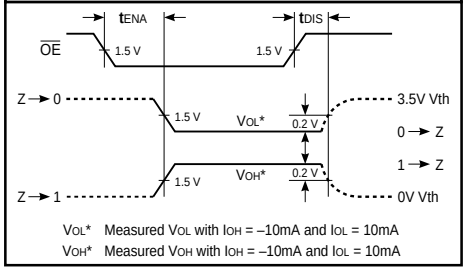
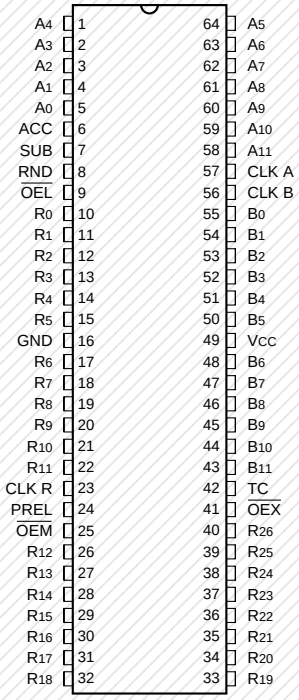


FIGURE B. THRESHOLD LEVELS



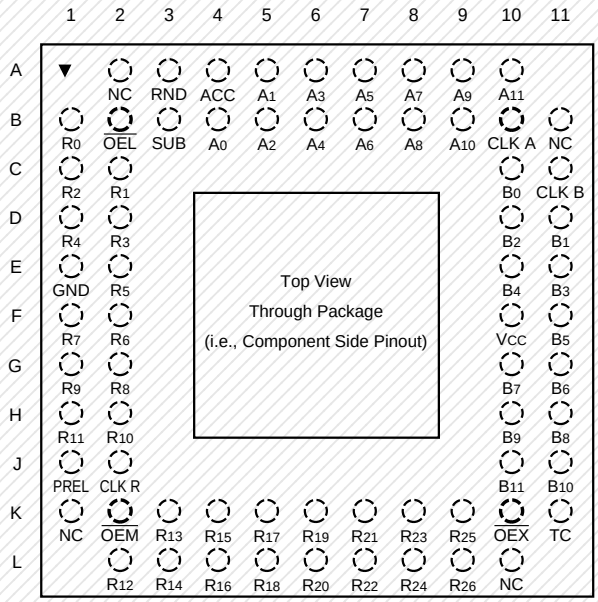
LMA1009 — ORDERING INFORMATION

64-pin



Discontinued Package

68-pin

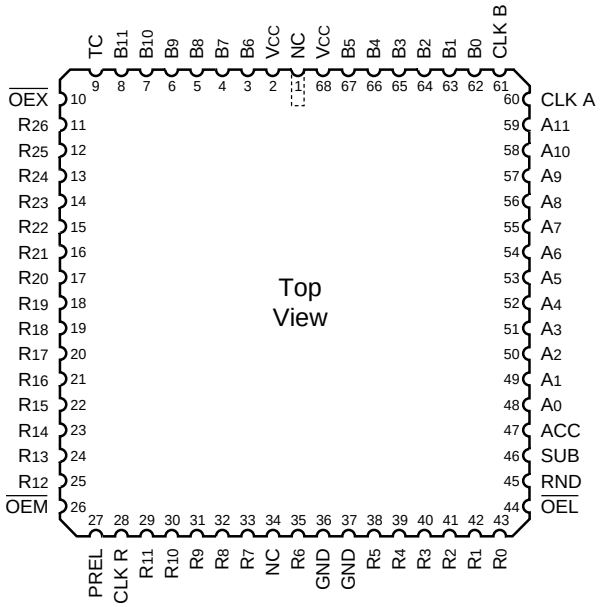


Discontinued Package

Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING	
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	

LMA2009 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	
	0°C to +70°C — COMMERCIAL SCREENING	
45 ns	LMA2009JC45	
20 ns	LMA2009JC20	
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	