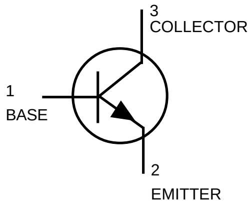
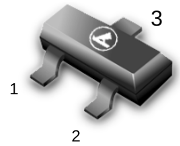
General Purpose Transistors

NPN Silicon

BCW72LT1





CASE 318–08, STYLE 6
SOT–23 (TO–236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	45	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR– 5 Board, (1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J , T_{stg}	–55 to +150	°C

DEVICE MARKING

BCW72LT1 = K2

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 2.0mAdc, V_{EB} = 0)	$V_{(BR)CEO}$	45	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 2.0 mAdc, V_{EB} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 µAdc, I_E= 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E= 10 µAdc, I_C= 0)	$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current	I_{CBO}				
(V_{CB}= 20 Vdc, I_E= 0)		—	—	100	nAdc
(V_{CB}= 20 Vdc, I_E= 0, T_A=100°C)		—	—	10	µAdc

1. FR– 5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

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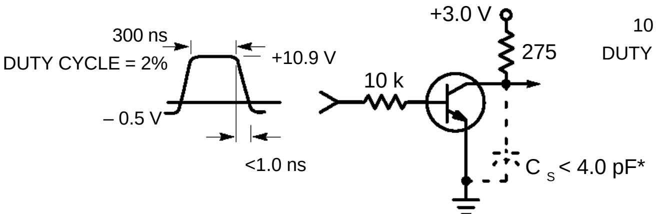
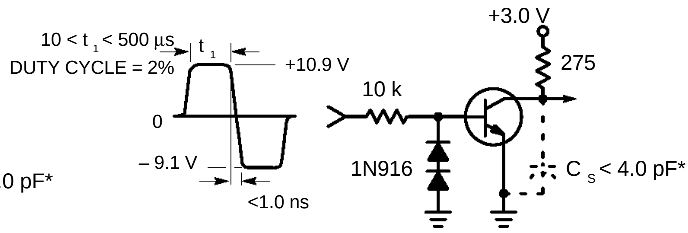
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C= 2.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	200	—	450	—
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)		—	—	0.25	
(I_C = 50 mAdc, I_B = 2.5 mAdc)		—	0.21	—	
Base–Saturation Voltage (I_C = 50 mAdc, I_B = 2.5 mAdc)	$V_{BE(on)}$	—	0.85	—	Vdc
Base–Emitter On Voltage (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	0.6	—	0.75	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	—	300	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E= 0, f = 1.0 MHz)	C_{obo}	—	—	4.0	pF
Input Capacitance (I_E = 0, V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{ibo}	—	9.0	—	pF
Noise Figure (I_C = 0.2 mAdc, V_{CE} = 5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	NF	—	—	10	dB

EQUIVALENT SWITCHING TIME TEST CIRCUITS





*Total shunt capacitance of test jig and connectors

Figure 1. Turn–On Time

Figure 2. Turn–Off Time

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TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

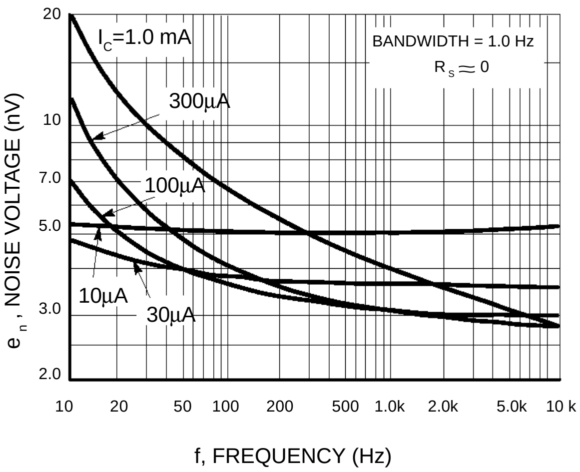

Figure 3. Noise Voltage

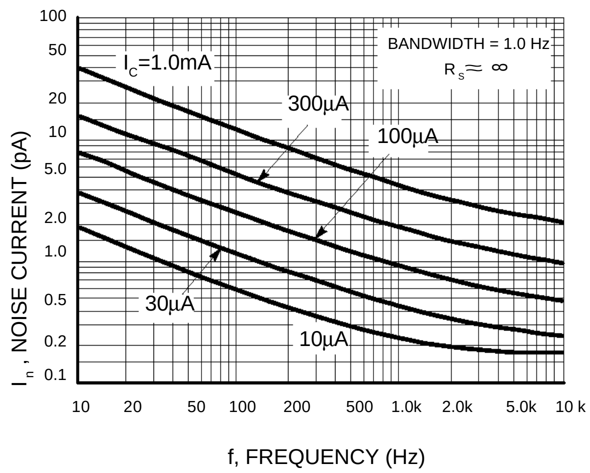

Figure 4. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

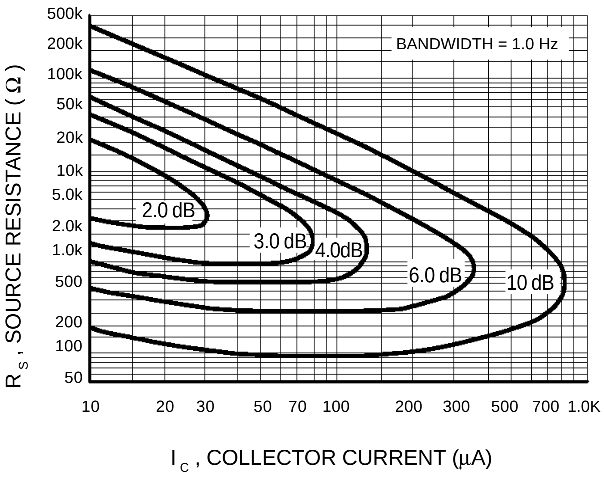

Figure 5. Narrow Band, 100 Hz

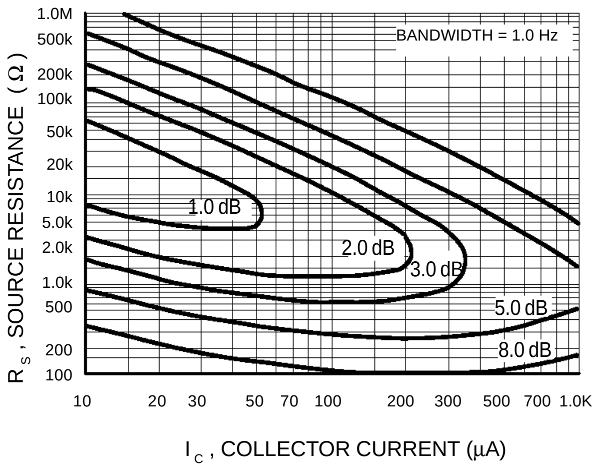

Figure 6. Narrow Band, 1.0 kHz

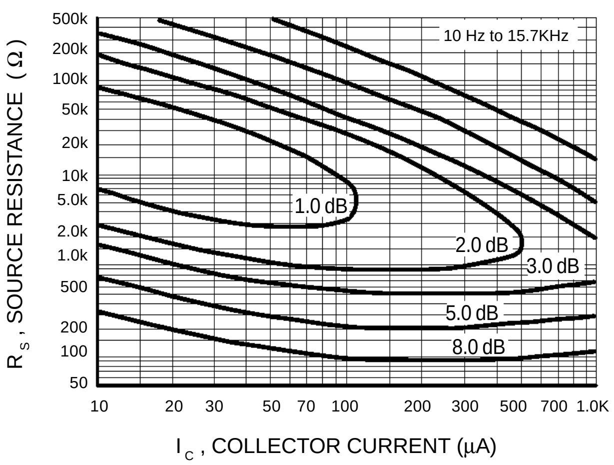

Figure 7. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10} \left(\frac{e_n^{\,2} + 4KTR_S + I_n^{\,2} R_S^{\,2}}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/ °K)
T = Temperature of the Source Resistance (°K)
R_s = Source Resistance (Ω)

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TYPICAL STATIC CHARACTERISTICS

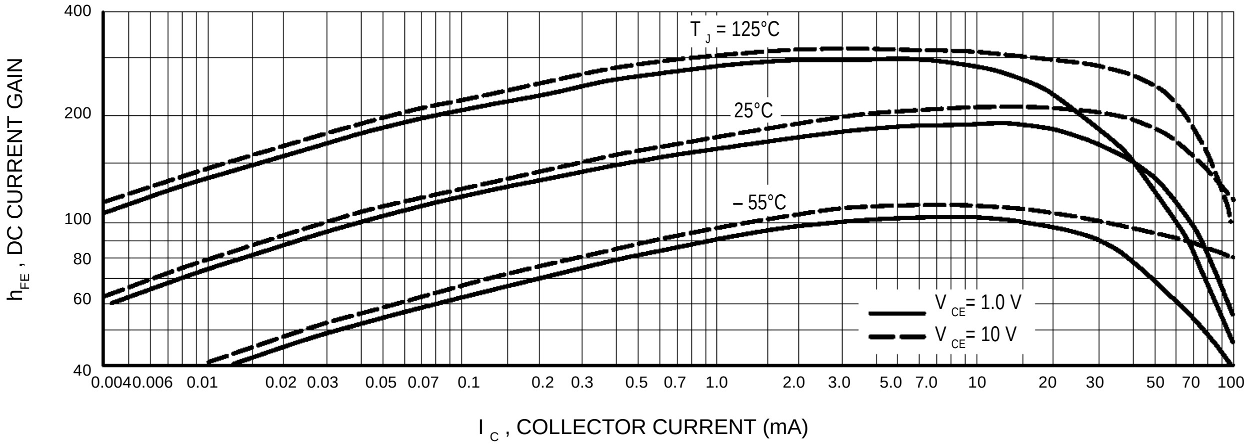

Figure 8. DC Current Gain

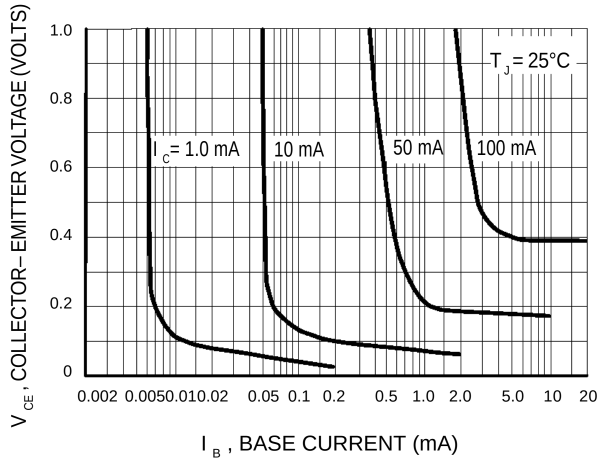

Figure 9. Collector Saturation Region

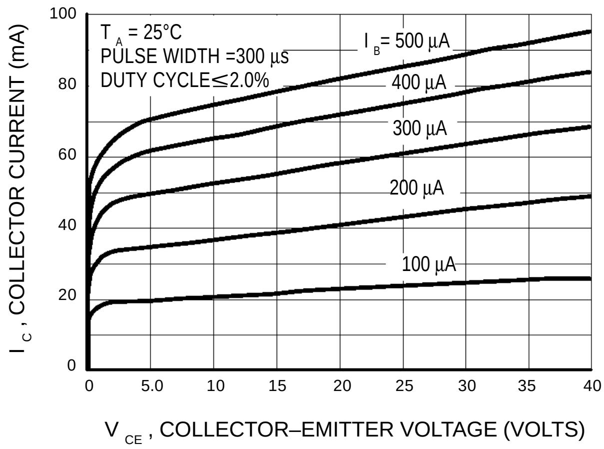

Figure 10. Collector Characteristics

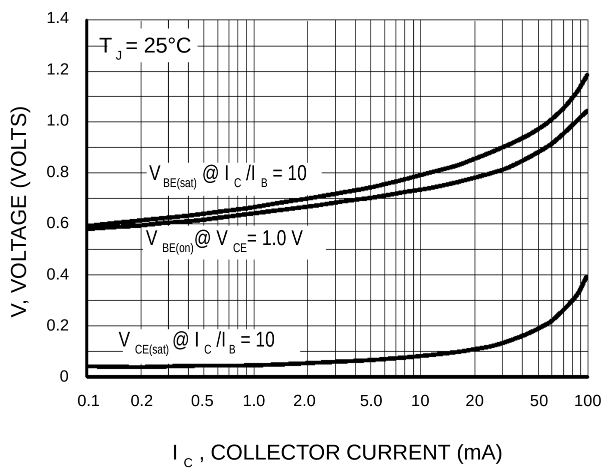

Figure 11. "On" Voltages

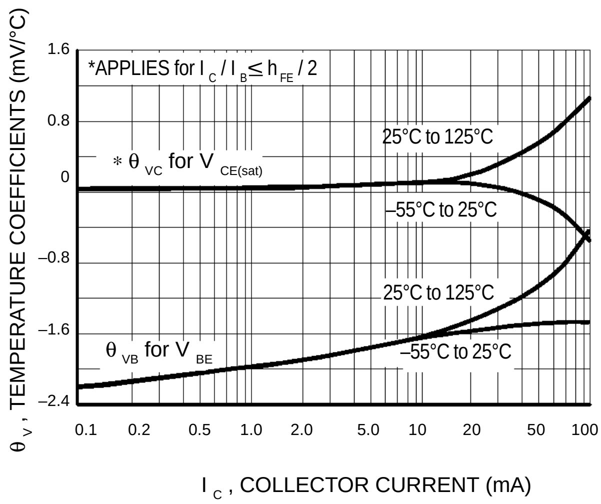

Figure 12. Temperature Coefficients

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TYPICAL DYNAMIC CHARACTERISTICS

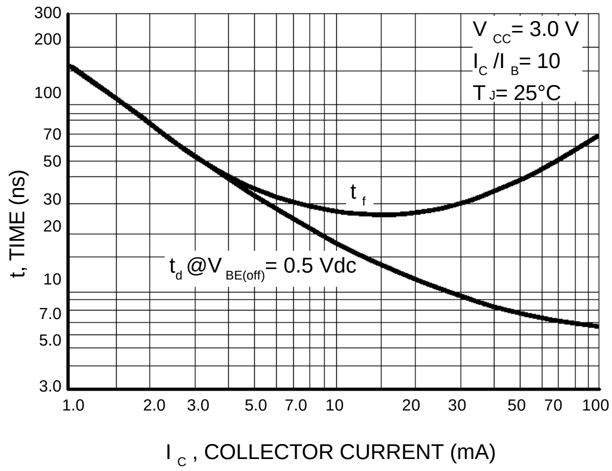

Figure 13. Turn–On Time

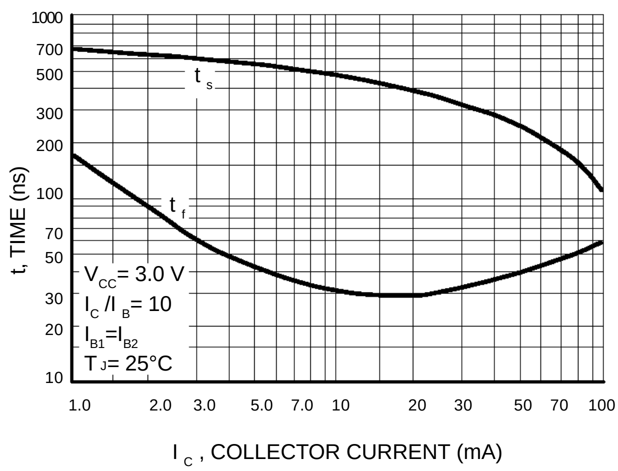

Figure 14. Turn–Off Time

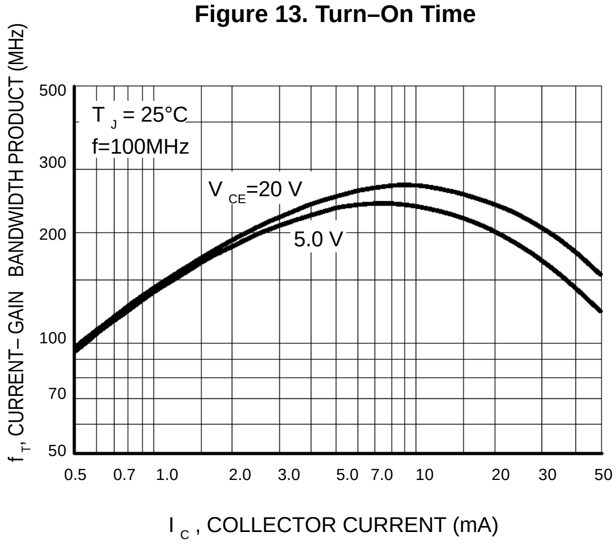

Figure 15. Current–Gain — Bandwidth Product

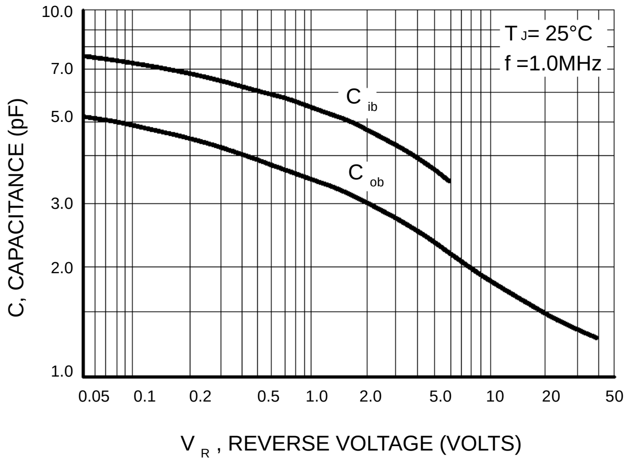

Figure 16. Capacitance

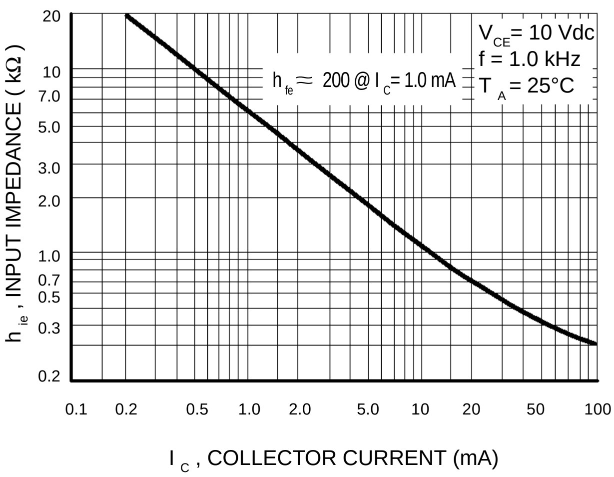

Figure 17. Input Impedance

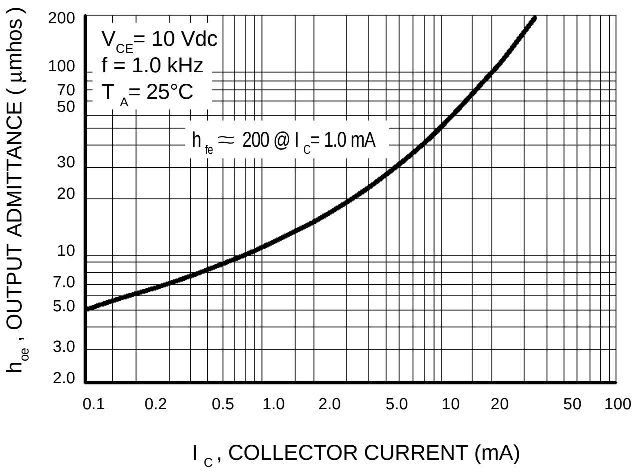

Figure 18. Output Admittance

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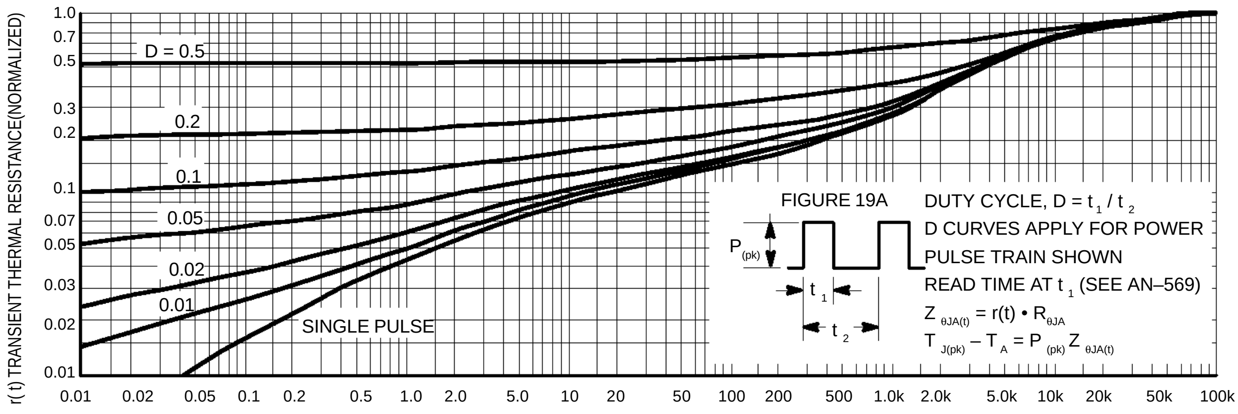

Figure 19. Thermal Response

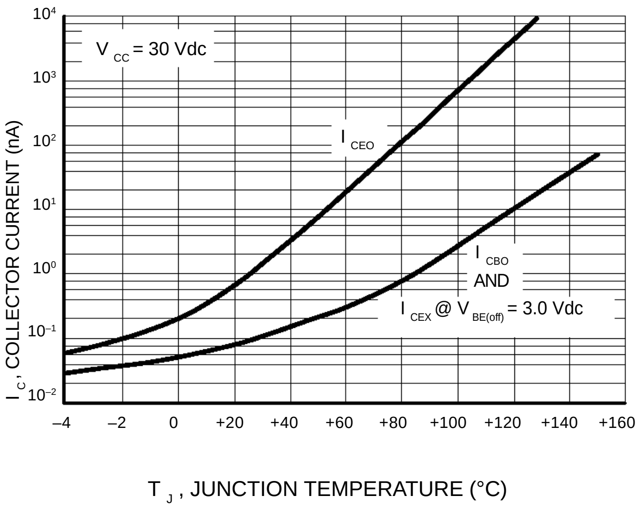

Figure 19A.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms. (D = 0.2)

Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see AN–569.

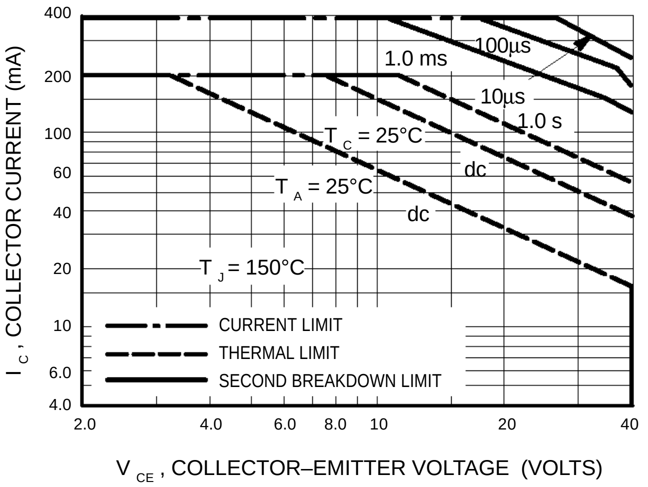

Figure 20.

The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 20 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.