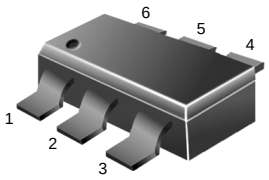
Low Voltage Bias Stabilizer with Enable

MDC5001T1

SILICON SMALLBLOCK™ INTEGRATED CIRCUIT



SOT–363
CASE 419B–01 STYLE 19

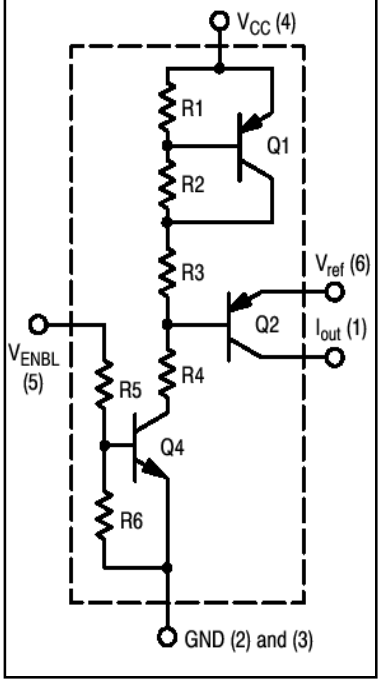
- Maintains Stable Bias Current in N–Type Discrete Bipolar Junction and Field Effect Transistors
- Provides Stable Bias Using a Single Component Without Use of Emitter Ballast and Bypass Components
- Operates Over a Wide Range of Supply Voltages Down to 1.8 Vdc
- Reduces Bias Current Variation Due to Temperature and Unit–to–Unit Parametric Changes
- Consumes <0.5 mW at V_{CC} = 2.75 V
- Active High Enable is CMOS Compatible

This device provides a reference voltage and acts as a DC feedback element around an external discrete, NPN BJT or N–Channel FET. It allows the external transistor to have its emitter/source directly grounded and still operate with a stable collector/drain DC current. It is primarily intended to stabilize the bias of discrete RF stages operating from a low voltage regulated supply, but can also be used to stabilize the bias current of any linear stage in order to eliminate emitter/source bypassing and achieve tighter bias regulation over temperature and unit variations. The “ENABLE” polarity nulls internal current, Enable current, and RF transistor current in “STANDBY.” This device is intended to replace a circuit of three to six discrete components.

The combination of low supply voltage, low quiescent current drain, and small package make the MDC5001T1 ideal for portable communications applications such as:

- Cellular Telephones
- Pagers
- PCN/PCS Portables
- GPS Receivers
- PCMCIA RF Modems
- Cordless Phones
- Broadband and Multiband Transceivers and Other Portable Wireless Products.

INTERNAL CIRCUIT DIAGRAM



MDC5001T1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	15	V_{dc}
Ambient Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C
Collector Emitter Voltage (Q2)	V_{CEO}	–15	V
Enable Voltage (Pin 5)	V_{ENBL}	V_{CC}	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Power Dissipation	P D		mW
(FR–5 PCB of 1, × 0.75, × 0.062,, T_A = 25°C)		150	
Derate above 25°C		1.2	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	833	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Supply Voltage	V_{CC}	1.8	2.75	10	Volts
Power Supply Current (V_{CC} = 2.75 V)	I_{CC}	—	130	200	mA
V_{ref}, I_{out} are unterminated					
See Figure 8					
Q2 Collector Emitter Breakdown Voltage	$V_{(BR)CEO2}$	15			Volts
(I_{C2} = 10 µA, I_{B2} = 0)					
Reference Voltage (V_{ENBL} = V_{CC} = 2.75 V, V_{out} = 0.7 V)	V ref				Volts
(I_{out} = 30 µA)		2.050	2.075	2.100	
(I_{out} = 150 µA)		2.110	2.135	2.160	
See Figure 1					
Reference Voltage (V_{ENBL} = V_{CC} = 2.75 V, V_{out} = 0.7 V,					
–40°C ≤ T_A ≤+85°C)					
V_{CC} Pulse Width = 10 mS, Duty Cycle = 1%	ΔV_{ref}				mV
(I_{out} = 10 µA)			±5.0	±10	
(I_{out} = 30 µA)			±15	±30	
(I_{out} = 100 µA)			±25	±50	
See Figures 2 and 11					

MDC5001T1

The following SPICE models are provided as a convenience to the user and every effort has been ade to insure their accuracy. However, no responsibility for their accuracy is assumed by ON Semiconductor.

.MODEL Q4 NPN		.MODEL Q1, Q2 PNP	
BF = 136	NE = 1.6	BF = 87	NK = 0.5
BR = 0.2	NF = 1.005	BR = 0.6	NR = 1.0
CJC = 318.6 f	RB = 140	CJC = 800E–15	RB = 720
CJE = 569.2 f	RBM = 70	CJE = 46E–15	RBM = 470
CJS = 1.9 p	RC = 180	EG = 1.215	RC = 180
EG = 1.215	RE = 1.6	FC = 0.5	RE = 26
FC = 0.5	TF = 553.6 p	IKF = 3.8E–04	TF = 15E–9
IKF = 24.41 m	TR = 10 n	IKR = 2.0	TR = 50E–09
IKR = 0.25	VAF = 267.6	IRB = 0.9E–3	VAF = 54.93
IRB = 0.0004	VAR = 12	IS = 1.027E–15	VAR = 20
IS = 256E–18	VJC = 0.4172	ISC = 10E–18	VAR = 20
ISC = 1 f	VJE = 0.7245	ISE = 1.8E–15	VJC = 0.4172
ISE = 500E–18	VJS = 0.39	ITF = 2E–3	VJE = 0.4172
ITF = 0.9018	VTF = 10	MJC = 0.2161	VTF = 10
MJC = 0.2161	XTB = 1.5	MJE = 0.2161	XTB = 1.5
MJE = 0.3373	XTF = 2.077	NC = 0.8	XTF = 2.0
MJS = 0.13	XTI = 3	NE = 1.38	XTI = 3
NC = 1.09		NF = 1.015	

RESISTOR VALUES

R_1 = 12 K
R_2 = 6 K
R_3 = 3.4 K
R_4 = 12 K
R_5 = 20 K
R_6 = 40 K

These models can be retrieved electronically by accessing the ON Semiconductor Web page at http://design–net.sps.mot.com/models and searching the section on SMALLBLOCKE models

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TYPICAL OPEN LOOP CHARACTERISTICS

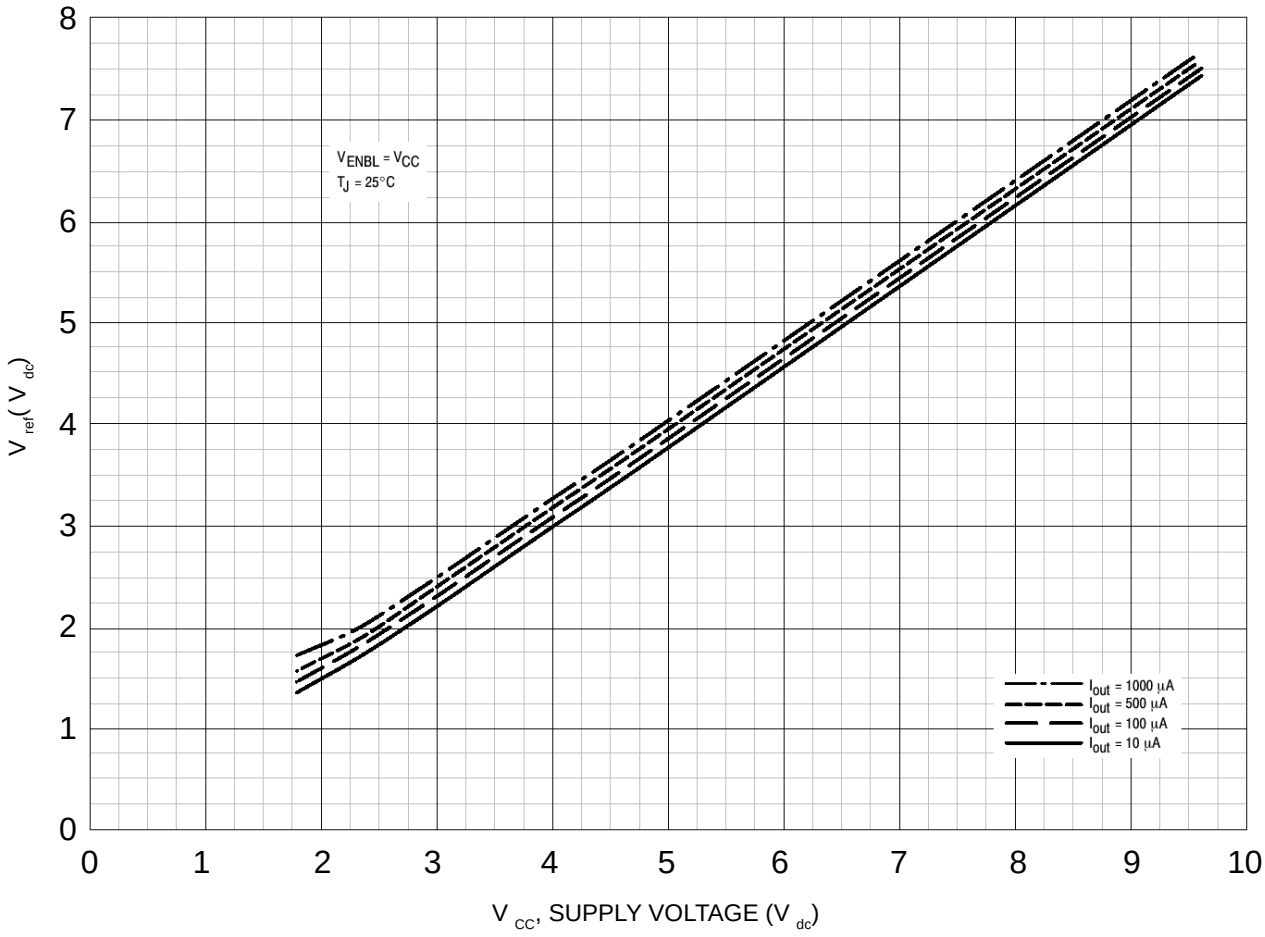


Figure 1. V_{ref} versus V_{CC} @ I_{out}

TYPICAL OPEN LOOP CHARACTERISTICS

(Refer to Circuits of Figures 10 through 15)

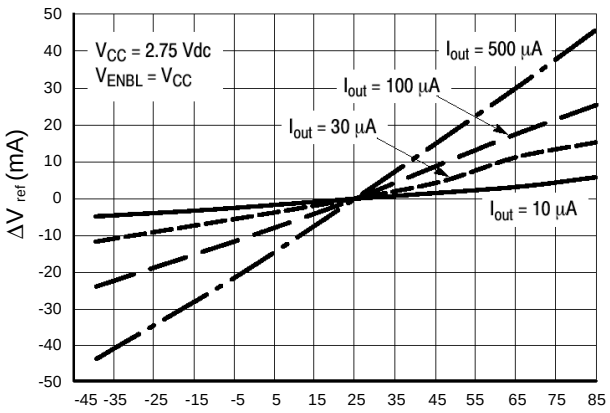


Figure 2. ΔV ref versus T J @ I out

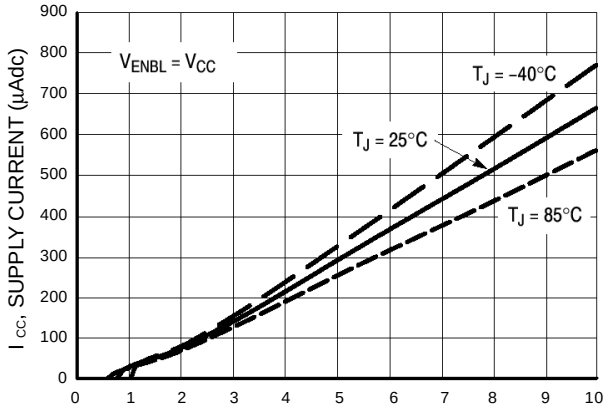


Figure 3. I CC versus V CC @ T J

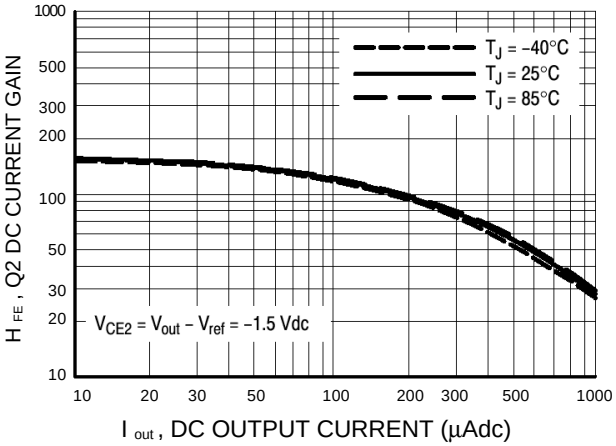


Figure 4. Q2 Current Gain versus Output Current @ T J

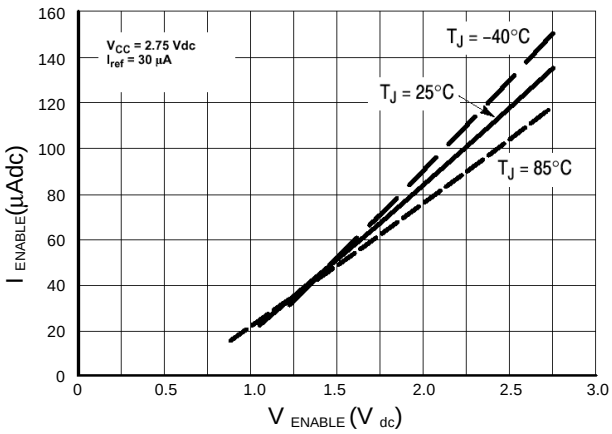


Figure 5. I enable versus V enable

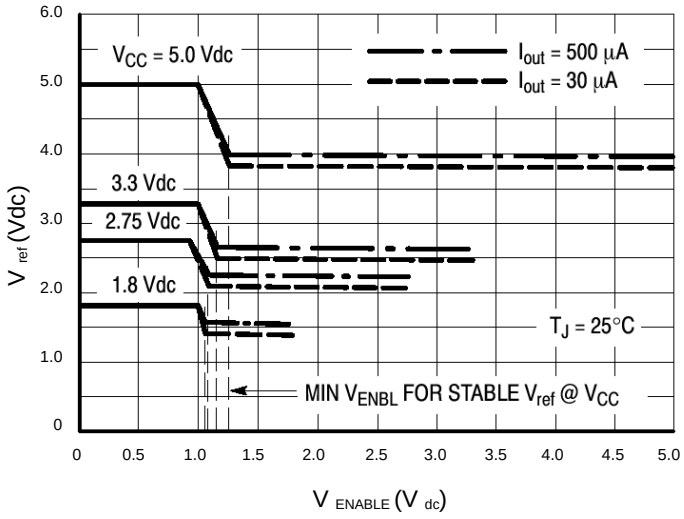
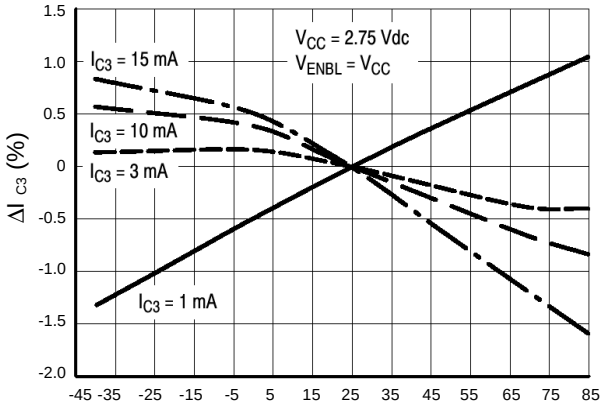


Figure 6. V ref versus V enable @ V CC and I out

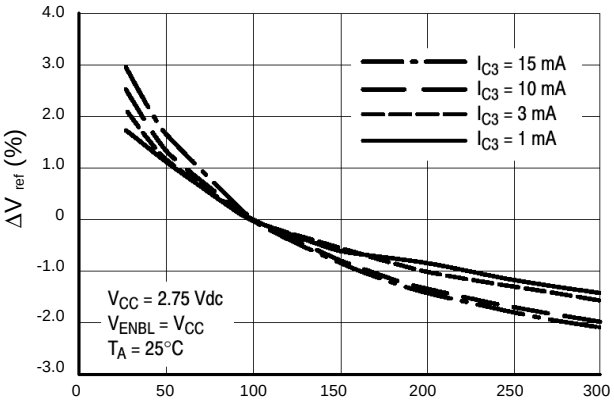
TYPICAL CLOSED LOOP PERFORMANCE

(Refer to Circuits of Figures 16 & 17)



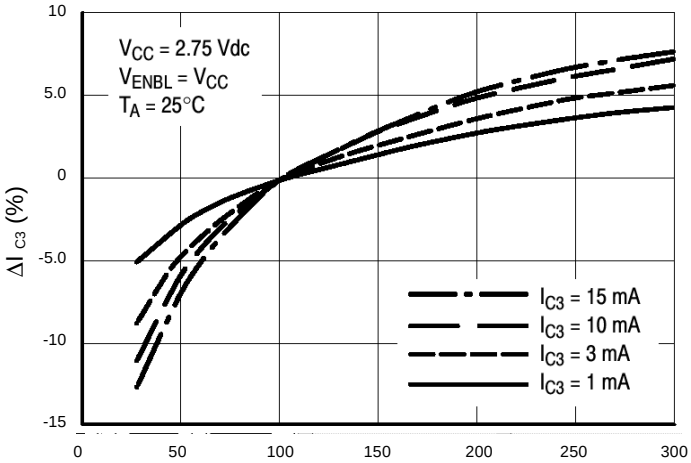
T A , AMBIENT TEMPERATURE (°C)

Figure 7. ΔI C3 versus T A @ I C3



EXTERNAL TRANSISTOR DC BETA @ I C3

Figure 8. ΔV ref versus External Transistor DC Beta @ I C3



H FE , EXTERNAL TRANSISTOR DC BETA

Figure 9. ΔI C3 versus External Transistor DC Beta @ I C3

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OPEN LOOP TEST CIRCUITS

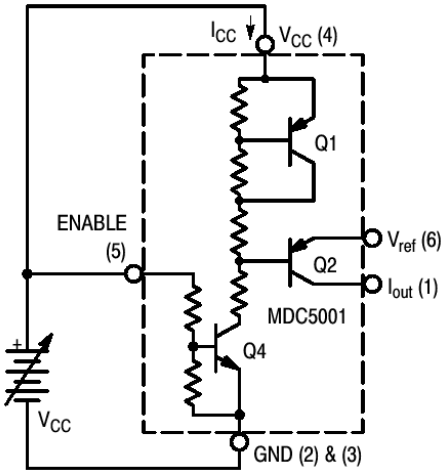


Figure 10. I_{CC} versus V_{CC} Test Circuit

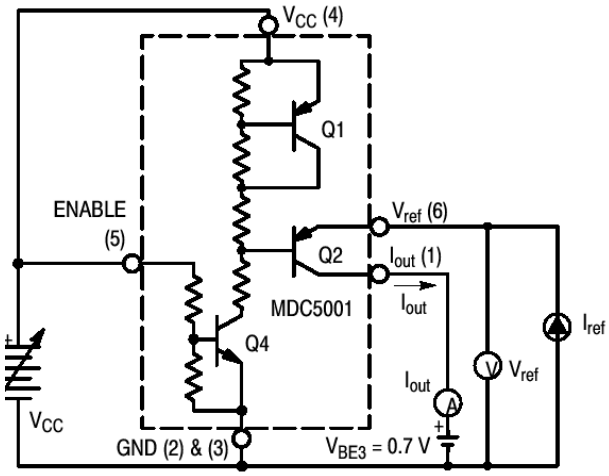


Figure 11. V_{ref} versus V_{CC} Test Circuit

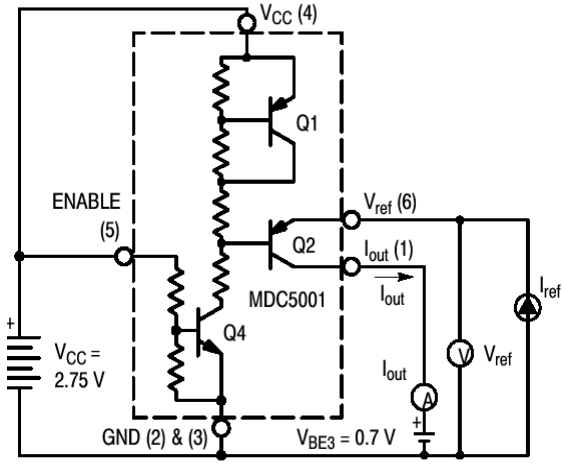


Figure 12. V_{ref} versus T_J Test Circuit

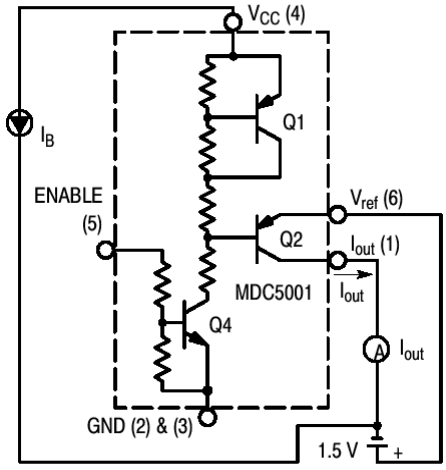


Figure 13. H_{FE} versus I_{out} Test Circuit

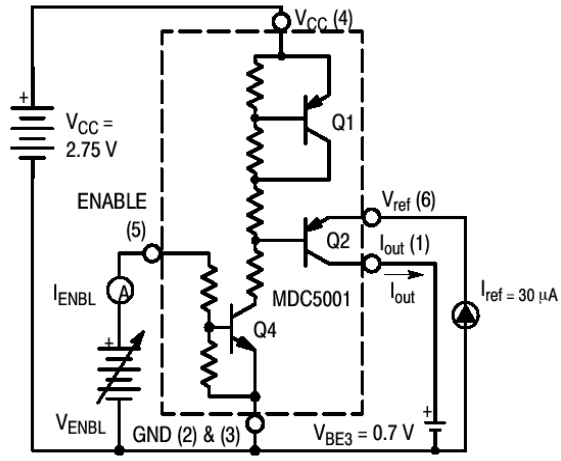


Figure 14. I_{ENBL} versus V_{ENBL} Test Circuit

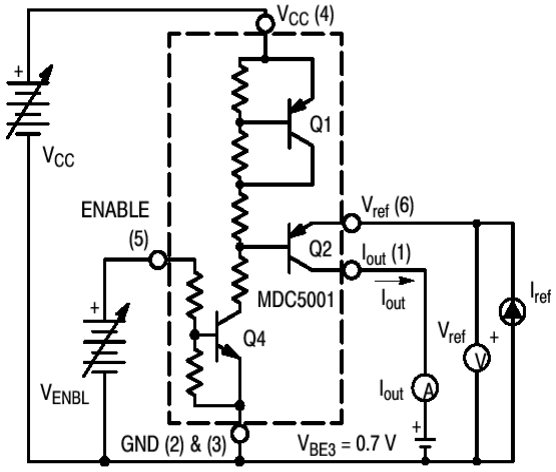


Figure 15. V_{ref} versus V_{ENBL} Test Circuit

NOTE 1: V_{BE3} is used to simulate actual operating conditions that reduce V_{CE2} & H_{FE2}, and increase I_{B2} & V_{ref}.

CLOSED LOOP TEST CIRCUITS

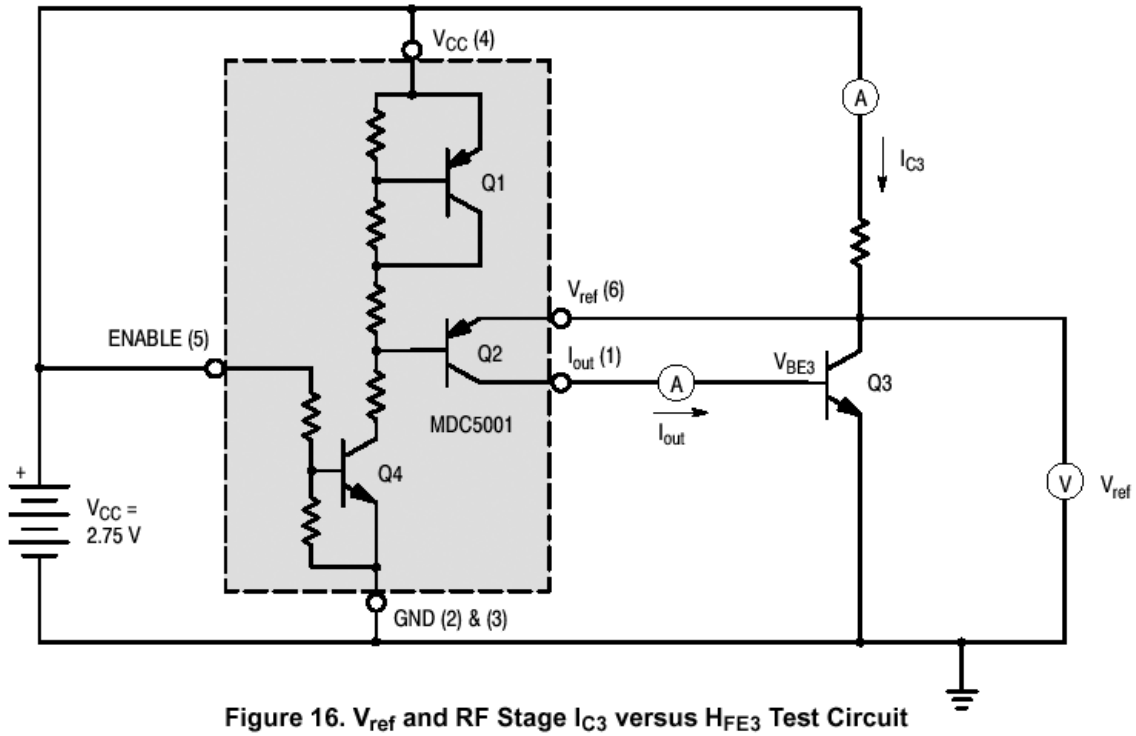


Figure 16. V_{ref} and RF Stage I_{C3} versus H_{FE3} Test Circuit

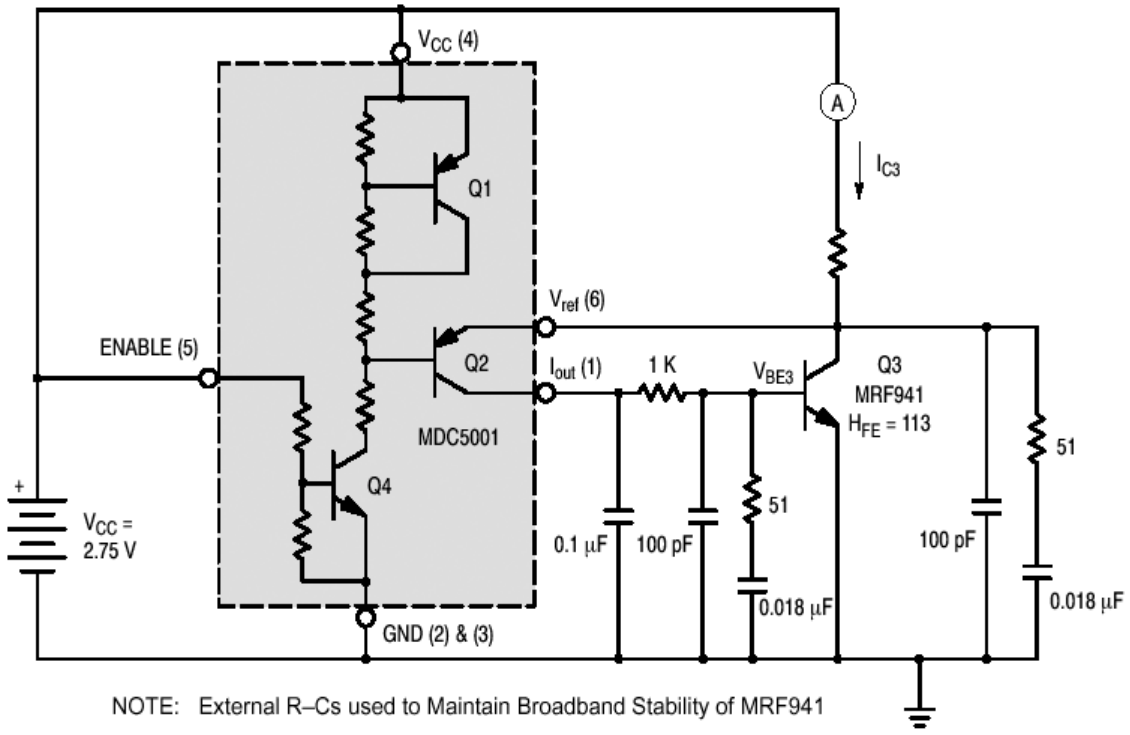
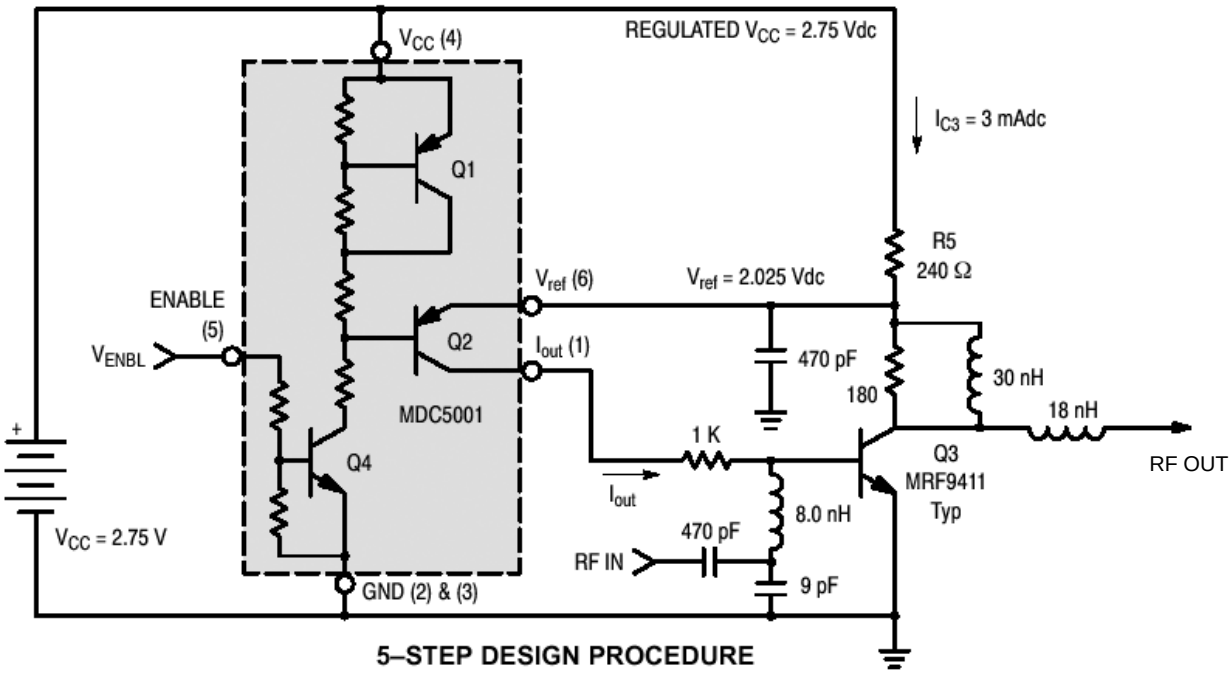


Figure 17. RF Stage I_{C3} versus T_A Test Circuit

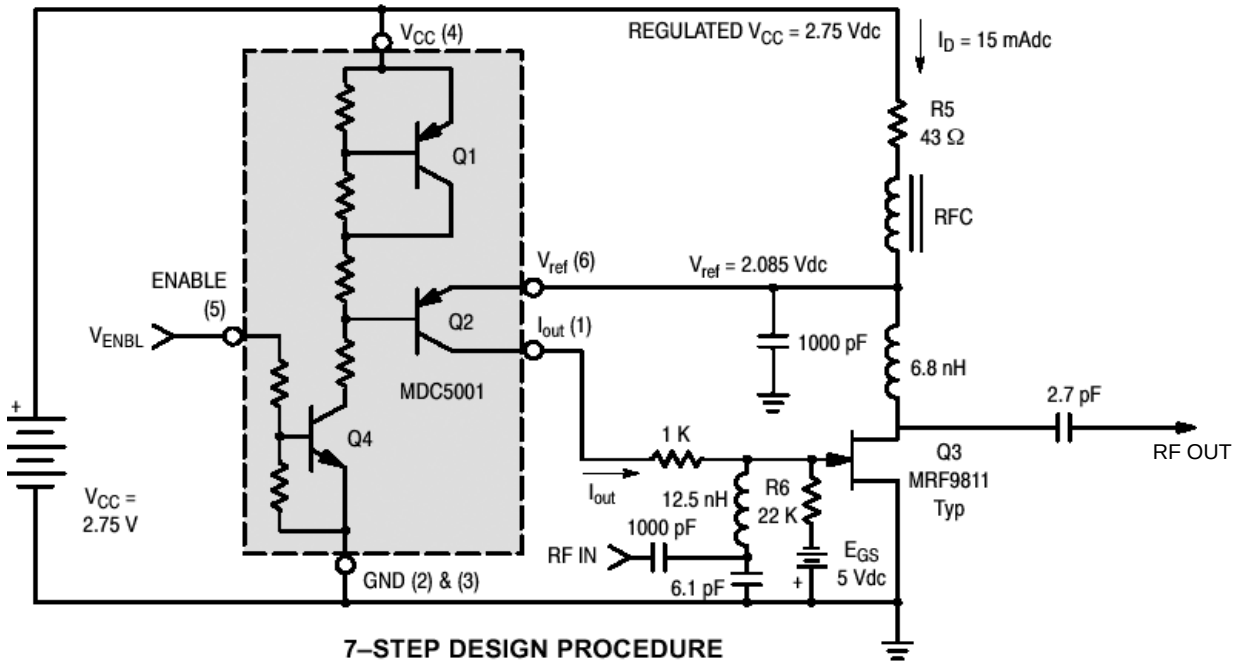
APPLICATION CIRCUITS



Step 1: Choose V_{CC} (1.8 V Min to 10 V Max)
Step 2: Insure that Min V_{ENBL} is . minimum indicated in Figures 5 and 6.
Step 3: Choose bias current, I_{C3} , and calculate needed I_{out} from typ H_{FE3}
Step 4: From Figure 1, read V_{ref} for V_{CC} and I_{out} calculated.
Step 5: Calculate Nominal R5 = (V_{CC} – V_{ref}) ÷ (I_{C3} + I_{out}). Tweak as desired.

Figure 18. Class A Biasing of a Typical 900 MHz BJT Amplifier Application

APPLICATION CIRCUITS



7–STEP DESIGN PROCEDURE

Step 1: Choose V_{CC} (1.8 V Min to 10 V Max)
Step 2: Insure that Min V_{ENBL} is ≥ minimum indicated in Figures 5 and 6.
Step 3: Choose bias current, I_D , and determine needed gate–source voltage, V_{GS} .
Step 4: Choose I_{out} keeping in mind that too large an I_{out} can impair MDC5000 $\Delta V_{ref}/\Delta T_J$ performance (Figure 2) but too large an R6 can cause I_{DGO} & I_{GSO} to bias on the FET.
Step 5: Calculate R6 = (V_{GS} + E_{GS}) ÷ I_{out}
Step 6: From Figure 1, read V_{ref} for V_{CC} & I_{out} chosen
Step 7: Calculate Nominal R5 = (V_{CC} – V_{ref}) ÷ (I_D + I_{out}) . Tweak as desired.

Figure 19. Class A Biasing of a Typical 890 MHz Depletion Mode GaAs FET Amplifier