

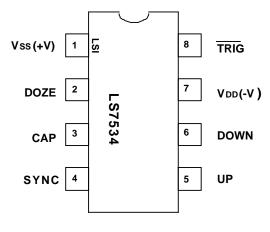
DIMMER LIGHT SWITCH WITH UP AND DOWN CONTROLS

August 1996

FEATURES:

- Phase-lock loop synchronization allows use as a Wall Switch
- Brightness control of incandescent lamps with touch plates (LS7534) or mechanical switches (LS7535)
- Dual Controls eliminate confusion
- Soft turn-on /turn-off
- Controls the "Duty Cycle" from 23% to 88% (conduction angles for AC half-cycles between 41° and 159°, respectively)
- Operates at 50Hz/60Hz line frequency
- Input for slow dimming
- +12V to +18V DC supply voltage (Vss VDD)
- LS7534/LS7535 (DIP); LS7534-S/LS7535-S SOIC - See Figure 1

CONNECTION DIAGRAM - TOP VIEW





DESCRIPTION:

LS7534/LS7535 are monolithic, MOS integrated circuits that are designed for brightness control of incandescent lamps. The outputs of these ICs control the brightness of a lamp by controlling the firing angle of a triac connected in series with the lamp. All internal timings are synchronized with the line frequency by means of a built-in phase-lock loop circuit. The output occurs once every half-cycle of the line frequency. Within the half-cycle, the output can be positioned anywhere between 159° conduction angle for maximum brightness and 41° conduction angle for minimum brightness in relation to the AC line frequency. The positioning of the output is controlled by applying the proper logic levels at the UP and DOWN inputs.

These functions may be implemented with very few interface components which is described in the application examples (See Fig. 5A and 5B). For touch plates, LS7534 is used (Fig. 5A). For mechanical switches, LS7535 is used (Fig. 5B).

In the following Operating Description of the application examples, an Activation is Touch for LS7534 and Switch Closure for LS7535.

Short Activation (34ms to 325ms)

UP - When the lamp is off, if a short activation is applied to the UP input, the lamp brightness is ramped up to full-on or to a previous brightness stored in the memory. The ramp-up time from off to full-on is 2.8 sec. The ramp-up time from off to any other brightness is proportionally shorter. When the lamp is on at any brightness, a short activation applied to the UP input has no effect.

DOWN - If a short activation is applied to the DOWN input, the lamp brightness is ramped down to off. The ramp-down time from full-on to off is 5.6 seconds. The ramp-down time from any other brightness is proportionally shorter. When the lamp is off, a short activation applied to the DOWN input has no effect.

Long Activation (Greater than 334ms)

UP - If a long activation is applied to the UP input, the lamp brightness ramps up from the pre-activation brightness as long as the activation is maintained or until the full brightness is reached. At full brightness any continued long activation has no further effect.

DOWN - If a long activation is applied to the DOWN input, the lamp brightness is ramped down as long as the long activation is maintained or until the minimum brightness is reached. At minimum brightness, any continued long activation has no further effect. When the lamp is off, a long activation applied to the DOWN input has no effect.

TABLE 1									
UP/DOWN SIGNAL DURATION									
INPUT		SHORT 34ms to 325 ms		LONG More than 334ms					
		PRE-ACTIVATION BRIGHTNESS	POST-ACTIVATION BRIGHTNESS	PRE-ACTIVATION BRIGHTNESS	POST-ACTIVATION BRIGHTNESS				
		Off	Memory ** (See Note 1)	Off	Increases from Min.				
UP		Max.	No Change	Max.	No change				
		Intermediate	No Change	Intermediate	Increases from pre- touch brightness				
		Off	No Change	Off	No change				
DOWN		Max.	Off *	Max.	Decreases from Max.				
		Intermediate	Off *	Intermediate	Decreases from pre- touch brightness				

* 5.6 second ramp-down from max. to off. Ramp-down time from any other brightness is proportionally shorter. ** 2.8 second ramp-up from off to max.

NOTE 1: "Memory" refers to the brightness stored in the memory. The brightness is stored in memory when the

lamp is turned off by a short activation. First time after power-up, a short activation produces max. brightness.

INPUT/OUTPUT DESCRIPTION:

Vss (Pin 1)

Supply voltage positive terminal.

DOZE (Pin 2)

A clock applied to this input causes the brightness to decrease in equal increments with each negative transition of the clock. Eventually, when the lamp becomes off, this input has no further effect. The lamp can be turned on again by activating the UP input. For the transition from maximum brightness to off, a total of 83 clock pulses are needed at the DOZE input.

When either the UP or the DOWN input is active, the DOZE input is disabled.

CAP (Pin 3)

The CAP input is for external component connection for the PLL filter capacitor. A capacitor of 0.047μ F ± 20% should be used at this input.

SYNC (Pin 4).

The AC line frequency (50Hz/60Hz), when applied to this input, synchronizes all internal timings through a phase lock loop. The signal for this input may be obtained from the line voltage by employing the circuit arrangement shown in the application examples.

UP (Pin 5).

This input controls the turn-on and the conduction angle, ϕ , of the TRIG output. A description of this is provided in the DESCRIPTION and TABLE 1. For LS7534, a logic low level is the active level whereas for LS7535 a logic high level is the active level. LS7535 has an internal pull-down resistor of about 500K Ohms on this input.

DOWN (Pin 6).

This input controls the turn-off and the conduction angle, ϕ , of the TRIG output. A description of this is provided in the DESCRIPTION and TABLE 1. For LS7534, a logic low level is the active level, whereas for LS7535 a logic high level is the active level. LS7535 has an internal pull-down resistor of about 500K Ohms on this input.

VDD (Pin 7).

Supply voltage negative terminal.

TRIG (Pin 8).

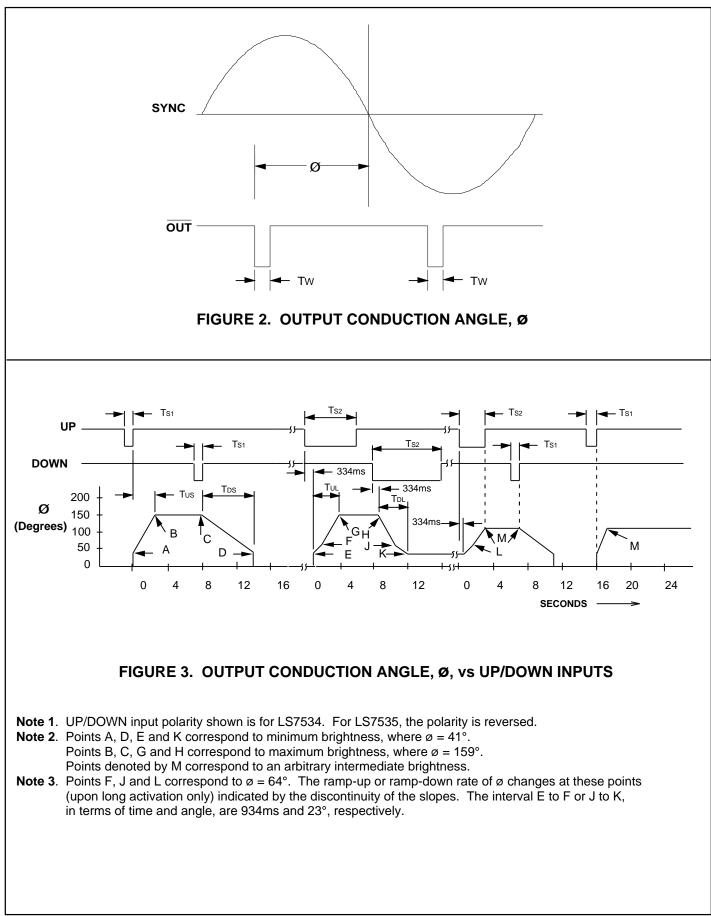
The TRIG output provides a low level pulse occurring every half-cycle of the SYNC signal. The conduction angle, ϕ , of the TRIG output can be varied within the range of 41^o to 159^o by means of either the UP or the DOWN input.

ABSOLUTE MAXIMUM RATINGS:									
PARAMETER DC supply voltage Any input voltage Operating temperature Storage temperature	SYMBOL Vss - Vdd Vin Ta Tstg		VALUE +20 Vss - 20 toVss + 0.5 0 to +80 -65 to +150		UNIT V °C °C °C				
(TA = 25°C, all voltages r									
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS			
Supply voltage Supply current	Vss Iss	+12 -	1.2	+18 1.7	V mA	- Vss = +15V, Output off			
Input Voltages:									
DÖZE LO	VIZL	0	-	Vss - 6	V	-			
DOZE HI	Vizh	Vss - 2	-	Vss	V	-			
SYNC LO	Virl	0	-	Vss - 9.5	V	-			
SYNC HI	Virh	Vss - 5.5	-	Vss	V	-			
UP, DOWN LO	VIOL	0	-	Vss - 8	V	-			
UP, DOWN HI	VIOH	Vss-2	-	Vss	V	-			
Input Current:									
SÝNC, UP, DOWN HI	Ін	-	-	110	uA	With Series 1.5M Resistor to 115 VAC Line			
SYNC, UP, DOWN LO	lı∟	-	-	100	nA	-			
DOZE HI	Ін	-	-	100	nA	-			
DOZE LO	lı∟	-	-	100	nA	-			
	Vон	-	Vss	-	V	-			
TRIG LO	Vol	-	Vss - 8	-	v	Vss = +15V			
TRIG Sink Current	los	50	-	-	mA	VSS = +15V, VSS = +15V, VOL = VSS - 4V			

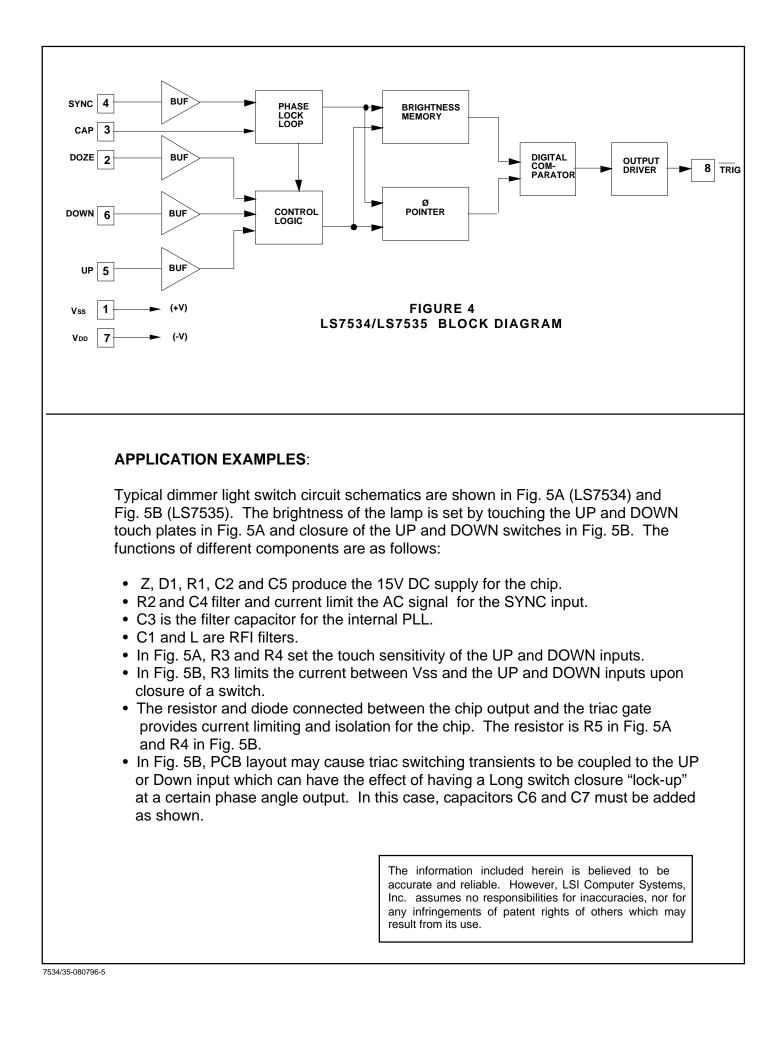
TRANSIENT CHARACTERISTICS (See Fig. 2 and 3) (All timings are based on fs = 60Hz, unless otherwise specified.)

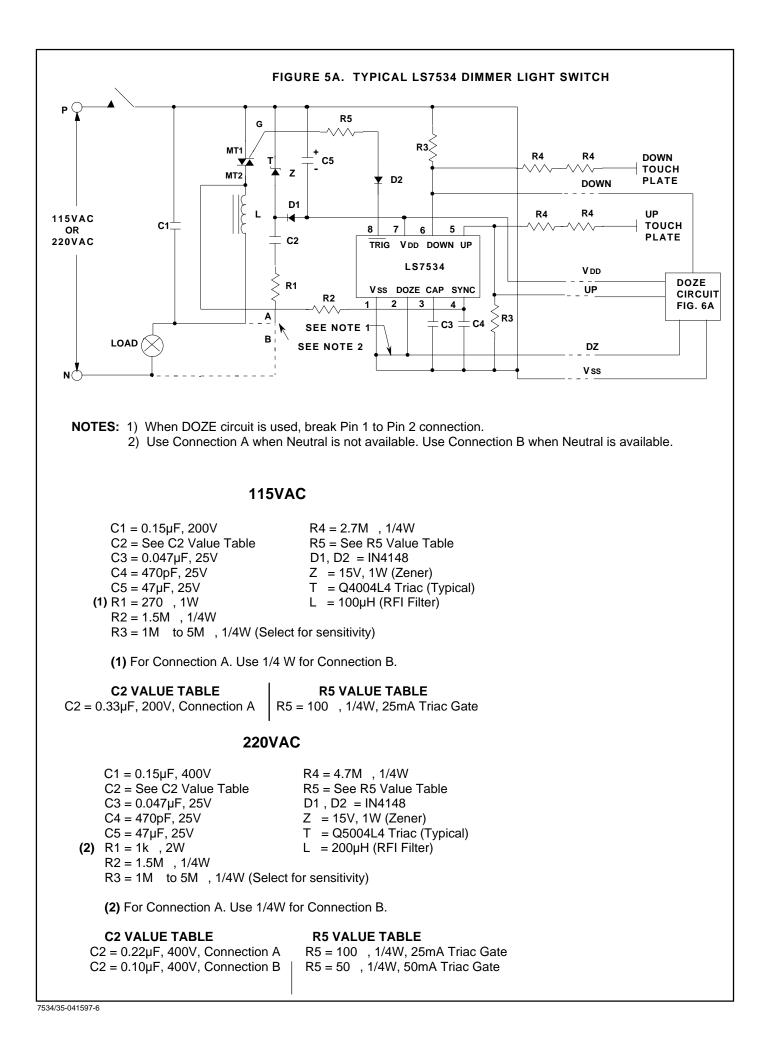
PARAMETER SYNC frequency UP, DOWN duration (SHORT) UP, DOWN duration (LONG)	SYMBOL fs Ts1 Ts2	MIN 40 34 334	TYP - - -	MAX 70 325 infinite	UNIT Hz ms ms
ø ramp time, off to max (UP,SHORT)	Tus	-	2.8	-	sec
ø ramp time, min to max (UP,LONG)	TUL	-	3.6	-	sec
ø ramp time, max to min (DOWN,SHORT)	TDS	-	5.6	-	sec
<pre>ø ramp time, max to min(DOWN,LONG)</pre>	TDL	-	3.6	-	sec
TRIG pulse width	Tw	-	33	-	μs
TRIG conduction angle (See Note)	Ø	41	-	159	degrees
DOZE frequency	fD	0	-	500	Hz

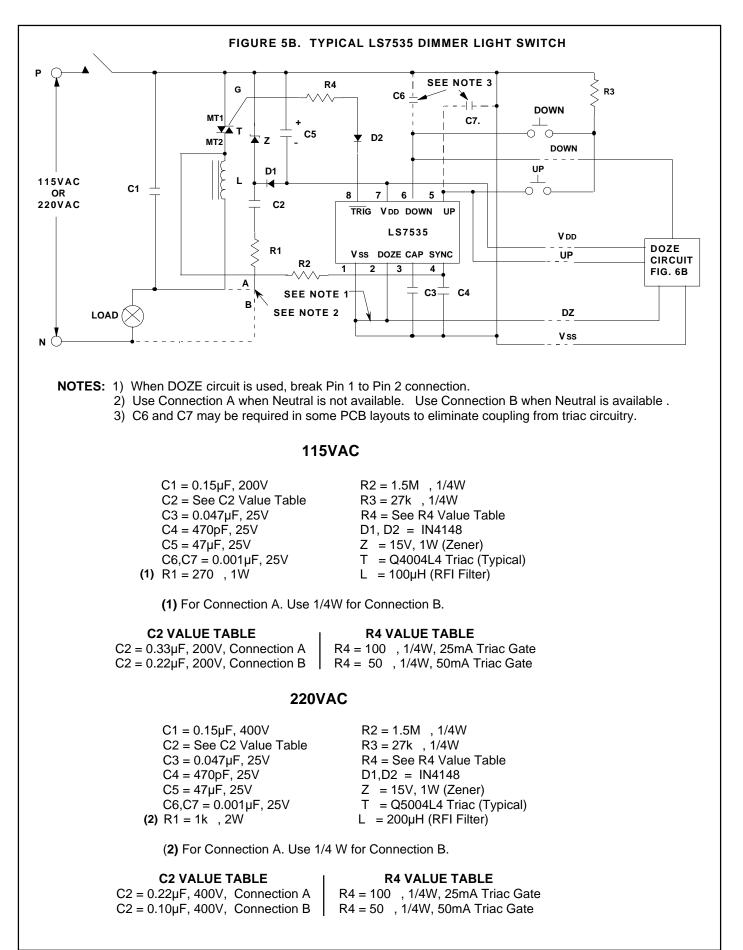
NOTE: The phase delay caused by the typical RC network used between SYNC input and the AC line (See Fig. 5A and Fig. 5B) reduces the effective ø values by 8°.



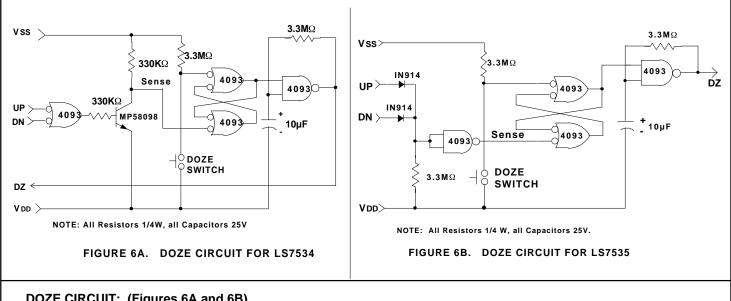
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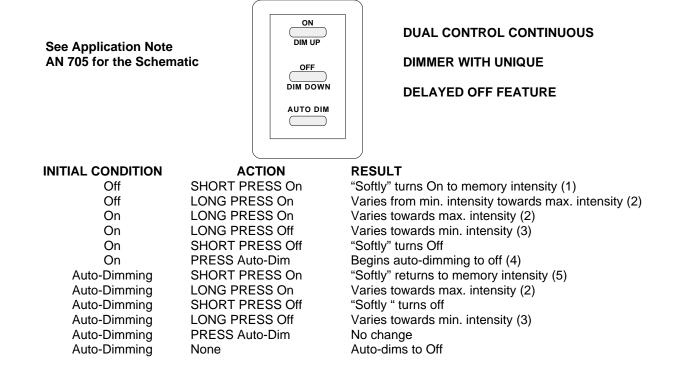
DOZE CIRCUIT: (Figures 6A and 6B)

The Doze circuits shown generate a slow clock (0.04Hz) at the DZ terminal. If the UP/DOWN inputs (Figures 5A and 5B) are not activated, the Sense node of the Doze circuit sits at a logic high level. A momentary pressing of the Doze switch sets the SR flip-flop, enabling the oscillator. Every negative transition of the clock (DZ terminal) causes the lamp brightness to be reduced by equal increments, until eventurally the lamp is shut- off.

When the lamp is off, the oscillator has no further effect on the dimmer circuit. When the lamp is turned on again by activating the UP input, the SR flip-flop is reset and the DZ clock is turned off.

When the Doze circuit is used, the connection between DOZE input (Pin 2) and Vss (Pin 1), as shown in Figures 5A and 5B, should be removed.

FIGURE 7. OPERATING DESCRIPTION OF A FULL-FEATURE LS7535 WALL SWITCH



(1) Last intensity achieved before turn off is stored as memory intensty.

(2) On (Dim Up) varies intensity towards maximum and stops there.

(3) Off (Dim Down) varies intensity towards minimum and stops there.

(4) Auto-dimming period controlled by RC components and intensity level when Auto-Dim is activated.

(5) Last intensity achieved before Auto-Dim started is stored as memory intensity.