APRIL 1997
Revision 1.1

LXT441

Switched 56 / DDS Integrated DSU / CSU

General Description

The LXT441 is an integrated transceiver and data formatter for Switched 56 (SW56) and Digital Data Service (DDS) Data Service Unit/Channel Service Unit (DSU/CSU) and Office Channel Unit (OCU) applications.

The LXT441 line interface section performs transmit pulse shaping and receive signal data and timing recovery at the user-network 4-wire metallic interface. The device operates at loop speeds of 56 kbps and 72 kbps, supporting SW56, 56 kbps DDS with or without secondary channel (SC) and 64 kbps clear channel DDS services.

The integrated DSU circuit provides a DCE interface and connects directly to data terminal equipment (DTE) using standard EIA530 control leads. Data formatting includes DDS framing, control code handling, loop code generation and detection, and zero code suppression processing.

The LXT441 has an on-chip 8-bit microprocessor interface that simplifies device configuration, status reporting, and SW56 call processing, and may be used for parallel data transfer to and from the 4-wire physical link.

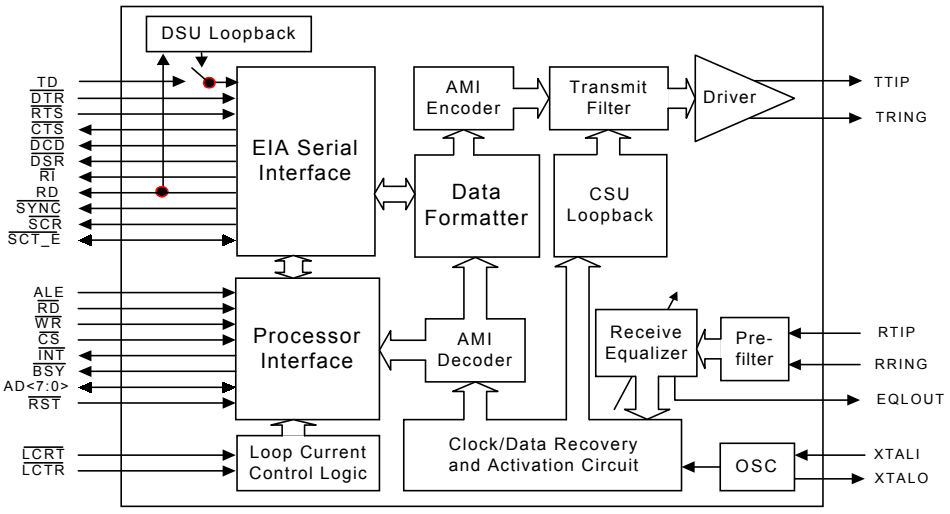
Features

- Supports most popular data rates for new DSU/CSUs
  - Switched 56 and 56 kbps DDS (DDS-PRI, 56 kbps loop speed)
  - 56 kbps DDS with secondary channel (DDS-SC, 72 kbps loop speed)
  - 64 kbps clear-channel DDS (CC-64K, 72 kbps loop speed)
- Switched 56 Call Control via EIA control leads or microprocessor
- Receiver performance monitoring
- Idle Code Transmission (CMI, DMI)
- Transmit timing recovered from network or supplied by system
- Network Control Code Detection and Generation
- CSU and DSU latching and non-latching loopbacks
- Available in 44-pin PLCC
- Single 8.192 MHz crystal or clock input
- 5V only CMOS process technology

Applications

- Leased-line DDS and Switched 56 DSU/CSUs
- Internet Service Provider (ISP) Equipment
- Internal DSU for Routers, Bridges and PC add-in cards
- Frame Relay Access Devices (FRAD)
- OCU Cards for Channel Banks and DLC Systems

LXT441 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT441 Pin Assignments

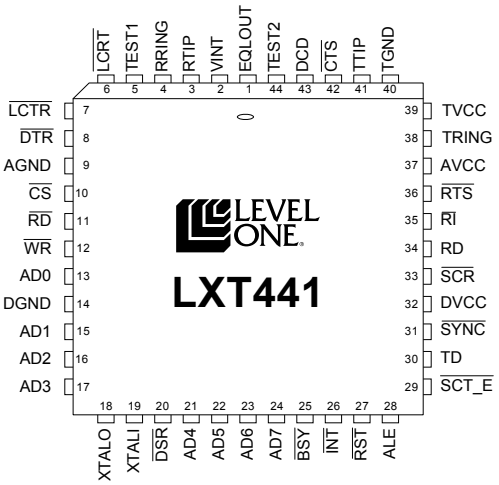


Table 1: LXT441 Microprocessor Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
10	$\overline{CS}$	I	**Chip Select**. Active Low. A Low on this pin enables the 8-bit parallel interface to perform read and write operations.
11	$\overline{RD}$	I	**Read**. Active Low. During read cycles, a Low on this pin turns on the internal drivers to present data to the 8-bit address/data bus.
12	$\overline{WR}$	I	**Write**. Active Low. During write cycles, a Low-to-High transition on this pin latches data present on the 8-bit bus into internal registers.
13 15 16 17 21 22 23 24	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus**. Multiplexed 8-bit parallel address data bus. These pins are used to access the read and write registers located within the LXT441.
25	$\overline{BSY}$	O	**Busy**. Active Low open-drain indication. Signal to host microcontroller that device has not completed read or write operation.
26	$\overline{INT}$	O	**Interrupt**. Active Low open-drain Interrupt. Signal to host microcontroller that an unmasked interrupt condition has been detected.
27	$\overline{RST}$	I	**Reset**. Active Low hardware reset pin. Must be pulsed Low on power-up to initialize all internal circuits. Must also be pulsed Low after changing the data rate setting, and after certain receive line conditions occur.
28	ALE	I	**Address Latch Enable**. When High, internal address latch is transparent. A High-to-Low transition latches the address present on pins AD<7:0>.

Table 2: LXT441 EIA Serial Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
8	$\overline{\text{DTR}}$	I	**Data Terminal Ready**. Active Low EIA signaling lead from DTE.
20	$\overline{\text{DSR}}$	O	**Data Set Ready**. Active Low EIA signaling lead to DTE.
29	$\overline{\text{SCT\_E}}$	I/O	**Extended Transmit Serial Clock**. Input or Output transmit clock dependent upon setting of TCCT control bit.
30	TD	I	**Transmit Data**. Transmit NRZ data from DTE.
31	$\overline{\text{SYNC}}$	O	**Word/Bit Synchronization**. 1-bit wide active Low output indicates word boundaries at DTE interface.
33	$\overline{\text{SCR}}$	O	**Receive Serial Clock**. Smooth 56 kHz for DDS-PRI, gapped 72 kHz (64 kHz) for DDS-SC and CC-64K.
34	RD	O	**Receive Data**. Receive NRZ data to DTE.
35	$\overline{\text{RI}}$	O	**Ring Indicator**. Indicates the presence of receive data (not control codes) when the receiver is in the control sequence mode (CALLMD = 1). Signifies incoming call for SW56 operation.
36	$\overline{\text{RTS}}$	I	**Request to Send**. Indicates a request by the DTE to transmit data. When High, CMI is transmitted on the line in DDS-PRI and DDS-SC. When this line goes High for a time greater than one byte period, the transmitter enters data mode for at least four byte periods.
42	$\overline{\text{CTS}}$	O	**Clear to Send**. Active Low EIA signaling lead indicates DCE readiness to transmit live data.
43	$\overline{\text{DCD}}$	O	**Data Carrier Detect**. Active Low EIA signaling lead indicating that the LIU receiver is fully operational; meaning that it is active, and that frame or bit sync is achieved, if enabled.

Table 3: LXT441 Line Interface Signal Descriptions

Pin	Symbol	I/O	Name / Description
1	EQLOUT	O	**Equalizer Monitor**. Must be left open when not used.
2	VINT	I	**Intermediate Voltage Reference**. Reference voltage used for internal analog circuits. This pin must be connected through a 1 kΩ resistor (Rv) to the center node between the two termination resistors, Rr, as shown in Figure 8.
3 4	RTIP RRING	I I	**Receive Tip and Ring**. Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
6	$\overline{\text{LCRT}}$	I	**Loop Current Rx/Tx**. A Low input, supplied by an external current sensing circuit, indicates the presence of loop current flowing from the receive to the transmit twisted pair wires, and initiates a CSU loopback.
7	$\overline{\text{LCTR}}$	I	**Loop Current Tx/Rx**. A Low input supplied by an external current sensing circuit indicates the presence of loop current flowing from the transmit to the receive twisted pair wires.
38 41	TRING TTIP	O O	**Transmit Ring and Tip**. Differential driver outputs. Designed to drive 135Ω twisted-pair cable through transmit line interface shown in application diagram, Figure 8.

Table 4: LXT441 Miscellaneous Signal Descriptions

Pin	Symbol	I/O	Name / Description
39	TVCC	–	**Transmit Supply.** Line driver power supply.
40	TGND	–	**Transmit Ground.** Line driver ground.
9	AGND	–	**Analog Ground**. Reference for all analog LIU circuits except the transmit driver.
37	AVCC	–	**Analog Supply**. Line interface primary power supply.
18 19	XTALO XTALI	O I	**Crystal Oscillator**. The required 8.192 MHz master clock may be provided by a crystal connected across these pins, or by a digital clock connected to XTALI. If a clock is provided on XTALI, XTALO must be left unconnected.
14	DGND	–	**Digital Ground**. Ground reference for all internal digital circuitry.
32	DVCC	–	**Digital Supply**. Digital circuitry power supply.
5 44	TEST1 TEST2	I I	**Factory Test Pins**. *Leave unconnected.*

FUNCTIONAL DESCRIPTION

The LXT441 is comprised of five basic sections: receiver, transmitter, microprocessor interface, data formatter and back-end system serial interface.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the oscillator circuit to synchronize the recovered clock and data.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing re-synchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135Ω line through a coupling transformer.

The microprocessor block employs an 8-bit multiplexed parallel interface to transfer status and control information to and from the system host controller. This processor port connects to both Intel® multiplexed and Motorola® non-multiplexed controllers with a minimum of external 'glue' logic.

The system serial interface facilitates the connection of a DTE (data terminal equipment) device to the LXT441, which in turn behaves as a DCE (data communication equipment.) The LXT 441 uses 6 standard EIA530 control leads ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and $\overline{\text{RI}}$) for flow control, status reporting and SW56 signaling. The serial interface supports both DSU and OCU operation, with the transmit clock provided by either the recovered receive clock, or an external reference.

Initialization

A hardware reset ($\overline{\text{RST}}$) is required under any of the following circumstances:

- Initial power-up
- A change in Data Rate setting
- A change in the local analog loopback configuration
- A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a "1 for n" redundancy scheme)
- The detection of an invalid line condition by the LXT441 receiver. (This will be indicated by either an XBPV or V_OFL interrupt.)

On receipt of the $\overline{\text{RST}}$ pulse, the LXT441 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. When received data has a 50% ones density, full operation is achieved within one second after $\overline{\text{RST}}$. Under the minimum ones density condition specified in Table 5, full operation is achieved within eight seconds after $\overline{\text{RST}}$. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT441 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RD output is not valid until full operation is achieved.

Table 5: Ones Density Requirements

Data Rate (kbps)	Minimum Average Ones Density
56.0	1/14
72.0	1/18

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT441 reports an LOS (Loss of Signal) condition and performs an automatic re-initialization.

The time required to achieve full operation after reinitialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Reinitialization is not triggered by impulse noise events.

Frame Alignment

When in DDS-SC or CC-64K modes, the LXT441 begins a frame alignment search at channel connection time. Channel connection time is defined as the time when the ACTIVE bit changes to a '1'.

The mean time to Frame Alignment is less than 5 ms. This means that, at 72 kHz on average, fewer than five frame comparisons are required to establish frame alignment.

Frame alignment is declared when the LXT441 detects three consecutive Frame Alignment Word (FAW) sequences matching the FAW. Detection of consecutive FAW sequences requires that each FAW sequence matches the FAW, and that each FAW sequence is exactly one frame apart.

Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the line equalizers which follow. Receive pulses are reconstructed by the receive equalizer, which is comprised of a step equalizer stage and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and time varying line characteristics such as temperature, humidity and age.

Clock Recovery

The clock recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the oscillator input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate $\overline{SCR}$ and all other required clocks (except $\overline{SCT\_E}$ when it is supplied as an external input).

Data Extraction

The data extraction block delivers raw recovered bipolar line data to the data formatter and decoder so that it may output the NRZ RD stream to the EIA interface and the receive EIA microprocessor register. A positive or negative differential pulse received between RTIP and RRING results in a logic 1 sent to the formatter, while no pulse is reported to the formatter as a logic 0. After decoding in the formatter section, the final RD output at the received data rate is valid on the falling edge of $\overline{SCR}$.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 5 are met, and the receive line signal contains at least one valid pulse every 26 bit periods. Loss of signal is declared after 32 consecutive zeros. However, the $\overline{SCR}$ output remains synchronized to the RTIP/RRING input for up to 40 consecutive zeros, after which re-initialization occurs. Spurious bipolar violations (due to channel noise, etc.), will not adversely affect long term LXT441 data reception.

Receiver Bipolar to NRZ Conversion

The receiver converts Bipolar data into NRZ data in the following manner:

- Bipolar B's are marks (of alternate polarity with respect to last mark) converted to NRZ 1s.
- Bipolar V's are marks (of same polarity with respect to last mark) converted to NRZ 1s.
- Bipolar O's are spaces converted to NRZ 0s.

This conversion process takes 1 byte plus 1 bit period, with corresponding NRZ data available 8 bit periods after the Bipolar data is received. There are, however, a few exceptions to this. Reception of the DSU Loopback control code and reception of the Zero Suppression control code require that a code replacement be performed upon the received data prior to conversion to NRZ format. See Table 28 for RX_DLP & RX_ZSC code replacement.

In DDS-SC mode, there are no violations. Thus, the receiver only converts O's and B's (bipolar data) to NRZ 0s or 1s respectively. Frame synchronization must be established to enable network code detection. Reception of the DSU Loopback code requires a code replacement operation to be performed prior to conversion to NRZ format. See Table 28 for R_DLP code replacement.

CC-64K mode is very much the same as DDS-SC mode. There are no byte replacements, and the only code is idle data (RX_DMI). See Table 28 for control codes & replacement policy for various modes.

Receiver Code Detection

The receiver converts bipolar received data into NRZ data. In DDS-PRI mode, this process requires bipolar violation (BPV) detection, valid/invalid BPV detection, and control code detection. A violation is detected upon receipt of Bipolar data which violates the Alternate Mark Inversion (AMI) Rule. A BPV is valid if, and only if, it belongs to a 7-bit Control Code, satisfying the following set of criteria:

- At least seven bit periods have passed without a violation since receipt of the violation in question.
- An odd number of B's (non-violation marks) were received since the last violation.
- The bit received prior to the violation was an O (a space).

Control Code Detection

The data presented at the RTIP/RRING pins undergoes bipolar to NRZ conversion, with automatic detection and decoding of control codes according to the following criteria:

- Detection of Idle (CMI), OOS, and OOF codes in DDS-PRI mode.
- Detection and conversion of DSU Loop code in DDS-PRI mode, and DSU Loop control code in DDS-SC mode.
- Detection of DDS-SC control codes for DDS-SC mode.
- Detection of the DDS-SC six-bit frame pattern for byte alignment of data and control streams for DDS-SC mode, and 8-bit data for CC-64K mode.
- Control of EIA handshake signals based on receiver status from the line interface unit.

All control codes except RX_DMI are encoded into valid BPVs. Thus, upon receipt of a valid BPV, control codes are decoded (as listed in Table 28). Any valid BPV which doesn't match a control code listed in the table results in an 'unmatched' code. The exception, RX_DMI, is detected when an all-marks (all B's and no V's) code is received. All control codes remain active for 7 bit periods after detection.

Bipolar received codes in both DDS-SC and CC-64K modes contain no violations. Therefore, data must be synchronized with the frame pattern, to establish the beginning of each word. The C/S bit is used to determine whether the unit is receiving network codes or data. When two of three consecutive C-bits are 0s the network code detector is enabled which tests if the data matches any of the control codes listed in Table 27. When two of three consecutive C-bits are 1s the unit reverts to data mode.

Loss of Frame Alignment

The LXT441 declares loss of frame alignment when it receives five consecutive Frame Alignment Word (FAW) sequences in error. Here, consecutive FAW sequences implies that each FAW sequence is expected to occur an integral number of frames after the FAW sequence which produced alignment. The initial alignment algorithm is the same as the frame recovery algorithm.

Recovery of Frame Alignment

The LXT441 begins recovery of frame alignment immediately after detecting loss of frame alignment. Frame Alignment Recovery is identical to the initial Frame Alignment search process described under Initialization.

Changes in Received Signal Strength

During initialization, the LXT441 selects filters appropriate to the strength of the received signal. After initialization, the LXT441 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulse noise events or by slow changes in signal amplitude caused by normal temperature and humidity variations (The maximum constant rate of change which the LXT441 can track is 6 dB per minute.) However, instantaneous “step” changes (see Figure 2) may temporarily interfere with data reception. Step changes may be caused by sudden changes in loop attenuation, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 3.

Under Condition 1, the LXT441 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT441 responds to significant step changes by re-initializing.

Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory when working with artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs). Excessive BPVs which are not valid code words are detected and counted by the LXT441. The XBPV interrupt flag will be set when excessive BPVs are detected by the LXT441 receiver. The device should be reinitialized via the application of a valid $\overline{\text{RST}}$ pulse in the presence of excessive BPVs.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT441 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of different length. These changes trigger the RLOS report and automatic re-initialization.

Receive Loss of Signal

Receive loss of signal (RLOS) is detected when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT441 automatically re-initializes when RLOS is present, and 40 consecutive zeros are counted. Figure 4 shows the RTIP/RRING input and RLOS control bit timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT441 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain active for a period of time (0.13 s < tH < 16 s) after signal energy reappears.

Figure 5 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go High for a time 0.26 s < tP < 16 s.

Figure 2: Step Changes in Receive Signal Strength = 20 $\log_{10}$ ($^{A2}/_{A1}$) dB

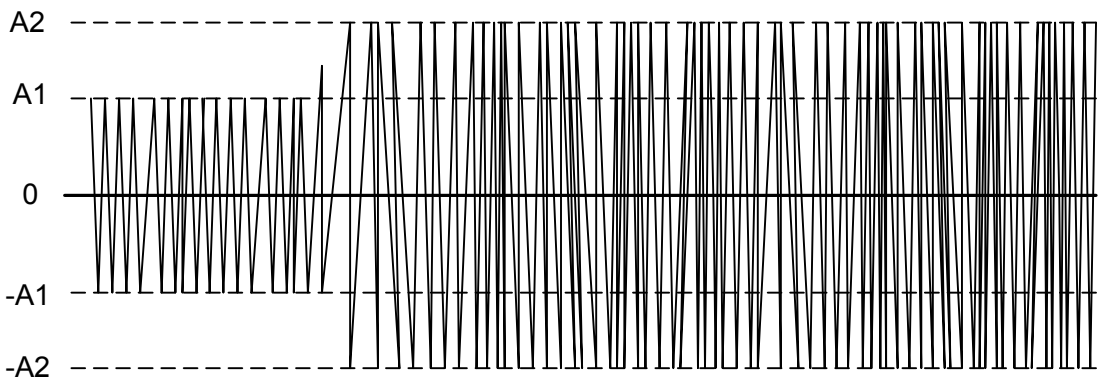
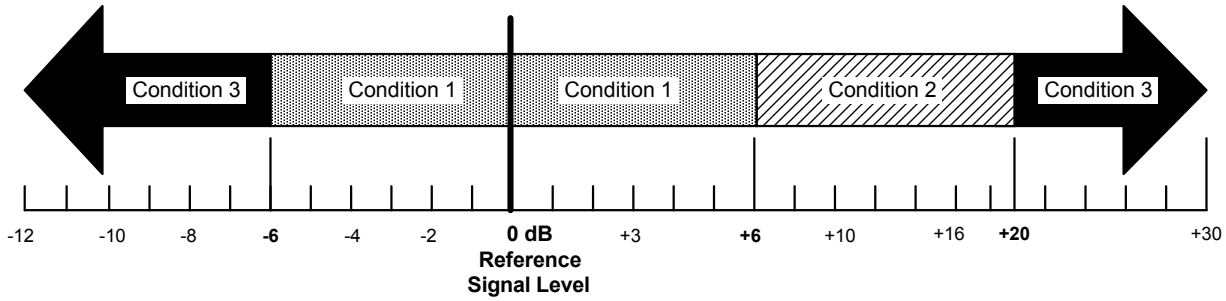


Figure 3: Conditions Based on Changes in Receive Signal Strength



Condition 3:
Increase > 20 dB or
Decrease > 6 dB

Automatic re-initialization. No action required. If the condition is due to a signal strength decrease, the LXT441 also reports RLOS.

Condition 1:
Increase 0 - 6 dB or
Decrease 0 - 6 dB

Automatic compensation (may re-initialize). May pass erroneous data temporarily before resuming error-free operation. No action required.

Condition 2:
Increase 6 - 20 dB

Re-initialization not guaranteed. The device may continue to pass erroneous data until reset. RESET pulse required to ensure accurate data reception.

Figure 4: RLOS Timing for a True Loss of Signal

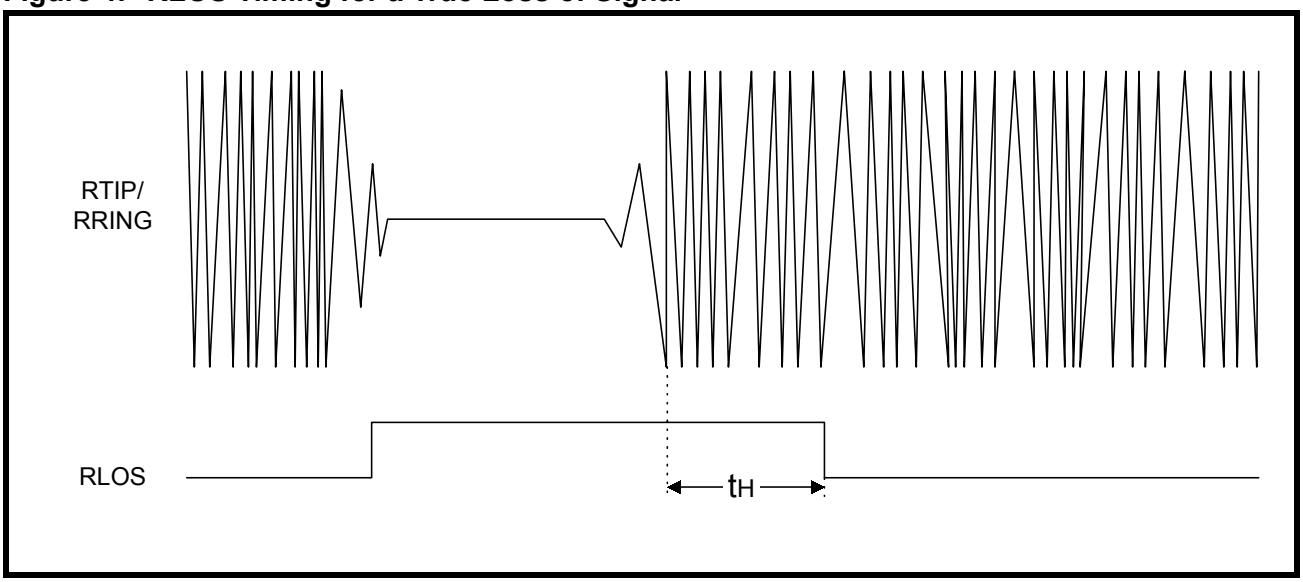
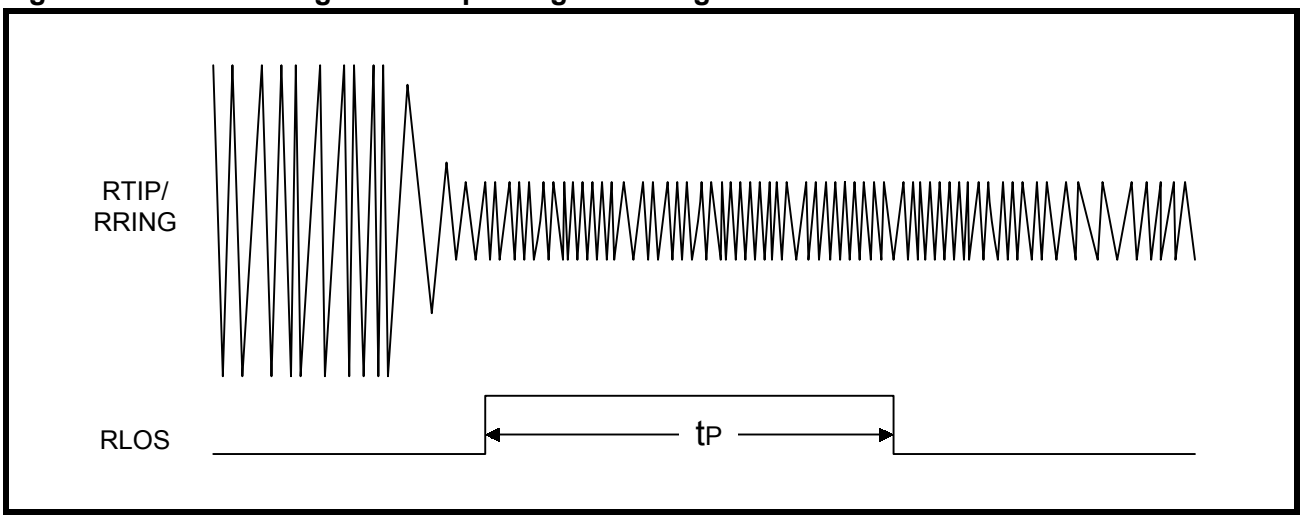


Figure 5: RLOS Timing for a Drop in Signal Strength > 6 dB



Transmission

Transmit data (TD) from the DTE is sampled on the rising edge of $\overline{SCT\_E}$. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the $\overline{SCT\_E}$ input/output clock. In DSU applications with TCCT=0, $\overline{SCR}$ is typically routed back out of the $\overline{SCT\_E}$ input/output pin to serve as a transmit demand clock. If EIAREG=1, then data at the serial interface is ignored, and the Transmit EIA 8-bit microprocessor register is used as the source of transmit data.

Once the transmit data is sampled and encoded, resulting AMI output pulses are processed through a set of frequency dependent filters. Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by control bits MODE0 and MODE1.) A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The resulting transmit pulses are then applied to the line driver for transmission onto the twisted-pair line.

Transmit Serial Interface

User data presented at the TD pin undergoes NRZ to bipolar conversion, with automatic generation of zero suppression code for DDS-PRI. In DDS-PRI mode, controlled generation of Control Mode Idle (CMI), and Data Mode Idle (DMI) may be accomplished by manipulating the $\overline{DTR}$/$\overline{RTS}$ control leads, or by writing to the TX_CMI or TX_DMI control bits. The microprocessor control bits take precedence over the $\overline{DTR}$/$\overline{RTS}$ for commanding CMI/DMI transmission.

In DDS-SC and CC-64K modes, controlled generation of the DDS-SC control codes may be selected, and the six-bit frame pattern is automatically inserted into the transmitted data stream.

Transmit timing is derived from the receive clock for a loop timed DSU/CSU, or from the $\overline{SCT\_E}$ input for tail-circuit loop timing, or in OCU applications.

Transmit NRZ to Bipolar Conversion

The Transmitter converts NRZ data and control codes into bipolar transmitted data. It is possible that several control codes are requested for transmission, thus a priority encoder must resolve which code should be transmitted; if no control code is requested, the transmitter sends out converted NRZ data (see Table 28 for priority of transmit control codes). The position of injected code words is set arbitrarily by a free-running internal bit counter. In DSU operation without a 'tail-circuit' (TCCT=0), the transmit word position is aligned to the receive word position. In DDS-SC and CC-64K modes, the receive word position is determined by the receive frame pattern, while in DDS-PRI mode, the receive word position is arbitrary.

In DDS-PRI MODE, code injection must take into account the polarity of the last transmitted mark (B or V), and whether an even or odd number of B's have been sent since the last V. The first criterion is used to assure that violations are transmitted correctly. The second criterion assures that any X's will be transmitted correctly - as O or B to maintain an odd number of B's since the last V.

In DDS-SC and CC-64K modes, code injection is accompanied by the injection of a frame pattern as the 8th bit of every outgoing data byte or code word. When no code is requested, the transmitter simply converts NRZ 0s and 1s into Bipolar O's and B's, respectively, and injects the frame bit at the proper location. See Table 28 for control codes in DDS-SC and CC-64K modes.

Transmit Code Generation

CONTROL-MODE-IDLE (CMI) can be generated from a logic-Low on EIA handshake signal $\overline{RTS}$ in DDS-PRI mode and DDS-SC mode.

Clear-To-Send ($\overline{CTS}$) goes High after receiving a Request-To-Send ($\overline{RTS}$) with delay based upon the time required to transmit the last complete CMI code, plus three idle data bytes.

DSU Loopback Code Generation in an OCU Application

If the TX_DLP control is set (register WR2-bit 6), then the controls which normally force transmission of CMI will now force transmission of DSU Loopback Code (DLP). The user can inject test data by pulling $\overline{RTS}$ High, and waiting for $\overline{CTS}$ High; indicating the end of a DLP byte and the start of a test data byte. In this case, the $\overline{RTS}$-to-$\overline{CTS}$ delay is not three to four bytes, but is less than one byte.

Loopback Operation

The LXT441 incorporates both a CSU loopback and a DSU loopback.

CSU Loopback

When the $\overline{\text{LCRT}}$ pin is set Low, a CSU loopback is engaged, with the recovered line data and clock being sent back through the transmit section and onto the line interface, as well as being output on the RD and $\overline{\text{SCR}}$ pins. TD and $\overline{\text{SCT\_E}}$ inputs are ignored in the loopback mode.

DSU Nonlatching Loopback

A nonlatching loopback operates upon receipt of a minimum of four consecutive bytes of the specified loopback code at the proper data rate, and continues for a minimum of four consecutive bytes after receipt of the last loopback code. The loopback is terminated upon receipt of five successive byte intervals without the loopback code (refer to Table 28 for the DSU-Loopback codes for all data rates). The four consecutive bytes must be contiguous; having no "filler" bits between DLP code bytes. In DDS-PRI operation, a loopback code byte is a 7-bit word, and in DDS-SC and CC-64K operation, a loopback code byte is an 8-bit word, with a ninth framing bit injected between the 7th and 8th bits of the code word.

System Serial Interface and Data Formatting

The LXT441 provides a EIA DCE serial interface with TD, RD, $\overline{\text{SCT}}$/$\overline{\text{SCT\_E}}$, $\overline{\text{SCR}}$, $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, $\overline{\text{RI}}$, & $\overline{\text{CTS}}$ pins for attaching data terminal equipment (DTE). The signal levels are TTL/CMOS compatible, allowing a direct connection to Serial Communication Controllers (SCC), while connection to external terminals require standard V.35/RS449 transceivers. User data for transmission undergoes processing in the data formatter to insert required zero suppression codes for DDS-PRI, and framing information for DDS-SC and CC-64K. Receive line data has zero suppression codes removed from DDS-PRI streams, while the framing bits are stripped from DDS-SC and CC-64K data. Secondary channel bits are passed to the RD and TD pins in DDS-SC, allowing transparent secondary channel processing. Refer to Figures 6 and 7 for EIA interface data structure and relative timing. For specific timing parameters, refer to Test Specifications.

Device Configuration

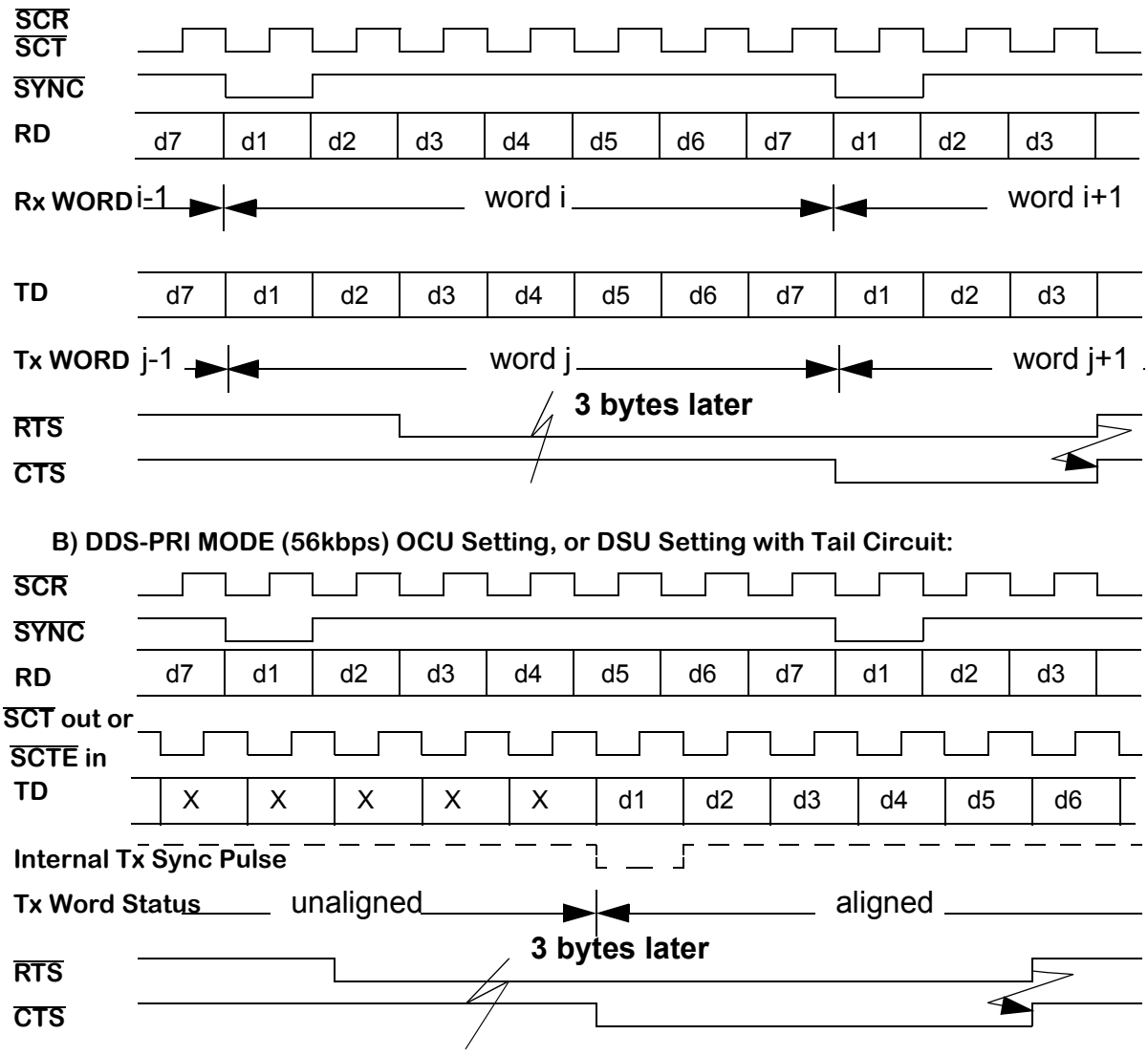
The user can select the operating mode and loop rate (DDS-PRI, DDS-SC, CC-64K) by writing the appropriate values to control bits MODE0 and MODE1.

Transmit timing modes are selected by configuring bits OCU and TCCT. Switched 56 call flow control is performed using either the EIA handshake lines or the microprocessor port. In DDS-SC mode, the secondary channel bandwidth is available transparently by interpreting transmit and receive data in relation to the $\overline{\text{SYNC}}$ signal.

Switched 56 Call Control

Switched 56 call control is performed between OCU and DSU by the interpretation of CMI and DMI codes sent from one end-point to the other. These codes correspond to ‘on-hook’ and off-hook’ conditions on the metallic trunk. Refer to the TIA/EIA-596 specification for specific signalling and timing requirements. The DSU ‘dials’ a call by seizing the trunk, waiting for a valid network ‘wink’ and then sending alternating CMI/DMI sequences which are interpreted as dial digits, much in the manner of pulse dialing. The DSU ‘answers’ a call by detecting non-CMI data from the OCU. CMI/DMI detection is performed by the LXT441 and may be monitored via the host controller. CMI/DMI transmission may be accomplished using either the $\overline{\text{RTS}}$ signal or the TXCODE register.

Figure 6: EIA Interface Data Structure & Timing - DDS-PRI Mode



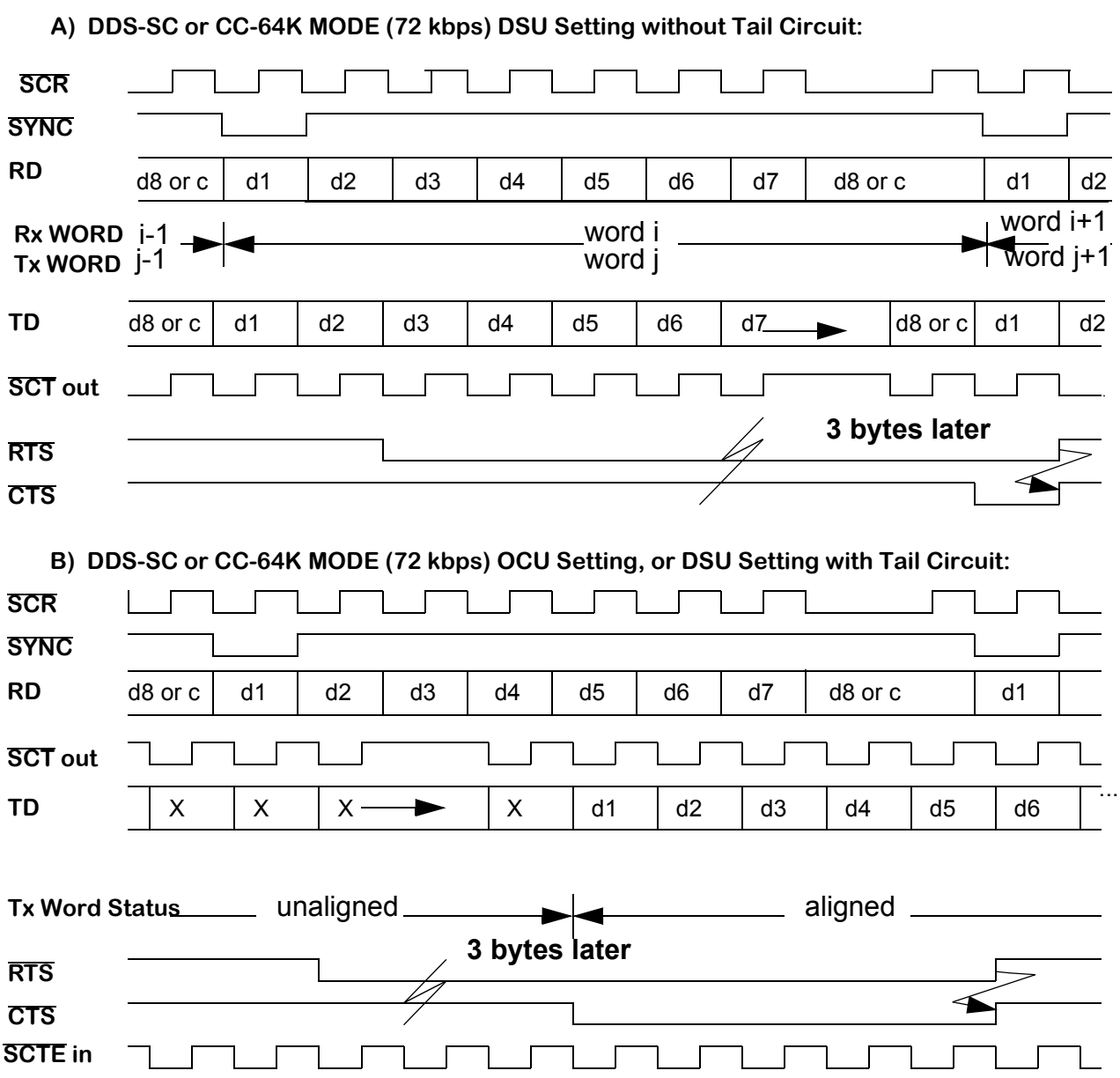
NOTES:

In DDS-PRI Mode when OCU= 0 and TCCT = 0, $\overline{SCR}$ and $\overline{SCT\_E}$ are output clocks with identical bit phase. The $\overline{SYNC}$ pulse indicates both the Transmit and Receive word positions. When $\overline{RTS}$ is pulled Low, $\overline{CTS}$ will go Low at the beginning of the fourth following transmit word position.

In DDS-PRI Mode when OCU = 1 and TCCT = 0, $\overline{SCR}$ and $\overline{SCT\_E}$ are output clocks having arbitrary relative phase. The transmit word alignment may be detected by the DTE by asserting $\overline{RTS}$ and observing the transmit bit period in which CTS goes Low.

In DDS-PRI Mode when TCCT = 1, $\overline{SCR}$ is an output, and $\overline{SCT\_E}$ is the transmit serial clock input with arbitrary phase position. Again, the DTE may detect the transmit word position by using the $\overline{RTS}$ and $\overline{CTS}$ lines.

Figure 7: EIA Interface Data Structure & Timing - DDS-SC or CC-64K Mode



NOTES:

In DDS-SC or CC-64K Modes the serial clock outputs $\overline{SCR}$ and $\overline{SCT}$ are each "gapped" 72 kHz clocks with an aggregate rate of 64 kHz. The single-period "gap" occurs during the 'd7' bit position.

In configurations with TCCT=1, the $\overline{SCTE}$ input must be a 72 kHz. 'smooth' (ungapped) clock, and the transmit word position is determined using $\overline{RTS}$ and $\overline{CTS}$.

APPLICATION INFORMATION

Design Considerations

Figure 8 shows a typical LXT441 application circuit. A DSU crystal (8.192 MHz) is connected across XTALI and XTALO, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The Rs/Cs shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the Rr/Rin network. Rv limits current into the low-impedance VINT driver during over-voltage conditions on the line.

The DTE is connected to the LXT441 EIA interface. NRZ data is required at TD and RD, so level conversion is required for standard bipolar signals such as V.35 and RS-232. Device configuration pins may be tied to Vcc or GND, or may be supplied with logic inputs from an external control circuit. Figure 9 provides details of typical protection and current sensing circuits. Table 6 lists external component recommendations. Refer to the following documents for DDS electrical specifications:

- ANSI T1.410 - 1992
- AT&T TR 62310 - 1993

Microprocessor Interfacing

The microprocessor interface is an 8-bit parallel port with multiplexed address/data pins and associated bus control signals. Interfacing to Motorola, Intel and Zilog controllers may be accomplished with a minimum of glue logic by following the guidelines below, and observing the timing parameters in Figures 11 and 12.

$\overline{CS}$ does not have to be asserted before ALE transitions Low, latching the address present on the multiplexed address/data bus.

The $\overline{INT}$ signal is cleared to inactive High following a read of the Interrupt Status register at address 08h.

BSY Operation

$\overline{BSY}$ indicates stable data available for read on $\overline{RD}$ cycles, and the proper internal latching of data on write cycles. Consecutive write cycles require that $\overline{BSY}$ goes inactive High before the next write. $\overline{BSY}$ may be used to 'stretch' the RD strobe. RD should not go High before $\overline{BSY}$ goes inactive High.

Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT441, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 8.) These inputs, pins 3 and 4, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT441 will switch to the highest gain filter, which produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report.

Layout considerations for LXT441 application circuits include:

- Minimum PCB trace lengths between the LXT441 and the 8.192 MHz crystal and loading capacitors.
- Minimum PCB trace lengths between resistors Rin and the RTIP and RRING pins. Shield these connections with ground traces.
- Minimum PCB trace lengths between the receive transformer and the receive termination network.

Even with good PCB layout practices, RLOS reporting can be unreliable if the twisted pair line cable is not connected to the OCU or CSU/DSU. The unterminated receive lines can pick up enough noise to trip the data detectors and cause an inaccurate RLOS reading. However, equipment designers can safely assume that the highest-gain filter with 50 dB of signal amplification will never be selected for normal operation on lines with up to 45 dB of attenuation at the Nyquist frequency.

The 50 dB filters were designed for applications in which the line attenuation is 48 dB or greater. The DDS specification requires an insertion loss at 56 and 72 kbps of 43 dB or less. The LXT441 incorporates built-in headroom up to 45 dB. So, for standard applications, the highest-gain filter will never be selected.

Power Supply Decoupling

Each +5V input should be tied to the same power plane, and each should be bypassed by a 0.47 µF decoupling capacitor. The bypass caps should be located as closely as possible to the device power and ground pins.

Figure 8: Typical LXT441 Application

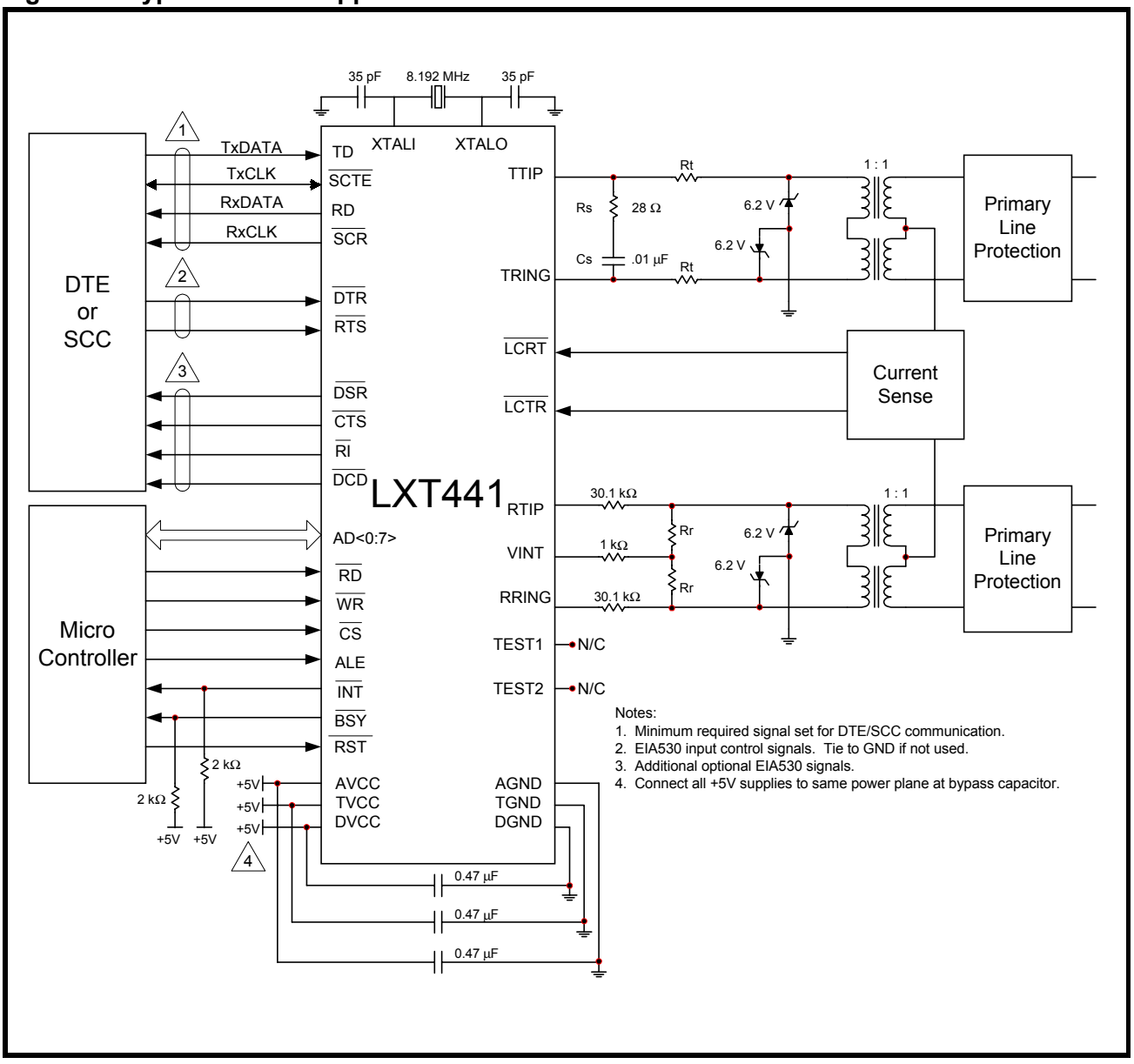
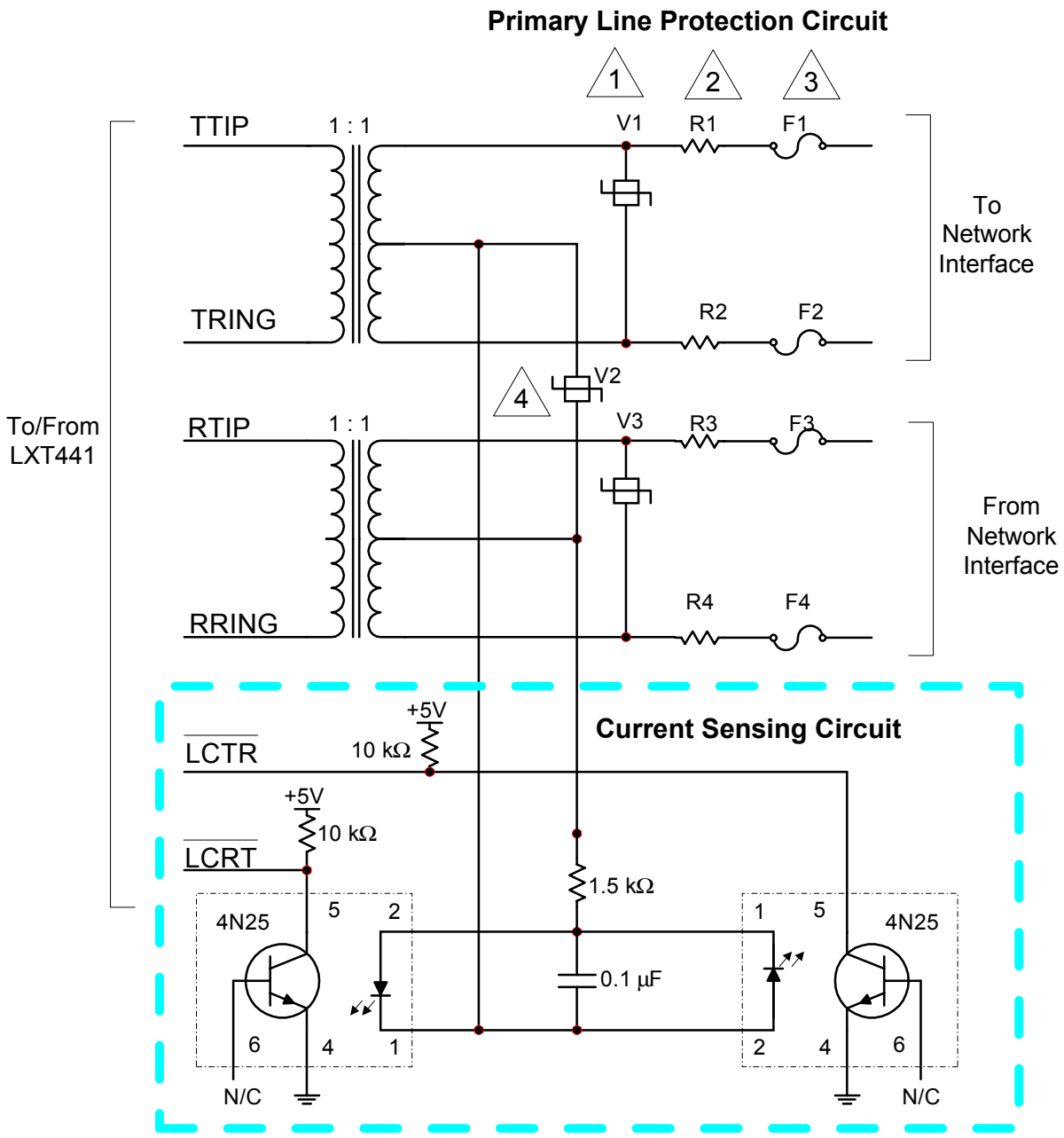


Figure 9: Typical Primary Line Protection and Current Sensing Circuits



Notes:

1. V1, V3 provide secondary overvoltage protection. Turn on above ≈ 3V
2. R1 - R4 are current limiting resistors. One per Rx/Tx pair is sufficient. Two per pair provide impedance symmetry.
3. F1 - F4 provide series current protection. One per Rx/Tx pair is sufficient. Two per pair provide impedance symmetry.
4. V2 provides pair-to-pair overvoltage protection. Turn on above ≈ 30V.

Table 6: External Component Recommendations

Component	Parameter	Recommended Value	
		LXT400 Compatible	LXT441 Only
Line Transformer Suggested Manufacturers: Midcom (800) 643-2661 B and H (612) 894-9590 Vitec (209) 651-1535	Turns ratio	1:1, ± 1%	1:1, ± 1%
	Structure	Center tapped (for line side)	Center tapped (for line side)
	Primary Inductance	200 mH minimum	40 mH minimum
	Leakage Inductance	22 to 43 µH maximum	43 µH maximum
	DC Resistance (Primary, Rwp)	7 - 17 Ω	8 Ω maximum (6Ω ± 10% preferred)
	DC Resistance (Secondary, Rws)	7 - 17 Ω	8 Ω maximum (6Ω ± 10% preferred)
	Interwinding Capacitance	350 pF maximum	80 pF maximum
Rin	Resistance, Tolerance, Rating	30.1 kΩ, ± 1 %, ¼ W	
Rt, **Rr**	Resistance Calculation, Tolerance, Rating	(135 Ω - Rwp - Rws)/2, ± 1%, ¼ W [1]	
Rv	Resistance, Tolerance, Rating	1 kΩ, ± 5%, ¼ W	
DSU Crystal	Nominal frequency	8.192 MHz	
	Holder style	HC-49/U	
	Operating Mode	Fundamental, parallel resonant	
	Cut	AT	
	Load Capacitance	22 pF nominal (excluding crystal C0)	
	Tolerance	± 35 ppm @ 25 °C	
	Range	± 50 ppm, -40 to +85 °C	
	Aging	3 ppm per year maximum	
	Maximum ESR	100 Ω	
	Drive Level	1 mW maximum	
DSU Crystal Loading Capacitors	Capacitance, Tolerance, Rating	35 pF, ± 5 %, 10 V	
	Construction	NPO ceramic or equivalent	
Transmit Shunt Network			
Rs	Resistance, Tolerance, Rating	28 Ω, ± 5 %, ¼ W	
Cs	Capacitance, Tolerance, Rating	0.01 µF, ± 20 %, 10 V	

1. Rwp = Primary winding resistance + resistance of series current limiting resistors and series protection devices.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 7 through 11 and Figures 10 through 12 represent the performance specifications of the LXT441 and are guaranteed by test, except where noted by design

Table 7: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage	AVCC referenced to AGND	V_{CC}	-0.3	6	V
	DVCC referenced to DGND	V_{CC}	-0.3	6	V
	TVCC referenced to TGND	V_{CC}	-0.3	6	V
Supply Variation	AVCC referenced to DVCC	V_{CCV}	-0.3	0.3	V
	DVCC referenced to TVCC	V_{CCV}	-0.3	0.3	V
	AVCC referenced to TVCC	V_{CCV}	-0.3	0.3	V
Ground Variation	AGND referenced to DGND	G_{NDV}	-0.3	0.3	V
	DGND referenced to TGND	G_{NDV}	-0.3	0.3	V
	AGND referenced to TGND	G_{NDV}	-0.3	0.3	V
Input voltage, any pin[1, 2]		-	AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin[2]		-	-	±20	mA
Continuous output current, any pin[2]		-	-	±25	mA
Continuous current, any VCC or GND pin		-	-	±50	mA
Storage Temperature		T_{ST}	-50	150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TTIP and TRING are referenced to DVCC and DGND.
2. Except supply pins.

Table 8: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended Supply Voltage TV_{CC}, AV_{CC}, DV_{CC}	V_{CC}	4.75	5.0	5.25	V
Recommended Operating Temperature	T_{OP}	-40	-	85	°C

Table 9: Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Supply Current	I_{CC}	-	60	80	mA	V_{CC} = 5.0 V
Input Low Voltage [2]	V_{IL}	-	-	0.8	V	Digital Inputs
Input High Voltage [2]	V_{IH}	2.0	-	-	V	Digital Inputs
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL}= 1.6 mA (TTL)
	V_{OL}	-	0.2	-	V	I_{OL}< 10µA (CMOS)
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH}= 400µA (TTL)
	V_{OH}	-	4.5	-	V	I_{OL} < 10µA (CMOS)
Input Leakage Current	I_{IL}	-40	-	40	µA	0 < V_{IN} < V_{CC}
Open Drain Leakage Current [3]	I_{ODL}	-	-	10	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.
3. Applies to $\overline{INT}$ and $\overline{BSY}$ only.

Table 10: AC Timing Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive Timing (Figure 10)	$\overline{SCR}$ period - out of lock	T_{PR} (ol)	$1-5x10^{-3}$ / $\overline{fb(rec)}$	1 / $\overline{fb(rec)}$	$1+5x10^{-3}$ / $\overline{fb(rec)}$	µs	no Rx input at RTIP/RRING
	$\overline{SCR}$ period - in lock	T_{PR} (il)	-	1 / fb(rec)	-	µs	Rx input present at RTIP/ RRING
	$\overline{SCR}$ pulse width High	T_{RCH}	$T_{PR}/2$ - 200	T_{PR} / 2	$T_{PR}/2$ + 200	ns	
	Rx signal input at RTIP/ RRING frequency tolerance	RX_{TOL}	-50	0	+50	ppm	
	RD delay from $\overline{SCR}$ falling edge	T_{RDD}	-500	-	500	ns	into 20 pF load
	Transition time on any digital output	T_{TO}	-	-	20	ns	into 20 pF load
Transmit Timing (Figure 10)	$\overline{SCT\_E}$ period	T_{PT}	-100ppm	1/Data Rate	+100ppm	µs	
	$\overline{SCT\_E}$ input pulse width High	T_{TWHI}	3	1 / $\overline{2fb(tx)}$	10	µs	
	$\overline{SCT\_E}$ output pulse width High	T_{TWHO}	1/2fb(tx) -200	1 / $\overline{2fb(tx)}$	1/2fb(tx) + 200	µs	
	TD setup to $\overline{SCT\_E}$ rising edge	T_{TSU}	700	-	-	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. fb (rec) = Frequency of incoming recovered datastream.
3. fb(tx) = Frequency of transmit bitrate clock on $\overline{SCT\_E}$ input.

Table 10: AC Timing Characteristics (Over Recommended Range) – continued

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit Timing (Figure 10)	TD hold time after $\overline{\text{SCT\_E}}$ rising edge	TTH	700	-	-	ns	
	Transition time on any digital input	TTI			40	ns	
	$\overline{\text{SCT\_E}}$ input frequency tolerance (with respect to fb(tx)	TXTOL	-100	0	+100	ppm	
Crystal Tolerances	XTALI input frequency	FXTAL	–	8.192	–	MHz	
	XTALI frequency tolerance	FMTOL	-100	0	+100	ppm	
Reset Timing	$\overline{\text{RST}}$ pulse width Low	TRWL	1000	-	-	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. fb (rec) = Frequency of incoming recovered datastream.
3. fb(tx) = Frequency of transmit bitrate clock on $\overline{\text{SCT\_E}}$ input.

Figure 10: EIA Timing

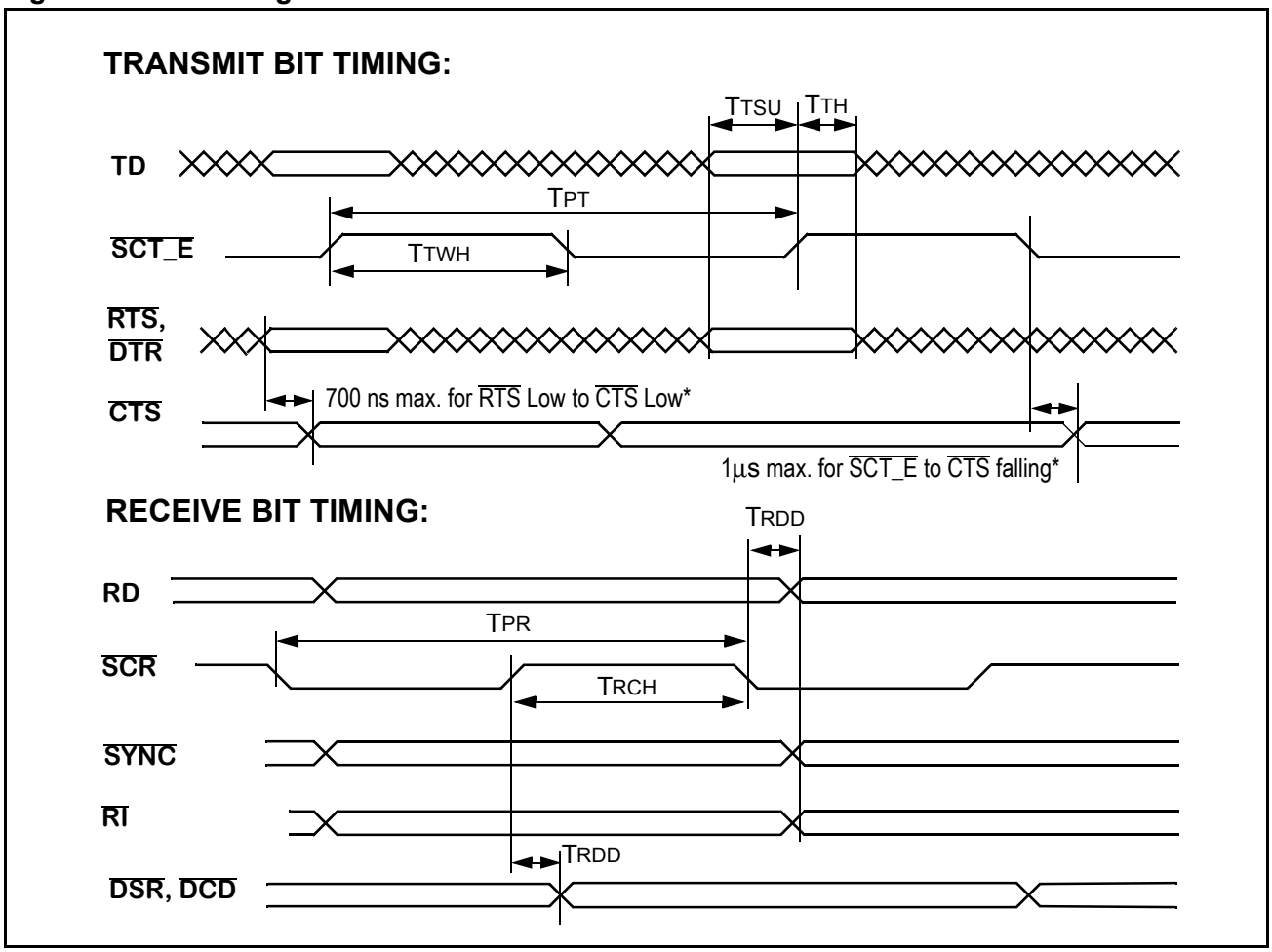


Table 11: Microprocessor Timing Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
$\overline{CS}$ setup to $\overline{RD}$ or $\overline{WR}$ falling edge	TCSU	15	-	-	ns	CLOAD = 20 pF
$\overline{CS}$ hold from $\overline{RD}$ or $\overline{WR}$ rising edge	TCHR TCHW	15	-	-	ns	CLOAD = 20 pF
ALE pulse width High	TALPW	35	-	-	ns	CLOAD = 100 pF
$\overline{RD}$ or $\overline{WR}$ hold from ALE rising edge	TRWH	10	-	-	ns	CLOAD = 100 pF
ALE hold from $\overline{RD}$ or $\overline{WR}$ rising edge	TALH	15	-	-	ns	CLOAD = 100 pF
ADDR setup to ALE falling edge	TASU	15	-	-	ns	CLOAD = 100 pF
ADDR hold from ALE falling edge	TAH	15	-	-	ns	CLOAD = 100 pF
$\overline{WR}$ pulse width Low	TWPW	95	-	-	ns	CLOAD = 100 pF
$\overline{RD}$ hold time after $\overline{BSY}$ High	TRDH	0	-	-	ns	CLOAD = 100 pF on $\overline{RD}$
DATA valid from $\overline{RD}$ falling edge	TDPR	5	-	70	ns	CLOAD = 100 pF
DATA hold from $\overline{RD}$ rising edge	TDHR	2	-	15	ns	CLOAD = 100 pF
$\overline{BSY}$ Low delay from $\overline{RD}$ or $\overline{WR}$ Low	TBP	5	-	55	ns	CLOAD = 20 pF / 2 kΩ
$\overline{BSY}$ Low duration	TBWL	122	-	344	ns	CLOAD = 20 pF / 2 kΩ
DATA setup to $\overline{WR}$ rising edge	TDSUW	30	-	-	ns	CLOAD = 100 pF
DATA hold from $\overline{WR}$ rising edge	TDHW	25	-	-	ns	CLOAD = 100 pF
$\overline{INT}$ clear after $\overline{RD}$ High for ADDR = 08h	TDCI	244	-	470	ns	CLOAD = 20 pF / 2 kΩ

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 11: Microprocessor Timing - Read Operations

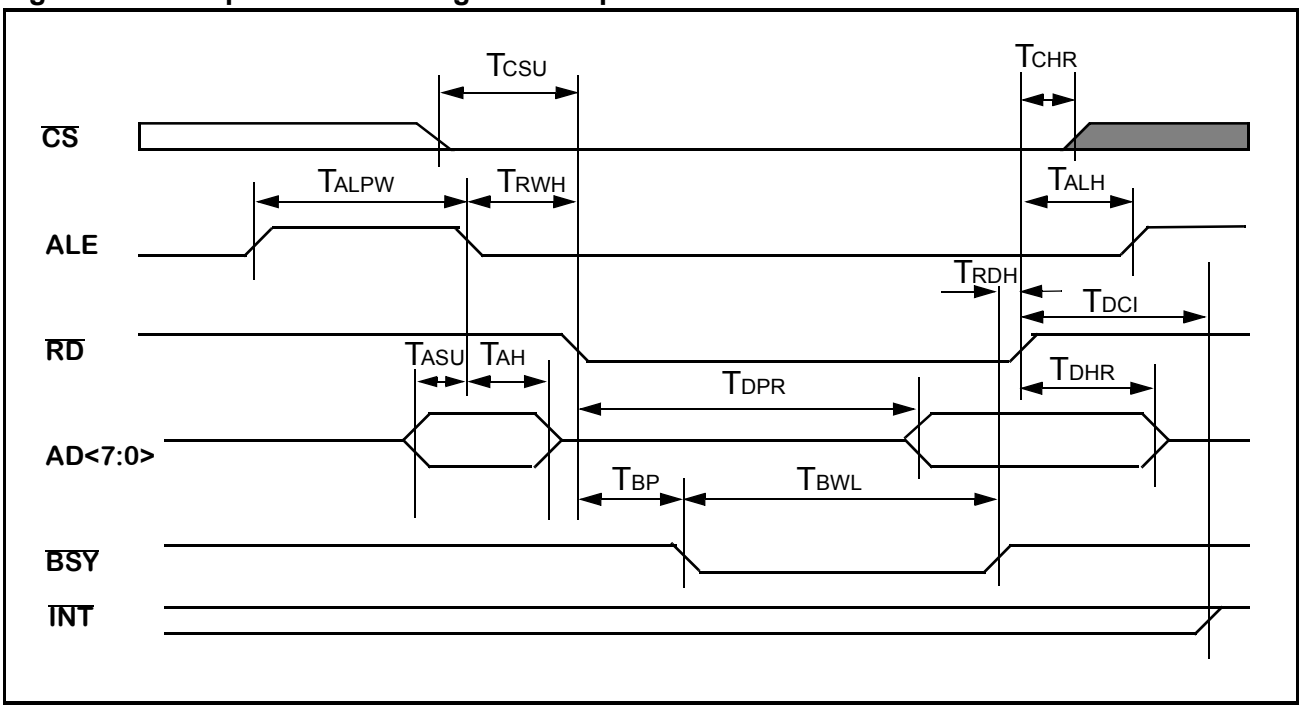
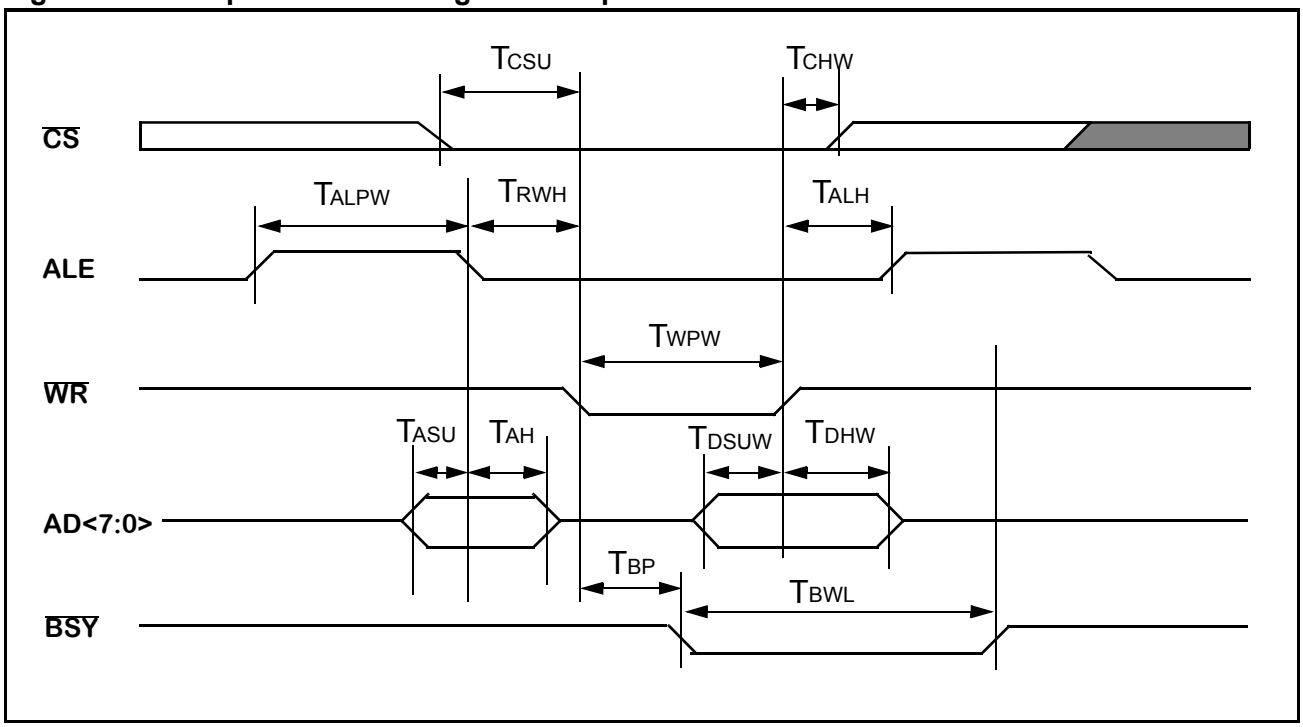


Figure 12: Microprocessor Timing - Write Operations



REGISTER DEFINITIONS

Introduction

The LXT441 incorporates a total of 19 registers, 8 Write and 11 Read registers. Refer to Table 12 for a complete list of register designations and addresses. Register addresses and other hexadecimal numbers are represented as “0xnn” where “nn” is the hex value.

Table 12: LXT441 Register Set

Address	Write Registers		Read Registers	
AD<7:0>	WRx	Name	RDx	Name
xxx00000	WR0	Device Control Register	RD0	readback of WR0
xxx00001	WR1	Transmit Control Register	RD1	readback of WR1
xxx00010	WR2	Receive Control Register	RD2	readback of WR2
xxx00011	Reserved			
xxx00100	Reserved			
xxx00101	WR5	EIA Select Register	RD5	readback of WR5
xxx00110	Reserved			
xxx00111	WR7	Transmit EIA Data Register	RD7	Receive EIA Data Register
xxx01000	WR8	Interrupt Enable Register	RD8	Interrupt Status Register
xxx01001	WR9	EIA Control Register	RD9	EIA Status Register
xxx01010	Reserved		RDA	Device Status Register
xxx01011	Reserved		RDB	Rx Slicer Level Register
xxx01100	WRC	Rx Code Interrupt Enables	RDC	Rx Codes Register
xxx01101	Reserved		RDD	Invalid BPV Counter
xxx01110	Reserved			
xxx01111	Reserved			

Table 13: LXT441 Register Bit Mapping

Register	R/W	Addr	b7	b6	b5	b4	b3	b2	b1	b0
Device Control	R/W	0x00	0	OCU	TCCT	SCT_EN	0	0	MODE1	MODE0
Transmit Control	R/W	0x01	BONDEN	CALLMD	0	TX_MRK	ZS_DIS	TX_CMI	TX_OOS	TX_OOF
Receive Control	R/W	0x02	DSU_LP	TX_DLP	CSU_LP	FILFCE	FFILT3	FFILT2	FFILT1	FFILT0
EIA Select	R/W	0x05	0	0	EIAREG	0	0	0	0	0
Tx EIA Data	W	0x07	D1	D2	D3	D4	D5	D6	D7	X, C, or D8
Rx EIA Data	R	0x07	D1	D2	D3	D4	D5	D6	D7	X, BF, C, or D8
Interrupt Enable	W	0x08	EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE
Interrupt Status	R	0x08	EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE
EIA Control (reset value)	W	0x09	FC_DCE (0)	DSR (1)	DCD (1)	RI (0)	CTS (1)	FC_DTE (0)	DTR (1)	RTS (1)
EIA Status	R	0x09	FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS
Device Status	R	0x0A	RLOS	FSYNC	ACTIVE	ISTATE	LL3	LL2	LL1	LL0
Rx Slicer Level	R	0x0B	MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0
Rx Code Interrupt Enable (reset value)	W	0x0C	MRK_EN (1)	ZSC_EN (0)	CMI_EN (1)	OOS_EN (0)	OOF_EN (0)	DLP_EN (0)	0 (0)	UNM_EN (0)
Rx Codes	R	0x0C	RX_DMI	RX_ZSC	RX_CMI	RX_OOS	RX_OOF	RX_DLP	RX_UMC	UNMTCH
BPV Count	R	0x0D	IBPV7	IBPV6	IBPV5	IBPV4	IBPV3	IBPV2	IBPV1	IBPV0

1. A Low on the $\overline{RST}$ input will force all register bits to 0, except where specified.

Table 14: Register WR0 - Device Control - Address 0x00

b7	b6	b5	b4	b3	b2	b1	b0
-	OCU	TCCT	SCT_EN	-	FTEST	MODE1	MODE0

Bit	Mnemonic	Function
b7	-	**Reserved.** Program to 0.
b6	OCU	**OCU and DSU Mode Selection.** Controls timing sources in conjunction with TCCT (see TCCT bit description for additional information).
b5	TCCT	**Tail Circuit.** Controls timing sources in conjunction with OCU as follows: **Bits<6:5>** / **Source for $\overline{\text{SCT\_E}}$** / **Source for TCLK** 10 / XTALI via Internal Oscillator / XTALI via Internal Oscillator[1] 11 / N/A / $\overline{\text{SCT\_E}}$ input pin 00 / RCLK / RCLK 01 / N/A / $\overline{\text{SCT\_E}}$ input pin
b4	SCT_EN	**Serial Clock Transmit Enable.** 0 = $\overline{\text{SCT\_E}}$ pin set to high impedance state; 1 = $\overline{\text{SCT\_E}}$ pin enabled as an output.
b3	-	**Reserved.** Program to 0.
b2	FTEST	**Factory Test (FTEST).** Program to 0.
b<1:0>	MODE<1:0>	**Mode Select (MODE<1:0>).** Sets Mode and Line Rate as follows: **Bits<1:0>** / **Operating Mode** / **Line Rate** 00 / DDS-PRI / 56 kbps 11 / DDS-PRI / 56 kbps 01 / DDS-SC / 72 kbps 10 / CC-64K / 72 kbps

1. Only applicable for DDS-PRI 56 kbps applications (MODE<1:0> = 00 or 11).

Table 15: Register WR1 - Transmit Control (DDS-PRI Mode) - Address 0x01

b7	b6	b5	b4	b3	b2	b1	b0
BONDEN	CALLMD	-	TX_MRK	ZS_DIS	TX_CM	TX_OOS	TX_OOF

Bit	Mnemonic	Function
b7	BONDEN	**Bonding Enable.** 0 = Bonding frame detection disabled; 1 = Bonding frame detection enabled.
b6	CALLMD	**Call Mode.** 0 = Allow data transfer from DTE; 1 = Indicate to DTE that call processing is underway
b5	-	**Reserved.** Program to 0.
b4	TX_MRK	**Transmit All Marks.** 1 = Transmit All Marks, the Data Mode Idle (DMI) sequence. (also sends all 1s DMI in CC-64K mode)
b3	ZS_DIS	**Zero Suppression Disable.** 1 = Disable Transmit Zero Suppression
b2	TX_CMI	**Transmit Control Mode Idle.** 1 = Transmit Control Mode Idle sequence
b1	TX_OOS	**Transmit Out Of Service.** 1 = Transmit Out Of Service sequence
b0	TX_OOF	**Transmit Out Of Frame.** 1 = Transmit Out Of Frame sequence

Table 16: Register WR1 - Transmit Control (DDS-SC Mode) - Address 0x01

b7	b6	b5	b4	b3	b2	b1	b0
T_UMC	-	-	T_IDLE	T_ZER	T_CMI	T_ASC	T_MOS

Bit	Mnemonic	Function
b7	T_UMC	**Transmit UMC.** 1 = Transmit Unassigned Multiplex Code sequence
b<6:5>	-	**Reserved.** Program to 0.
b4	T_IDLE	**Transmit Idle.** 1 = Transmit the Data Mode Idle (DMI) sequence. (also sends all 1s DMI in CC-64K mode)
b3	T_ZER	**Transmit All 0s.** 1 = Transmit all Zeros
b2	T_CMI	**Transmit Control Mode Idle.** 1 = Transmit Control Mode Idle sequence.
b1	T_ASC	**Transmit Abnormal Station Code.** 1 = Transmit Abnormal Station Code sequence
b0	T_MOS	**Transmit Mux Out of Sync.** 1 = Transmit Multiplexer Out of Sync sequence

Table 17: Register WR2 - Receive Control - Address 0x02

b7	b6	b5	b4	b3	b2	b1	b0
DSU_LP	TX_DLP	CSU_LP	FILFCE	FFILT3	FFILT2	FFILT1	FFILT0

Bit	Mnemonic	Function
b7[1]	DSU_LP	**DSU Loopback.** 1 = Forces local DSU loopback (EIA RD connected to TD)
b6	TX_DLP	**Transmit Non-Latching DSU Loopback.** 1 = Transmit Non-Latching DSU Loopback Code in DDS-SC, or BPV sequence in DDS-PRI. Not used in CC-64K
b5[2]	CSU_LP	**CSU Loopback.** 1 = Forces CSU loopback
b4	FILFCE	**Filter Force Enable.** 0 = Filter Forcing Disabled (Program to 0 for normal operation.); 1 = Filter Forcing Enabled
b<3:0>	FFILT<3:0>	**Filter Forcing Control Bits.** Filter Gain = (0X0F - FFILT<3:0>)*6dB.

1. Readback of RD2 yields the logical OR of the value written to bit b7 (DSU_LP) and DSU loop status.
2. Readback of RD2 yields the logical OR of the value written to bit b5 (CSU_LP) and CSU loop status.

Table 18: Register WR5 - EIA Select - Address 0x05

b7	b6	b5	b4	b3	b2	b1	b0
-	-	EIAREG	-	-	-	-	-

Bit	Mnemonic	Function
b<7:6>	-	**Reserved.** Program to 0.
b5	EIAREG	**EIA Register Mode.** 0 = Transmit data sourced by EIA TD pin; 1 = Transmit data sourced by transmit EIA data register.
b<4:0>	-	**Reserved.** Program to 0.

Table 19: Register WR7 - Transmit EIA Data - Address 0x07

b7	b6	b5	b4	b3	b2	b1	b0
D1	D2	D3	D4	D5	D6	D7	X, C, D8

Bit	Mnemonic	Function
b<7:1>	D<1:7>	**Data Bits.** Data transmitted on 4-wire link when EIAREG = 1. Refer to Table 20 for data formats.
b0	X,C,D8	**EIA Register Mode.** X = Don't Care in DDS-PRI. C = Secondary channel bit in DDS-SC. D8 = Data bit 8 in CC-64K.

Table 20: Register WR7 - Transmit EIA Data Formats

Mode	Line Rate	4-Wire Data Format									Comments
DDS-PRI	56 kbps	D1	D2	D3	D4	D5	D6	D7			7-bit byte
DDS-SC	72 kbps	D1	D2	D3	D4	D5	D6	D7	F	C	9-bit byte
CC-64K	72 kbps	D1	D2	D3	D4	D5	D6	D7	F	D8	9-bit byte
Mode	**DTE Clock**	**DTE Serial Data Format**									**Comments**
DDS-PRI	56 kbps smooth	D1	D2	D3	D4	D5	D6	D7			7-bit byte
DDS-SC	64 kbps gapped	D1	D2	D3	D4	D5	D6	D7	C		8-bit byte
CC-64K	64 kbps gapped	D1	D2	D3	D4	D5	D6	D7	D8		8-bit byte

1. D*x* = Data bits to/from DTE
2. C = DDS secondary channel control bits
3. F = DDS framing bits

Table 21: Register RD7 - Rx EIA Data - Address 0x07

b7	b6	b5	b4	b3	b2	b1	b0
D1	D2	D3	D4	D5	D6	D7	X, BF, C, D8

Bit	Mnemonic	Function
b<7:1>	D<1:7>	**Data Bits.** Data received on 4-wire link
b0	X,BF,C,D8	**EIA Register Mode.** X = Don't Care in DDS-PRI. BF = Bonding Frame indicator in DDS-PRI, if BONDEN=1. C = Secondary channel bit in DDS-SC. D8 = Data bit 8 in CC-64K

Table 22: Register WR8 - Interrupt Enable - Address 0x08

b7	b6	b5	b4	b3	b2	b1	b0
EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE

Bit	Mnemonic	Function
b7	EIADEL	**EIA Control Lead Change Interrupt Enable.** 0 = Disable; 1 = Enable.
b6	IDEL	**Loop Current Change Interrupt Enable.** 0 = Disable; 1 = Enable.
b5	RX_CODE	**Receive BPV Control Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b4	V_OFL	**Violations Count Overflow Interrupt Enable.** 0 = Disable; 1 = Enable.
b3	XBPV	**Excess Invalid BPV Interrupt Enable.** 0 = Disable; 1 = Enable.
b2	FSYNC	**Bonding, or DDS FAW Sync Interrupt Enable.** 0 = Disable; 1 = Enable.
b1	RSYNC	**Receive $\overline{\text{SYNC}}$ Interrupt Enable.** 0 = Disable; 1 = Enable.
b0	ACTIVE	**Active State Interrupt Enable.** 0 = Disable; 1 = Enable.

1. On power-up, this register contains all-zeros, which disables all interrupts.

Table 23: Register RD8 - Interrupt Status - Address 0x08

b7	b6	b5	b4	b3	b2	b1	b0
EIADEL	IDEL	RX_CODE	V_OFL	XBPV	FSYNC	RSYNC	ACTIVE

Bit	Mnemonic	Function
b7	EIADEL	**EIA Control Lead Change Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when either the $\overline{\text{DTR}}$ or $\overline{\text{RTS}}$ input line changes state in the LXT441.
b6	IDEL	**Loop Current Change Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when the loop current state changes. For changes in loop current direction, both inputs $\overline{\text{LCTR}}$ and $\overline{\text{LCRT}}$ will change state. State transitions of these two signals are debounced for 1.5 ms and multiple transitions within this time period are resolved into only one IDEL event.
b5	RX_CODE	**Receive BPV Code Interrupt.** 1 = Interrupt has occurred. This interrupt is generated upon reception of or cessation of reception of the codes listed in Table 27 (Register RDC description) as enabled by the corresponding bits in register WRC. In DDS-PRI mode, RX_DMI will generate an interrupt only when CALLMD (in register WR1) is set to logic 1 by the user. In DDS-SC mode, RX_DMI will never generate an interrupt.
b4	V_OFL	**Violations Count Overflow Interrupt.** 1 = Interrupt has occurred. This interrupt is generated when the Invalid Bipolar Violations Counter (V_CNT0 to V_CNT7) overflows at an invalid BPV count of 256.
b3	XBPV	**Excess Invalid BPV Interrupt.** 1 = Interrupt has occurred. If eight or more occurrences of invalid BPV events in sixteen groups of consecutive mark symbols are received, the XBPV interrupt is generated. This high density of BPV's requires re-activation of the LXT441, via an external $\overline{\text{RST}}$ pulse.
b2	FSYNC (BSYNC)	**Bonding, or DDS FAW Sync.** 1 = Interrupt has occurred. The Bonding Frame Sync (BSYNC) or Bit Frame Sync (FSYNC) interrupt is generated when either going into or out of synchronization for Bonding Sync or DDS-SC/CC-64K FAW sync.
b1	RSYNC	**Receive $\overline{\text{SYNC}}$ Interrupt.** 1 = Interrupt has occurred. The RSYNC interrupt is generated coincident with the falling edge of the $\overline{\text{SYNC}}$ pulse.
b0	ACTIVE	**Active State Interrupt.** 1 = Interrupt has occurred. The ACTIVE interrupt is generated when the LXT441 enters or exits the receiver active state. When activation sequence has completed, and reliable data transmission is achieved, the receiver enters the active state. When receive signal energy is lost, or is detected to be outside the range required for optimal equalization, the receiver exits the active state, and attempts to re-activate.

1. On power-up, this register contains all-zeros. All RD8 bits which are High will be cleared along with the interrupt when RD8 is read.

Table 24: Register WR9 - EIA Control - Address 0x09

b7	b6	b5	b4	b3	b2	b1	b0
FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS

Bit	Mnemonic	Function
b7	FC_DCE	**Force DCE Enable.** 0 (Default) = Disables User Programming of DCE Control Leads; 1 = Enables User Programming of DCE Control Leads.
b6	DSR	**Data Set Ready.** 0 = DSR Inactive; 1 (Default) = DSR Active.
b5	DCD	**Data Carrier Detect.** 0 = DCD Inactive; 1 (Default) = DCD Active.
b4	RI	**Ring Indicator.** 0 (Default)= RI Inactive; 1 = RI Active.
b3	CTS	**Clear to Send.** 0 = CTS Inactive; 1 (Default) = CTS Active.
b2	FC_DTE	**Force DTE Enable.** 0 (Default) = Disables User Programming of DTE Control Leads; 1 = Enables User Programming of DTE Control Leads.
b1	DTR	**Data Terminal Ready.** 0 = DTR Inactive; 1 (Default) = DTR Active.
b0[1]	RTS	**Request to Send.** 0 = RTS Inactive; 1 (Default) = RTS Active.

1. Forcing this bit will not cause CTS transition.

Table 25: Register RD9 - EIA Status - Address 0x09

b7	b6	b5	b4	b3	b2	b1	b0
FC_DCE	DSR	DCD	RI	CTS	FC_DTE	DTR	RTS

Bit	Mnemonic	Function
b7	FC_DCE	**Force DCE Enable.** 0 (Default) = User Programming of DCE Control Leads Disabled; 1 = User Programming of DCE Control Leads Enabled
b6[1]	DSR	**Data Set Ready.** 0 = DSR Inactive; 1 (Default) = DSR Active.
b5[1]	DCD	**Data Carrier Detect.** 0 = DCD Inactive; 1 (Default) = DCD Active.
b4[1]	RI	**Ring Indicator.** 0 (Default) = RI Inactive; 1 = RI Active.
b3[1]	CTS	**Clear to Send.** 0 = CTS Inactive; 1 (Default) = CTS Active.
b2	FC_DTE	**Force DTE Enable.** 0 (Default) = User Programming of DTE Control Leads Disabled; 1 = User Programming of DTE Control Leads Enabled.
b1[2]	DTR	**Data Terminal Ready.** 0 = DTR Inactive; 1 (Default) = DTR Active.
b0[2]	RTS	**Request to Send.** 0 = RTS Inactive; 1 (Default) = RTS Active.

1. For DCE control leads, status is actual line condition - not value forced via WR9.
2. For DTE control leads, status is actual value on device pin - not value forced via WR9.

Table 26: Register WRC - Rx Code Interrupt Enable - Address 0x0C

b7	b6	b5	b4	b3	b2	b1	b0
IDLE	ZSC	CMI	OOS	OOF	DLP	UMC	UNM

Bit	Mnemonic	Function
b7	IDLE	**RX_DMI Interrupt Enable.** 0 = Disable; 1 = Enable.
b6	ZSC	**Zero Code Interrupt Enable.** 0 = Disable; 1 = Enable.
	(ZERO)	**(all zeros in DDS-SC/CC-64K).** 0 = Disable; 1 = Enable.
b5	CMI	**Receive Control mode Idle Interrupt Enable.** 0 = Disable; 1 = Enable.
b4	OOS	**Out of Sync.** 0 = Disable; 1 = Enable.
	(ASC)	**Abnormal Station Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b3	OOF	Out of Frame Interrupt Enable. 0 = Disable; 1 = Enable.
	(MOS)	**Mux out of Sync Interrupt Enable.** 0 = Disable; 1 = Enable.
b2	DLP	**DSU Loopback Interrupt Enable.** 0 = Disable; 1 = Enable.
b1	UMC	**Unassigned Mux Code Interrupt Enable.** 0 = Disable; 1 = Enable.
b0	UNM	**Unmatched Code Interrupt Enable.** 0 = Disable; 1 = Enable.

Table 27: Register RDC - Rx Codes - Address 0x0C

b7	b6	b5	b4	b3	b2	b1	b0
RX_DMI	RX_ZSC	RX_CMI	RX_OOS	RX_OOF	RX_DLP	RX_UMC	UNMTCH

Bit	Mnemonic	Function[1,2]
b7	RX_DMI	**Receiving DMI.** 1 = Receiving Data Mode Idle
b6	RX_ZSC	**Receiving ZSC.** 1 = Receiving Zero Suppression Code in DDS-PRI
	(RX_ZER)	**(All Zeros)**. 1 = Receiving All 0s in DDS-SC
b5	RX_CMI	**Receiving CMI.** 1 = Receiving Control Mode Idle
b4	RX_OOS	**Receiving OOS.** 1 = Receiving Out of Service code in DDS-PRI
	(RX_ASC)	**(Receiving ASC).** 1 = Receiving Abnormal Station Code in DDS-SC
b3	RX_OOF	**Receiving OOF.** 1 = Receiving Out of Frame code in DDS-PRI
	(RX_MOS)	**(Receiving MOS).** 1 = Receiving Mux Out of Sync Code in DDS-SC
b2	RX_DLP	**Receiving DLP.** 1 = Receiving valid DSU Non-latching loopback code
b1	RX_UMC	**Receiving UMC.** 1 = Receiving Unassigned Mux Code in DDS-SC
b0	UNMTCH	**Unmatched Code.** 1 = Receiving control code that does not match codes in Table 28

1. An interrupt will be generated due to the presence of a control code if the corresponding enable bit in WRC is set. Only one code word need be received for the corresponding bit to go High in all cases except for RX_DLP. In the case of DSU loopback code, four consecutive repetitions of the RX_DLP code are required. The code must be absent for at least five consecutive word periods for the bit to be cleared.
2. The bits in this register are not latched, and are updated every 125 µs.

Table 28: Summary of Transmit and Receive Control Codes

Code Description	DDS-PRI Code								DDS-SC Code										CC-64K	Tx Priority
	Name	D1	D2	D3	D4	D5	D6	D7	Name	D1	D2	D3	D4	D5	D6	D7	F	C		
Data Mode Idle	MRK	B	B	B	B	B	B	B	IDLE	1	1	1	1	1	1	1	F	1	IDLE	Priority 1 (highest)
Control Mode Idle	CMI	B	B	B	B	X	O	V	CMI	1	1	1	1	1	1	1	F	0	N/A	Priority 2; Priority 6[1] with TX_DLP =0
DSU Loopback	DLP	N	O	B	O	X	O	V	DLP	N	0	1	0	1	1	0	F	0	N/A	Priority 2; Priority 6[1] with TX_DLP =1
		replace with								replace with										
		O	O	B	O	O	O	O		N	0	1	0	0	0	0	F	1		
Out of Service or Abnormal Station	OOS	N	O	O	B	X	O	V	ASC	N	0	0	1	1	1	1	F	0	N/A	Priority 3
Out of Sync	OOF	N	O	B	B	X	O	V	MOS	N	0	0	1	1	0	1	F	0	N/A	Priority 4
Unassigned Mux	N/A	N/A							UMC	N	0	0	1	1	0	0	F	0	N/A	Priority 5
Zero-Suppression (All Zeros)	ZSC	_	O	O	O	X	O	V	ZER	0	0	0	0	0	0	0	F	0	N/A	Priority 6; For DDS-PRI replace OOOOOOO with OOOOXOV
		replace with																		
		_	O	O	O	O	O	O												
Data	---	---							---	---									---	Priority 7

1. Transmit CMI priority is 6 for $\overline{RTS}$=0 on the EIA interface.
2. B = a mark (pulse); V = bipolar violation mark; O = a space; X = B or O to make # of B's since last V odd. N = 1/0.
3. F = DDS-SC and CC-64K frame bit.
4. Bit numbering <D1:D7> is arbitrary for DDS-PRI codes.

Table 29: Register RDA - Device Status - Address 0x0A

b7	b6	b5	b4	b3	b2	b1	b0
RLOS	FSYNC	ACTIVE	ISTATE	LL3	LL2	LL1	LL0

Bit	Mnemonic	Function
b7	RLOS	**Receive Loss of Signal.** 1 = LXT441 Receiver has lost signal due to level being below threshold, or step change in signal magnitude. RLOS indicator, goes High after initial activation if receive signal level drops to zero volts, or drops by more than 6 dB. RLOS will then stay High until the receiver automatically re-initializes in the presence of the receive signal at a new voltage level, or the return of the signal at the old voltage level. An ACTIVE interrupt is generated in register RD8 when RLOS goes High, and again when RLOS goes Low to indicate the resumption of normal data reception. RLOS is not a latched bit.
b6	FSYNC	**FAW Sync.** 1 = DDS FAW Sync in DDS-SC or CC-64k
b5	ACTIVE	**Receiver Active.** 1 = LXT441 Receiver Activated
b4	ISTATE	**Loop Current Present.** 1 = Presence of loop current determined by a logic 0 level at $\overline{\text{LCRT}}$ or $\overline{\text{LCTR}}$ device pins. The $\overline{\text{LCRT}}$ and $\overline{\text{LCTR}}$ inputs are debounced for 1.5 ms after the initial transition by either signal. Also, up to 1.5 ms of skew between the state transitions in these signals is resolved into only one IDEL interrupt event as reported in RD8.
b<3:0>	LL<3:0>	**Loop Loss Indicator Bits.** Value of the receive filter selected by receive activation circuit. Refer to Table 30 for the nominal Nyquist frequency loop loss (+/-3dB) corresponding to the LL<3:0> value.

Table 30: Insertion Loss and Line Length Values for bits LL<3:0>

Line Rate	Parameter	Bit Codes LL<3:0>								
		0111	1000	1001	1010	1011	1100	1101	1110	1111
56 kbps	Insertion Loss (dB)	50.5	44.4	38.4	32.3	26.0	19.7	13.6	7.3	0.0
	Line Length (km)	8.5	7.5	6.4	5.3	4.2	3.2	2.1	1.1	0.0
72 kbps	Insertion Loss (dB)	50.7	45.0	38.8	32.5	26.3	20.0	14.0	7.4	0.0
	Line Length (km)	8.0	7.0	6.0	5.0	4.0	3.0	2.0	1.0	0.0

1. Insertion Loss @ fb/2 in dB.
2. Line Range in km (24 AWG PIC, no bridged taps)

Table 31: Register RDB - Rx Slicer Level - Address 0x0B

b7	b6	b5	b4	b3	b2	b1	b0
MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0

Bit	Mnemonic	Function
b<7:0>	MAG<7:0>	**Receive Signal Magnitude.** MAG<7:0> represents the receive slicer level, and is used with the LL0-LL3 bits from register RD_A to calculate the twisted-pair loop attenuation using the following formula[1]: Nyquist frequency Loop Attenuation in dB equals [Attenuation Value in dB for LL<3:0> at selected data rate[2]] + 20log10(0x3C/ MAG<7:0>hex).

1. The attenuation values for LL<3:0> at 56 and 72 kbps and the values for 20log10(0x3C/MAG<7:0>hex) can be added together to compute an estimate of the actual line loss to +/-1 dB.
2. Refer to Table 30 for attenuation values.

Table 32: Register RDD - Rx Invalid BPV Count - Address 0x0D

b7	b6	b5	b4	b3	b2	b1	b0
IBPV7	IBPV6	IBPV5	IBPV4	IBPV3	IBPV2	IBPV1	IBPV0

Bit	Mnemonic	Function
b<7:0>	IBPV<7:0>	**Invalid BPV Count.** IBPV<7:0> is an 8-bit count of receive pulses that are judged to be BPVs that are not legal DDS-PRI codes. When this counter is read, it is reset 00h. If this counter overflows, the V_OFL interrupt is set.