LXT908

Universal Ethernet Interface Adapter

General Description

The LXT908 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides all the active circuitry to interface most standard 802.3 controllers to either the 10BASE-T media or Attachment Unit Interface (AUI). In addition to standard 10 Mbps Ethernet, the LXT908 also supports full-duplex operation at 20 Mbps.

LXT908 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing and reversed polarity detection/correction. The LXT908 can be used to drive either the AUI drop cable or the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC compliant EMI performance.

The LXT908 is fabricated with an advanced CMOS process and requires only a single 3.3 or 5 volt power supply.

Applications

- 10BASE-T Hub and Switching products
- Computer/workstation 10BASE-T LAN adapter boards

Features

Functional Features

- Improved Filters - Simplifies FCC Compliance
- Integrated Manchester Encoder/Decoder
- 10BASE-T compliant Transceiver
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet

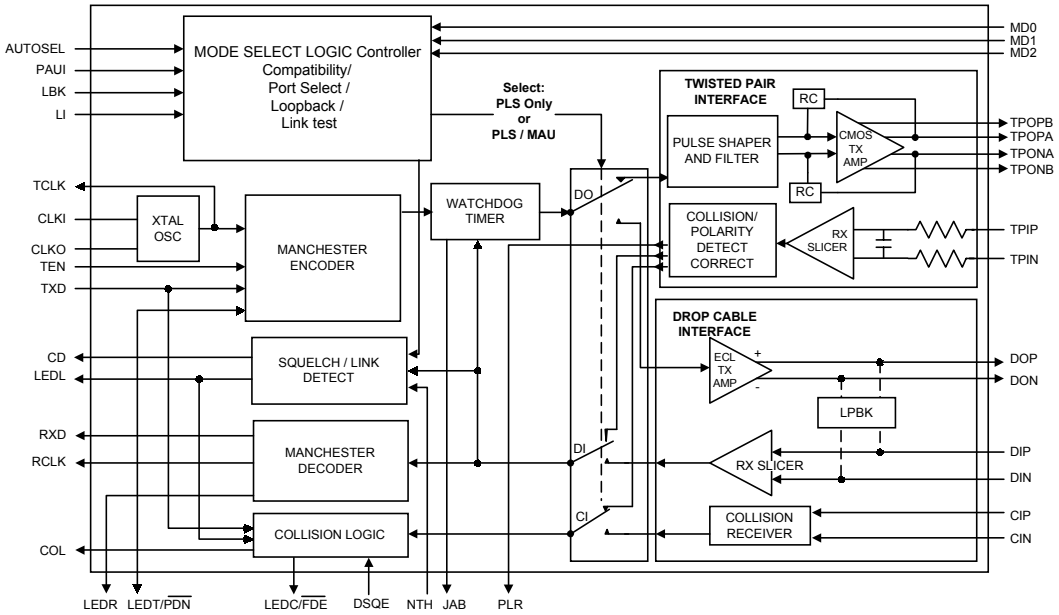
Convenience Features

- Automatic/Manual AUI/RJ45 Selection
- Automatic Polarity Correction
- SQE Disable/Enable function
- Power Down Mode with tristated outputs
- Four loopback modes
- Single 3.3V or 5V operation
- Available in 44-pin PLCC package

Diagnostic Features

- Four LED Drivers
- AUI/RJ45 Loopback

LXT908 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT908 Pin Assignments

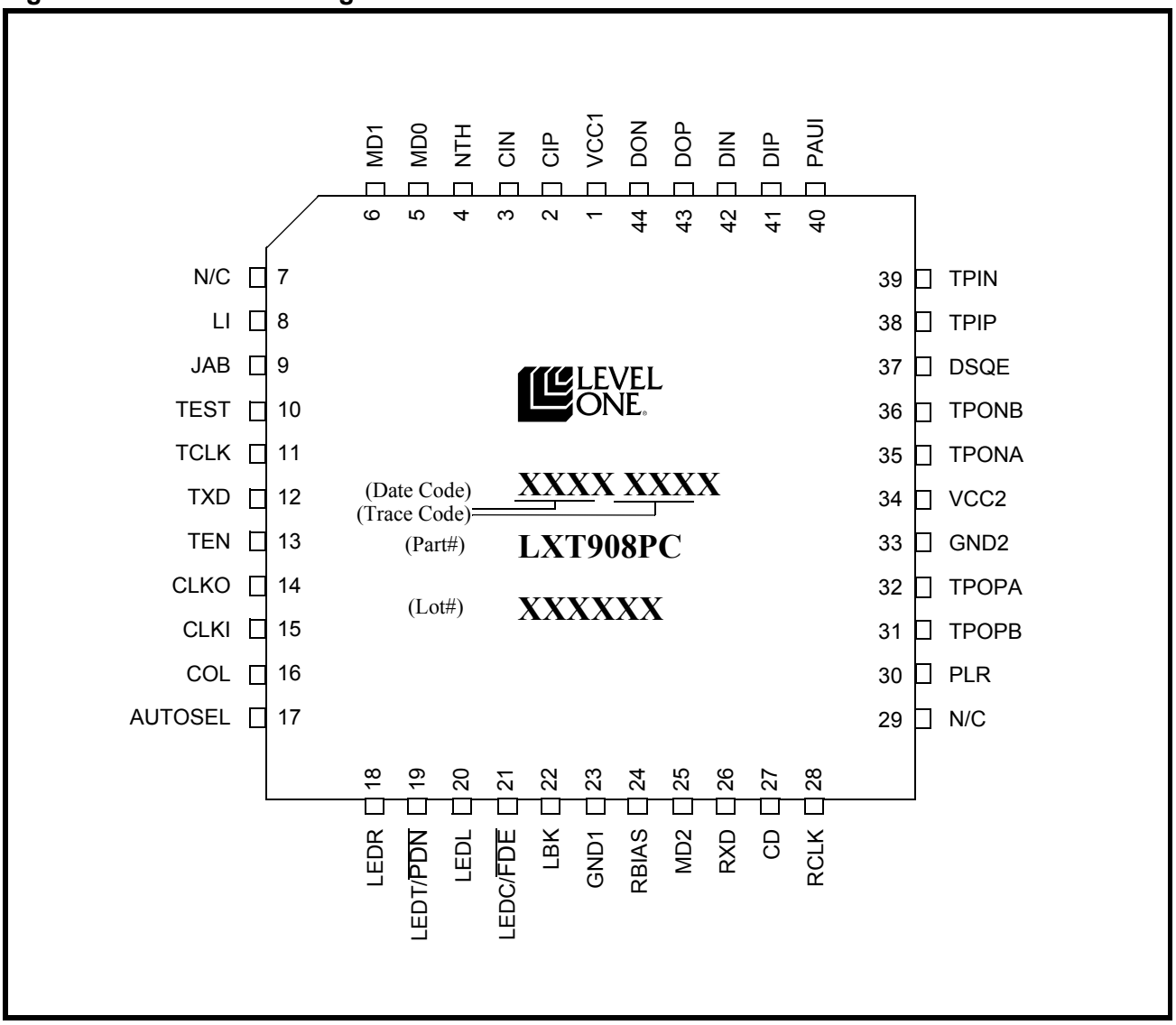


Table 1: LXT908 Signal Descriptions

Pin #	Symbol	I/O	Description
1 34	VCC1 VCC2	- -	**Power 1 and 2.** Connect to positive power supply terminal (+3.3VDC or +5 VDC).
2 3	CIP CIN	I I	**AUI Collision Pair.** Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
4	NTH	I	**Normal Threshold.** When NTH is High, the normal TP squelch threshold is in effect. When NTH is Low, the normal TP squelch threshold is reduced by 4.5 dB.
5 6 25	MD0 MD1 MD2	I I I	**Mode Select 0 (MD0), Mode Select 1 (MD1) and Mode Select 2 (MD2).** Mode select pins determine the controller compatibility mode as specified in Table 2.
7	N/C	-	**No Connect**. *This pin must be tied to ground or device damage may occur.*
8	LI	I	**Link Test Enable.** Controls Link Integrity Test; enabled when High, disabled when Low.
9	JAB	O	**Jabber Indicator.** Output goes High to indicate Jabber state.
10	TEST	I	**Test.** *This pin must be tied High.*
11	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller. TCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
12	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Test Specifications for details).
14 15	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller. COL goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
17	AUTOSEL	I	**Automatic Port Select.** When High, automatic port selection is enabled (the LXT908 defaults to the AUI port only if TP link integrity = Fail). When Low, manual port selection is enabled (the PAUI pin determines the active port).
18	LEDR	O	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive, except when data is being looped back to DIN/DIP from a remote transceiver (external MAU). LED "On" time (i.e., Low output) is extended by approximately 100 ms.
19	LEDT/ $\overline{\text{PDN}}$	O I	**Transmit LED (LEDT)/Power Down ($\overline{\text{PDN}}$).** Open drain driver for the transmit indicator LED. Output is pulled Low during transmit. LED "On" time (i.e., Low output) is extended by approximately 100 ms. If externally tied Low, the LXT908 goes to power down state. In power down state, TCLK, COL, RXD, CD and RCLK (pins 11, 16, 26, 27 and 28, respectively) are tri-stated.
20	LEDL	O I	**Link LED.** Open drain driver for link integrity indicator LED. Output is pulled Low during link test pass. If externally tied Low, internal circuitry is forced to "Link Pass" state and the LXT908 will continue to transmit link test pulses.

Table 1: LXT908 Signal Descriptions – continued

Pin #	Symbol	I/O	Description
21	LEDC/ $\overline{\text{FDE}}$	O I	**Collision LED (LEDC)/Full Duplex Enable ($\overline{\text{FDE}}$).** Open drain driver for the collision indicator LED pulls Low during collision. LED "On" time (i.e., Low output) is extended by approximately 100 ms. If externally tied Low, the LXT908 disables the internal TP loopback and collision detection circuits to allow full duplex operation or external TP loopback.
22	LBK	I	**Loopback.** Enables internal loopback mode. Refer to Functional Description and Test Specifications for details.
23 33	GND1 GND2	– –	**Ground Returns 1 and 2.** Connect to negative power supply terminal (ground).
24	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
26	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller. RXD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
27	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network. CD goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
28	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input. RCLK goes to high impedance (tri-state) when LEDT/$\overline{\text{PDN}}$ is pulled Low externally.
29	N/C	-	**No Connect.** *This pin must be tied to ground or device damage may occur.*
30	PLR	O	**Polarity Reverse.** Output goes High to indicate reversed polarity at the TP input.
32 31 35 36	TPOPA TPOPB TPONA TPONB	O O O O	**Twisted-Pair Transmit Pairs A & B.** Two differential driver pair outputs (A and B) to the twisted-pair cable.The outputs are pre-equalized. Each pair must be shorted together with an 11.5 Ω 1% resistor to match an impedance of 100Ω.
37	DSQE	I	**Disable SQE.** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE must be disabled for normal operation in Hub/Switch applications.
38 39	TPIP TPIN	I I	**Twisted-Pair Receive Pair.** A differential input pair from the TP cable. Receive filter is integrated on-chip. No external filters are required.
40	PAUI	I	**Port/AUI Select.** In Manual Port Select mode (AUTOSEL Low), PAUI selects the active port. When PAUI is High, the AUI port is selected. When PAUI is Low, the TP port is selected. In Auto Port Select mode, PAUI must be tied to ground.
41 42	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

FUNCTIONAL DESCRIPTION

Introduction

The LXT908 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an AUI (PLS-Only device) for use with 10BASE-2 or 10BASE-5 coaxial cable networks, or as an Integrated PLS/MAU for use with 10BASE-T twisted-pair networks. In addition to standard 10 Mbps operation, the LXT908 also supports full-duplex 20 Mbps operation.

The LXT908 interfaces a back end controller to either an AUI drop cable or a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the LXT908 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT908 Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/ MAU mode). The LXT908 Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the LXT908 performs all required MAU functions defined by the IEEE 802.3 10BASE–T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the LXT908 receives incoming signals from the AUI DI circuit with ± 18ns of jitter and drives the AUI DO circuit.

Controller Compatibility Modes

The LXT908 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Motorola, Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments, as well as custom controllers. Five different control signal timing and polarity schemes (Modes 1 through 5) are required to achieve this compatibility. Mode select pins (MD2:0) determine Controller compatibility modes as listed in Table 2. Refer to Test Specifications for a complete set of timing diagrams for each mode.

Transmit Function

The LXT908 receives NRZ data from the controller at the TXD input as shown in the block diagram on the first page of this Data Sheet, and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 2. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC-compliant EMI performance. During idle periods, the LXT908 transmits link integrity test pulses on the TPO circuit (if LI is enabled and integrated PLS/ MAU mode is selected). External resistors control the termination impedance.

Figure 2: LXT908 TPO Output Waveform

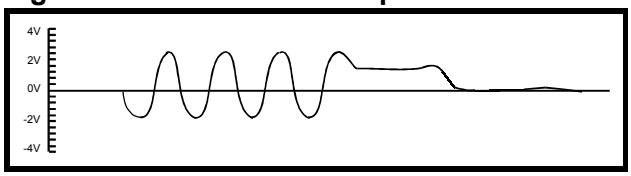


Table 2: Controller Compatibility Mode Options

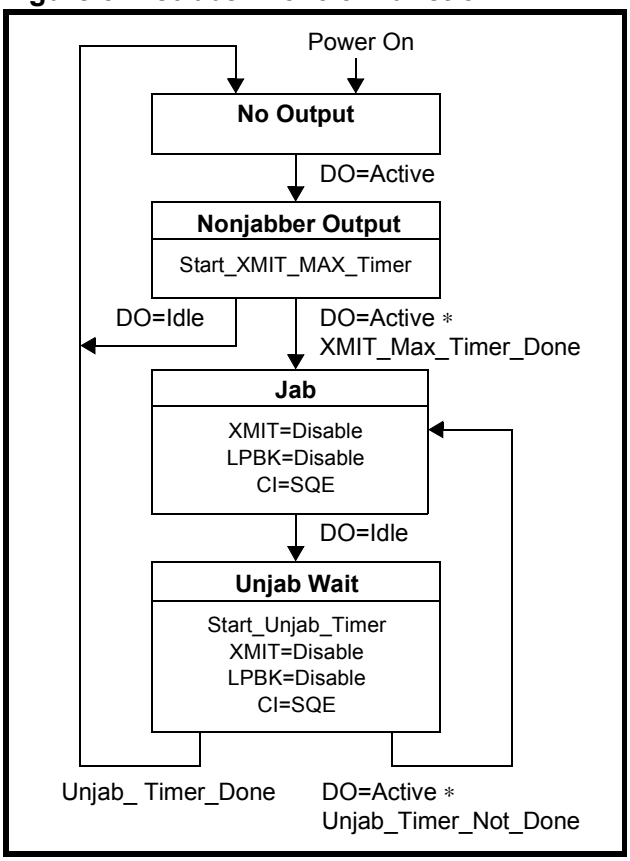
Controller Mode	MD2	MD1	MD0
Mode 1 - For AMD AM7990, Motorola 68EN360, MPC860 or compatible controllers	Low	Low	Low
Mode 2 - For Intel 82596 or compatible controllers	Low	Low	High
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[1]	Low	High	Low
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	Low	High	High
Mode 5 - For custom controllers (Mode 3 with TCLK, RCLK and COL inverted)	High	High	Low

1. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL in Mode 3; or on CLKI, LBK and TCLK in Mode 5.

Jabber Control Function

Figure 3 is a state diagram of the LXT908 Jabber control function. The LXT908 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the LXT908 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: Jabber Control Function



Receive Function

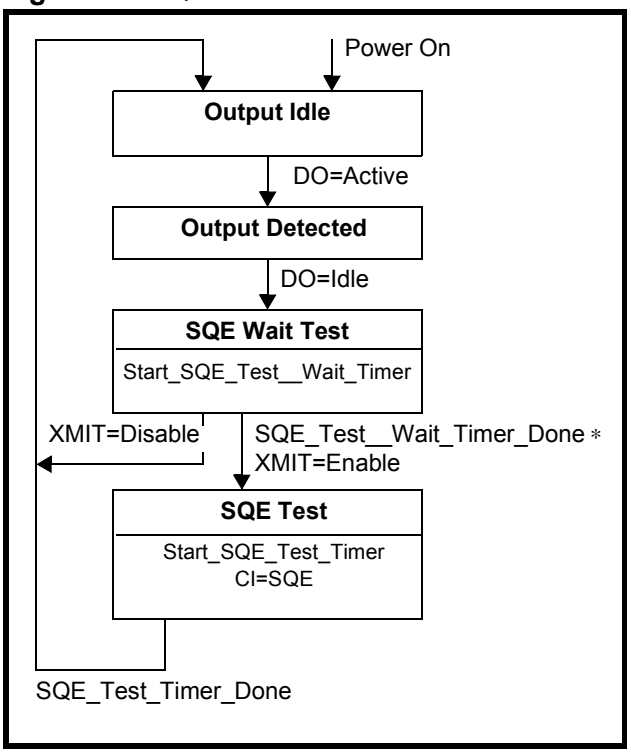
The LXT908 receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and recovered clock on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT908 receive function enters the idle state. If the polarity of the TPI circuit is reversed, LXT908 detects the polarity reverse and reports it via the PLR output. The LXT908 automatically corrects reversed polarity.

SQE Function

In the integrated PLS/MAU mode, the LXT908 supports the signal quality error (SQE) function as shown in Figure 4, although the SQE function can be disabled. After every successful transmission on the 10BASE-T network when SQE is enabled, the LXT908 transmits the SQE signal for 10BT ± 5BT over the internal CI circuit which is indicated on the COL pin of the device. SQE must be disabled for normal operation in hub and switch applications. In twisted-pair applications, the SQE function is disabled when DSQE is set High, and enabled when DSQE is Low. When using the 10BASE-2 port of the LXT908, the SQE function is determined by the external MAU attached.

Figure 4: SQE Function



Polarity Reverse Function

The LXT908 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT908 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.). Polarity correction is always enabled.

Loopback Function

The LXT908 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT908 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The LXT908 also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied Low, the LXT908 disables the collision detection and internal loopback circuits, to allow external loopback or full-duplex operation.

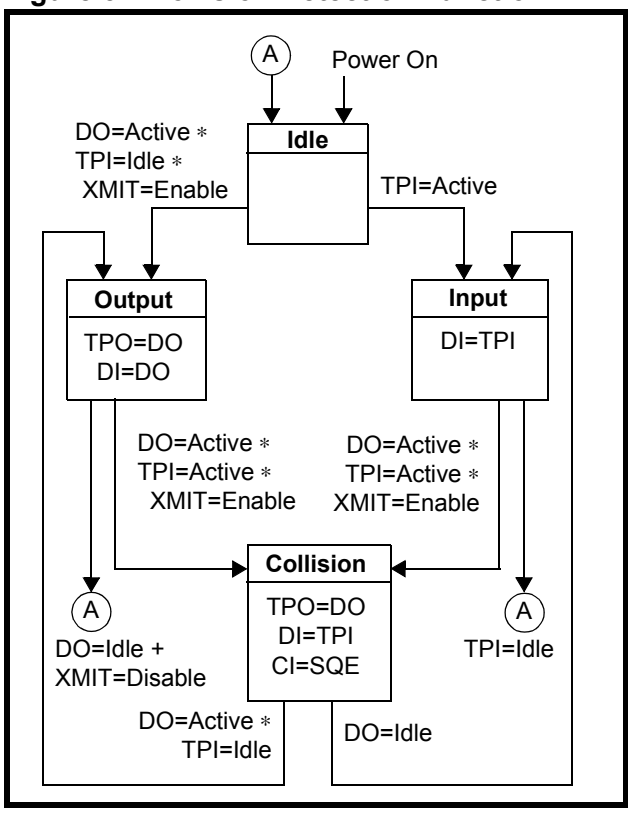
"Normal" TP loopback is controlled by pin 22 (LBK). When the TP port is selected and LBK is High, TP loopback is "forced", overriding collisions on the TP circuit. When LBK is Low, normal loopback is in effect.

AUI loopback is also controlled by the LBK pin. When the AUI port is selected and LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

Collision Detection Function

The collision detection function operates on the twisted pair side of the interface. For standard (half-duplex) 10BASE-T operation, a collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT908 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT908 collision detection function. Refer to Test Specifications for collision detection and COL/CI output timing (NOTE: For full-duplex operation, the collision detection circuitry must be disabled.)

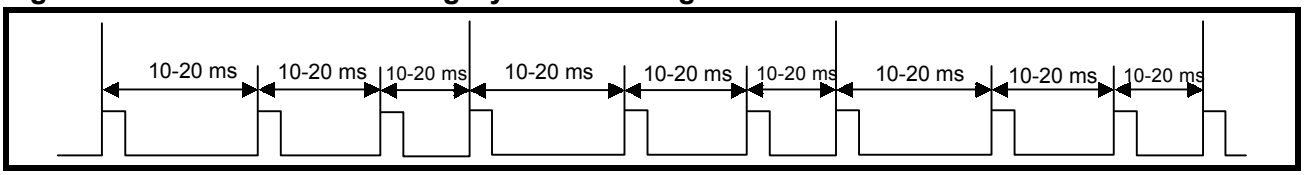
Figure 5: Collision Detection Function



Link Pulse Transmission

The LXT908 transmits standard link pulses which meet the 10BASE-T specifications. Figure 6 shows the link integrity pulse timing.

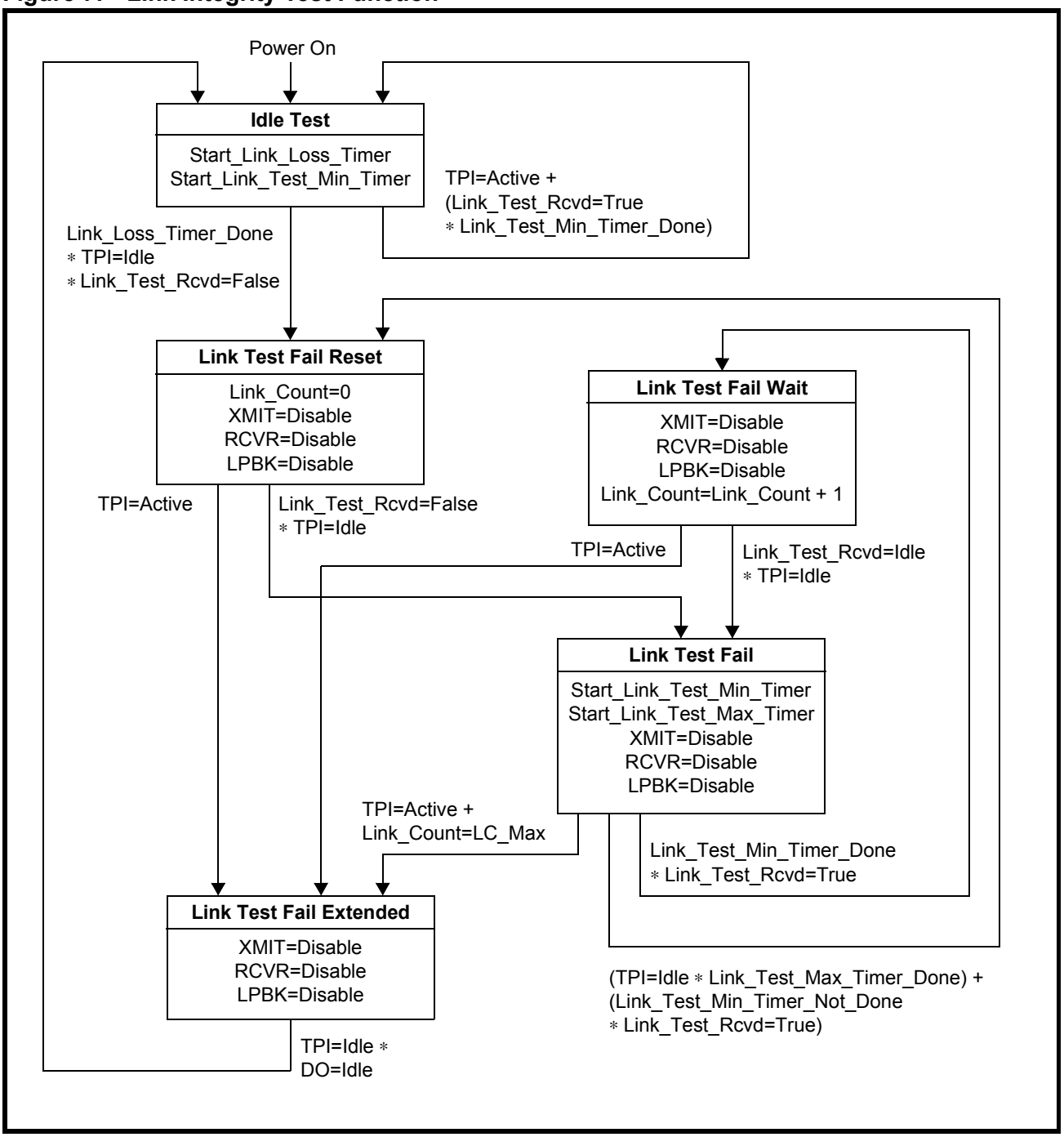
Figure 6: Transmitted Link Integrity Pulse Timing



Link Integrity Test Function

Figure 7 is a state diagram of the LXT908 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT908 ignores any link integrity pulse with interval less than 2 - 7ms. The LXT908 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 7: Link Integrity Test Function



APPLICATION INFORMATION

Figures 8 through 14 show some typical LXT908 applications.

External Components

Crystal Information

Suitable crystals are available from various manufacturers. Table 3 lists some suitable crystals based on limited evaluation. Designers should test and validate all crystals before using them in production.

Table 3: Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

Magnetic Information

The LXT908 requires a 1:1 ratio for the receive transformer and a 1:2 ratio for the transmit transformer. Table 4 lists transformers suitable for the applications described in this data sheet. Designers should test and validate all magnetics before committing to a specific component.

Table 4: Suitable Magnetics

Manufacturer	Part Number	
	Twisted-Pair	AUI
Belfuse	S553-5999-52	S553-1006-AE
	S553-5999-86	-
Fil-Mag	23Z118	23Z90
	23Z118SM	23Z90SM
Halo	TD74-1406Q	TD01-0756K
	TG74-1406N1	TG01-0756N
Valor	PT4152	LT6032
	ST4152	ST7032

Layout Requirements

Auto Port Select with External Loopback Control

Figure 8 is a typical LXT908 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT908 pin-out. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

Programmable option pins are grouped center left. The PAUI pin is tied Low and all other option pins are tied High. This set-up selects the following options:

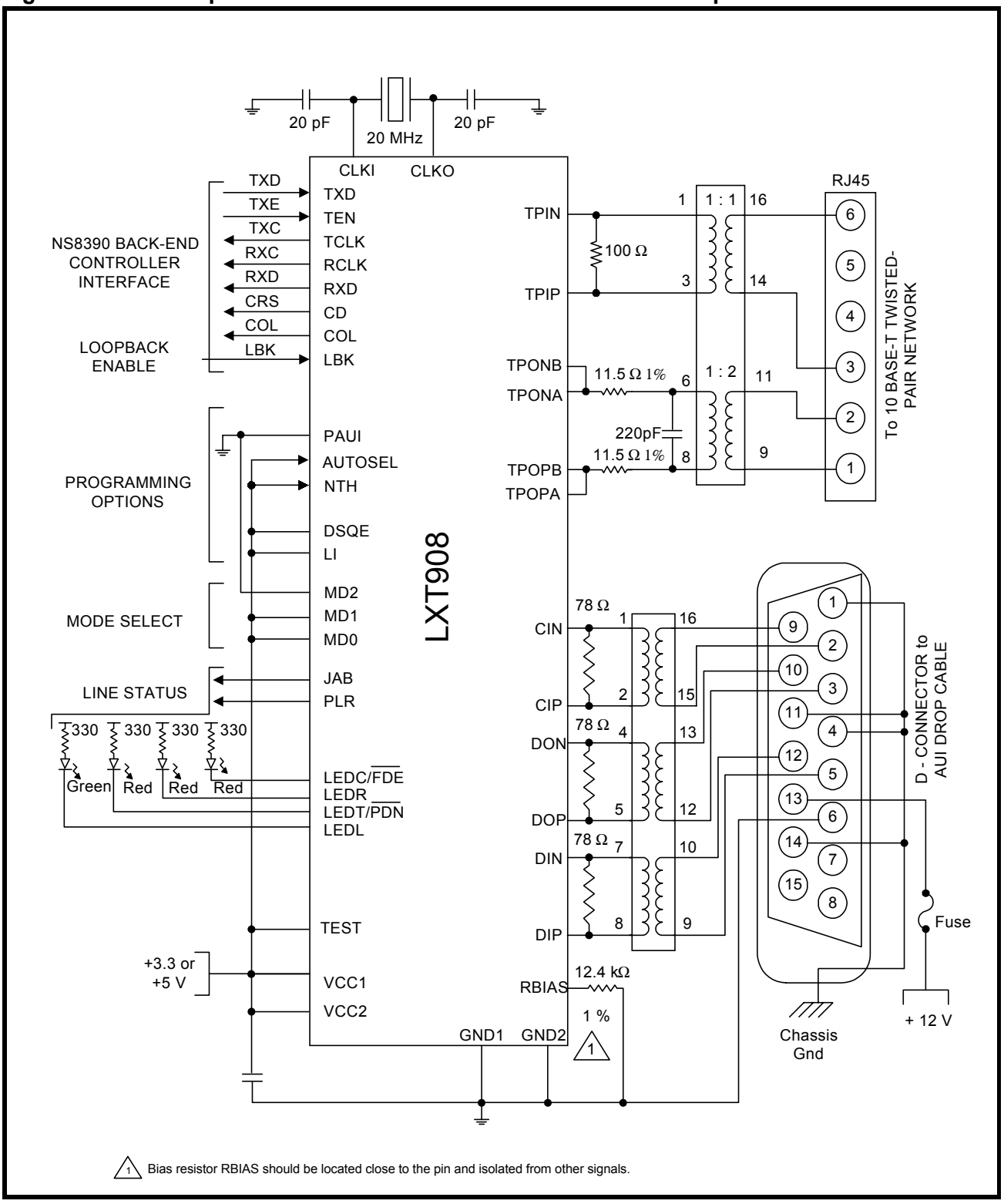
- Automatic Port Selection (PAUI Low and AUTOSEL High)
- Normal Receive Threshold (NTH High)
- Mode 4, compatible with National NS8390 controllers (MD2:0 = Low, High, High)
- SQE Disabled (DSQE High)
- Link Testing Enabled (LI High)

Status outputs are grouped at lower left. Line status outputs drive LED indicators and the Jabber and Polarity status indicators are available as required.

Power and ground pins are shown at the bottom of the diagram. A single power supply is used for both VCC1 and VCC2 with a decoupling capacitor installed between the power and ground busses.

The TP and AUI interfaces are shown at upper and lower right, respectively. Impedance matching resistors for 100 UTP are installed in each I/O pair but no external filters are required.

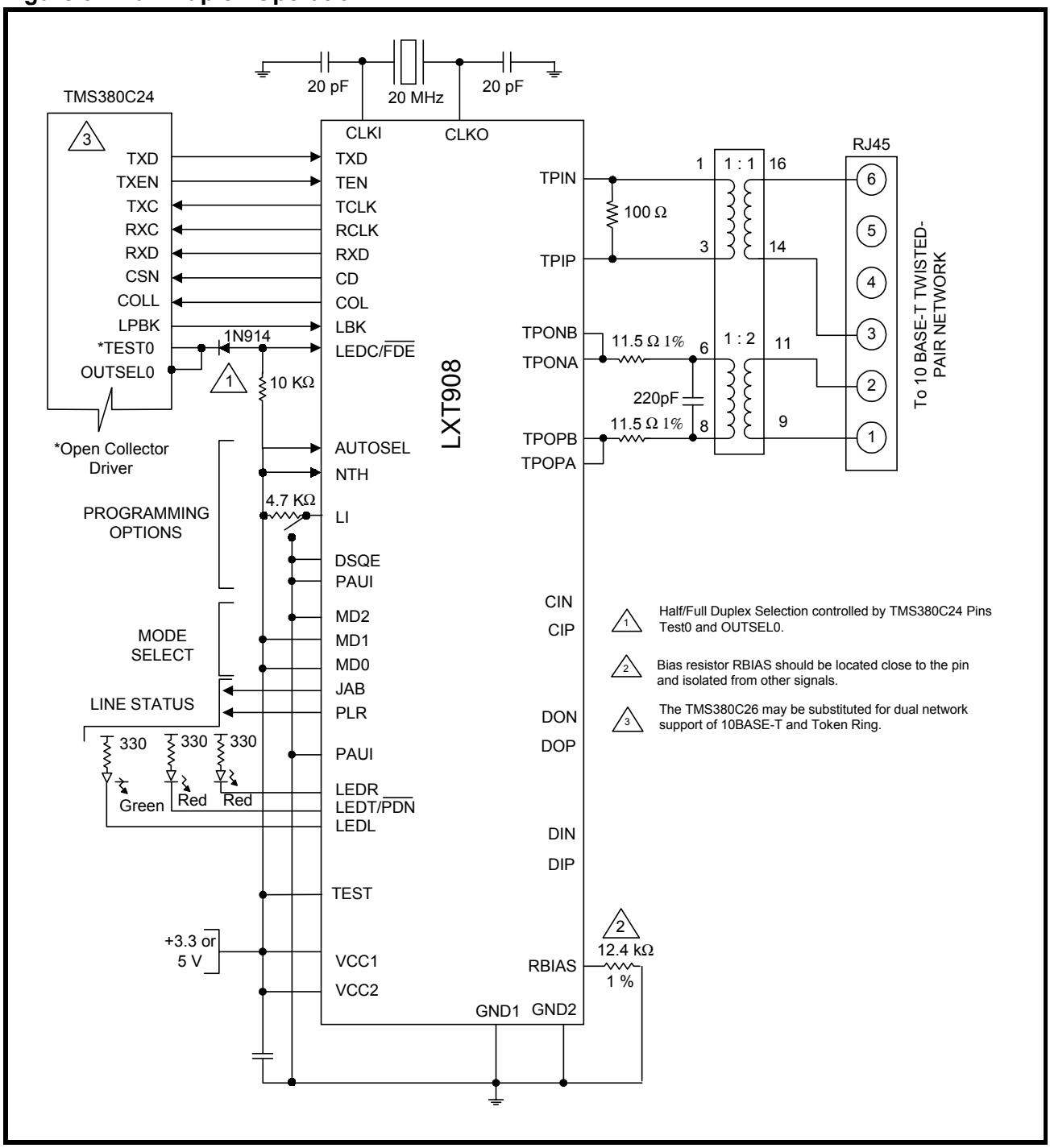
Figure 8: LAN Adapter Board - Auto Port Select with External Loopback Control



Full Duplex Support

Figure 9 shows the LXT908 with a Texas Instruments 380C24 CommProcessor. The 380C24 is compatible with Mode 4 (MD2:0 = Low, High, High). When used with the 380C24 or other full duplex-capable controller, the LXT908 supports full-duplex Ethernet, effectively doubling the available bandwidth of the network. In this application the SQE function is enabled (DSQE tied Low), and the LXT908 AUI port is not used.

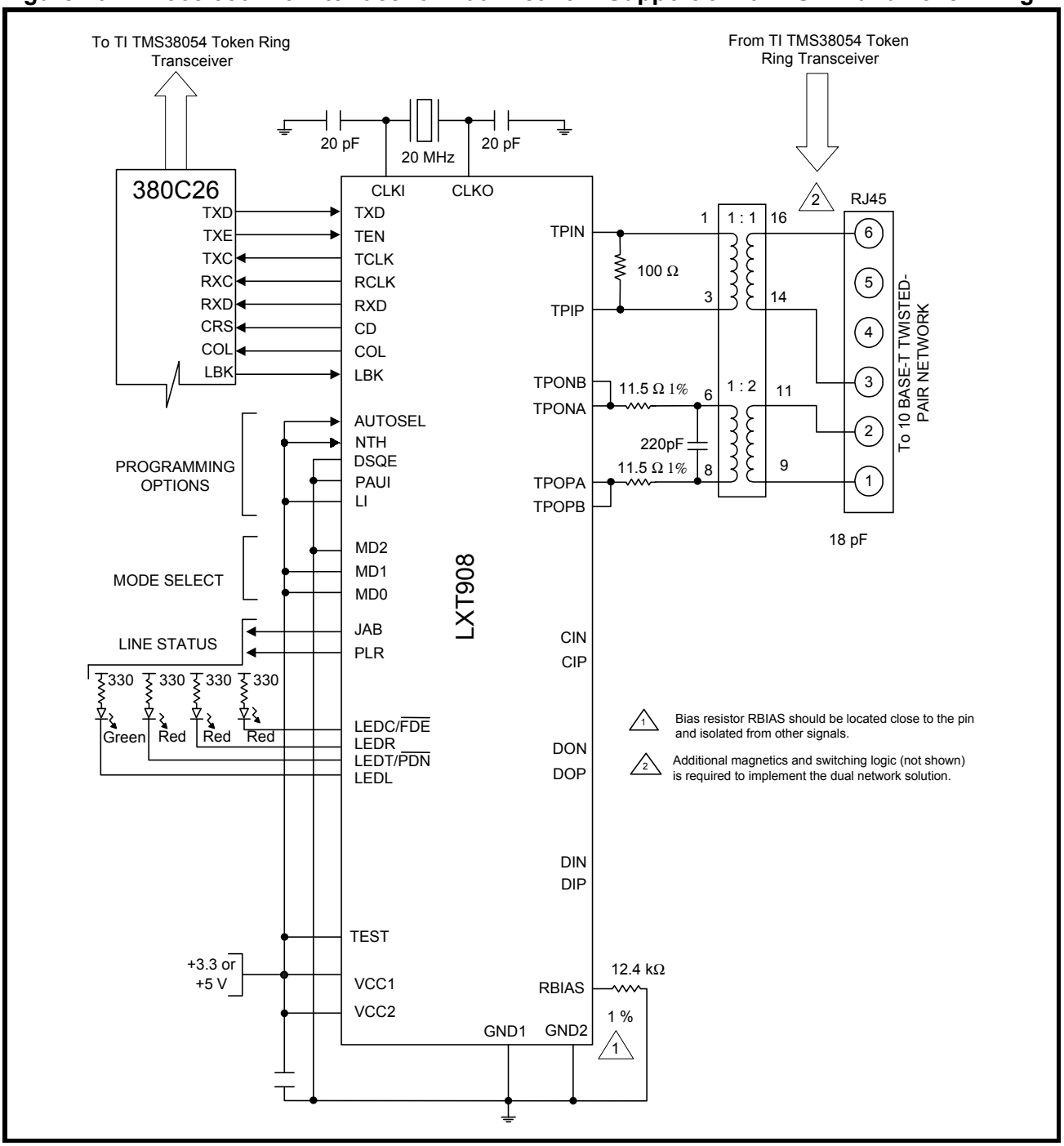
Figure 9: Full-Duplex Operation



Dual Network Support-10Base T and Token Ring

Figure 10 shows the LXT908 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD2:0 = Low, High, High). When used with the 380C26, both the LXT908 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector. The LXT908 AUI port is not used.

Figure 10: LXT908/380C26 Interface for Dual Network Support of 10BASE-T and Token Ring



Manual Port Select & Link Test Function

With MD2:0 = Low, High, Low, the LXT908 logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960, and Seeq 8005 controllers). Figure 11 shows the setup for Fujitsu controllers. Figure 12 shows the four inverters required to interface with the Seeq 8005 controller. As in Figure 8, both these Mode 3 applications show the LI pin tied High, enabling Link Testing; and the NTH and DSQE pins are both tied High, selecting the standard receiver threshold and disabling SQE. However, in these applications AUTOSEL is tied Low, allowing external port selection through the PAUI pin.

Figure 11: LAN Adapter Board - Manual Port Select with Link Test Function

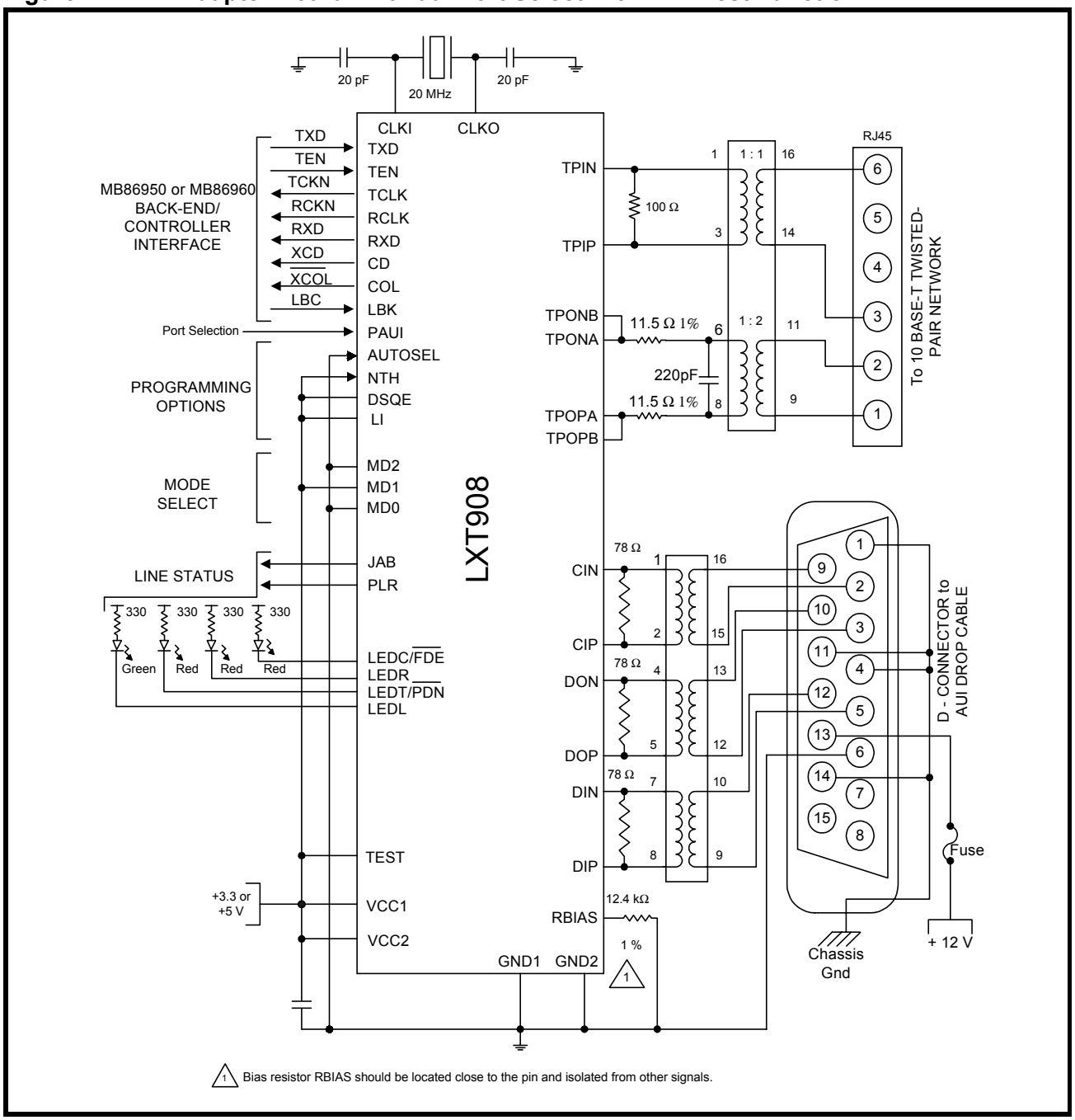
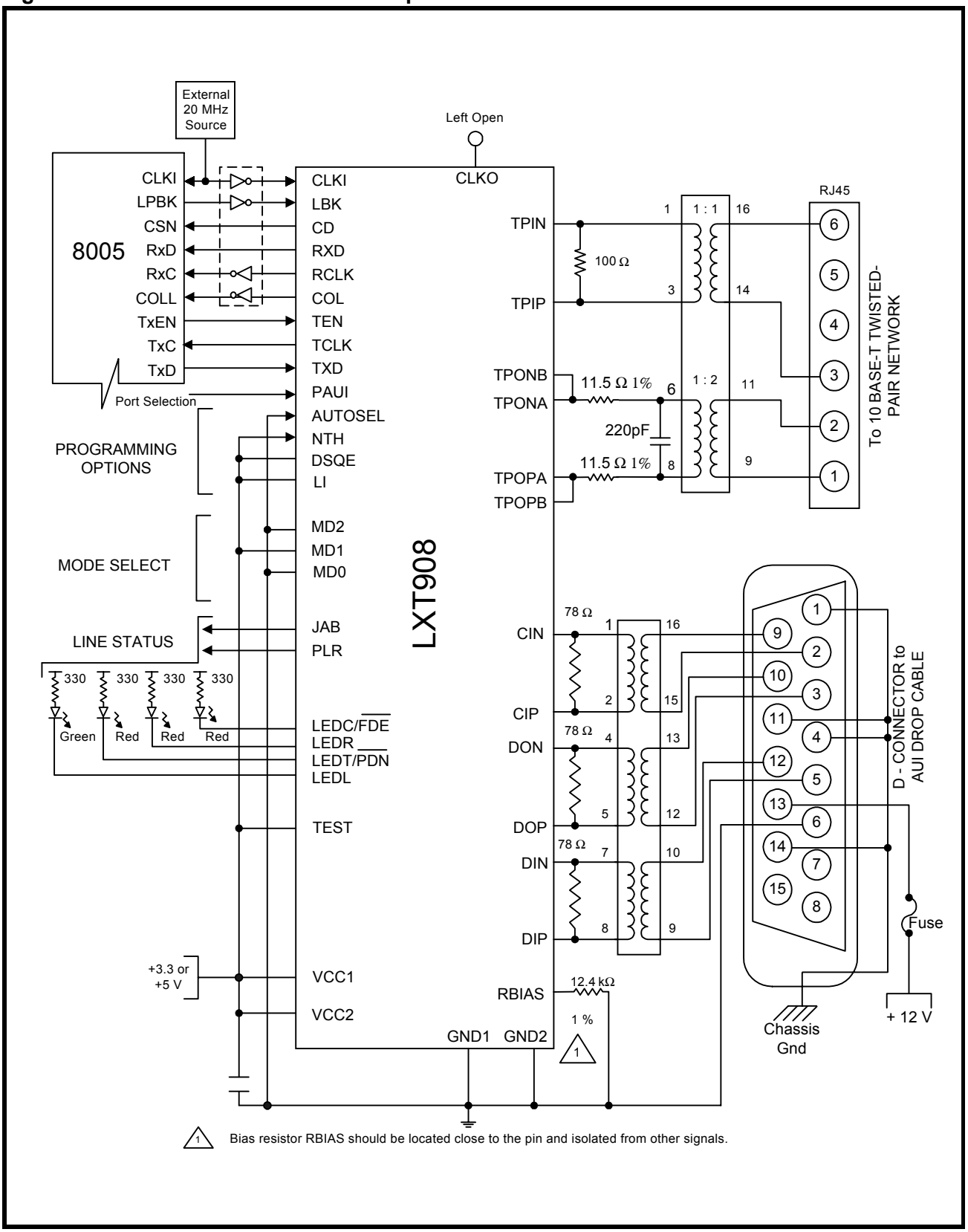


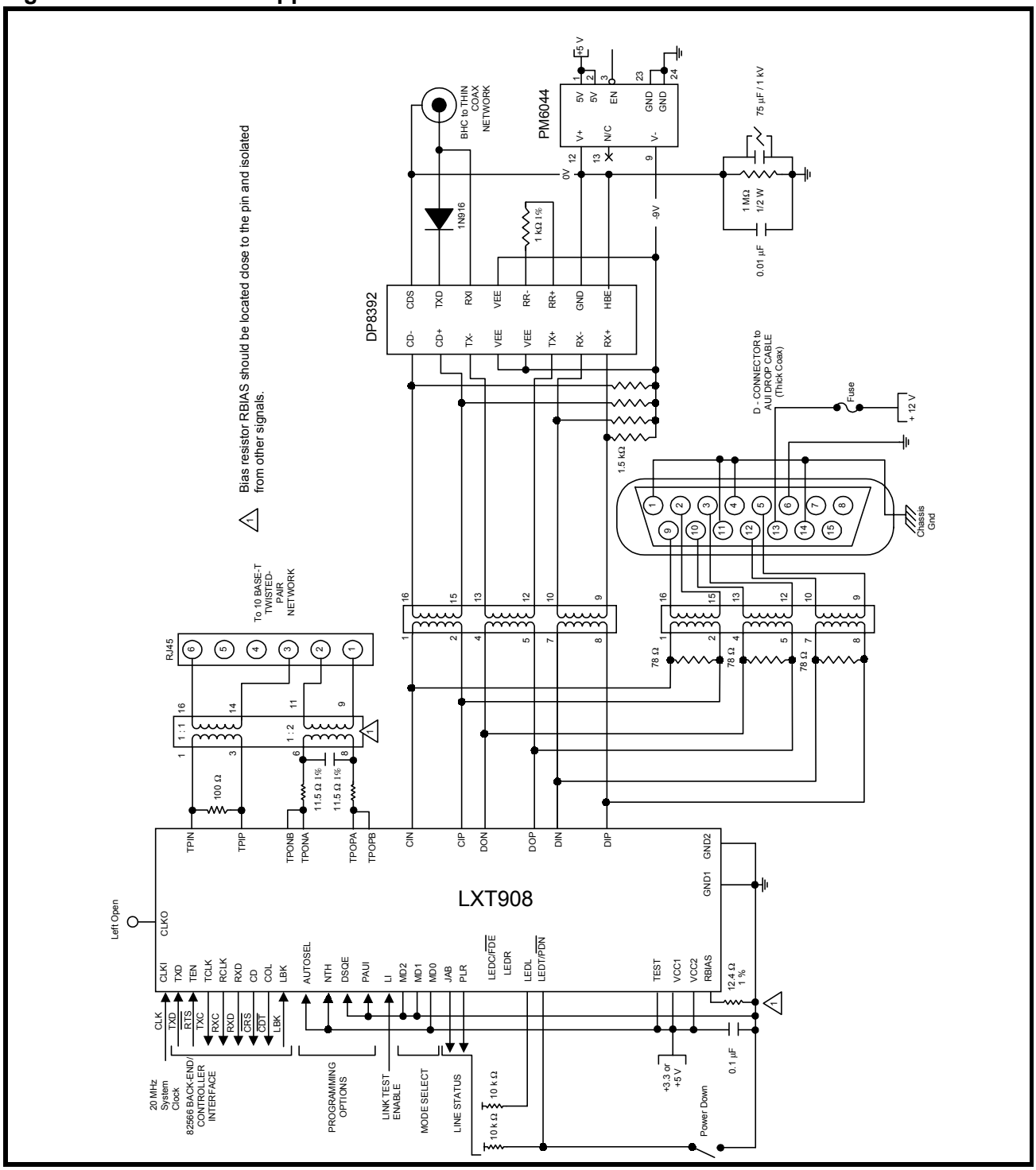
Figure 12: Manual Port Select with Seeq 8005 Controller



Three Media Application

Figure 13 shows the LXT908 in Mode 2 (compatible with Intel 82596 controllers) with additional media options for the AUI port. Two transformers are used to couple the AUI port to either a D-connector or a BNC connector. (A DP8392 coax transceiver with PM6044 power supply are required to drive the thin coax network through the BNC.)

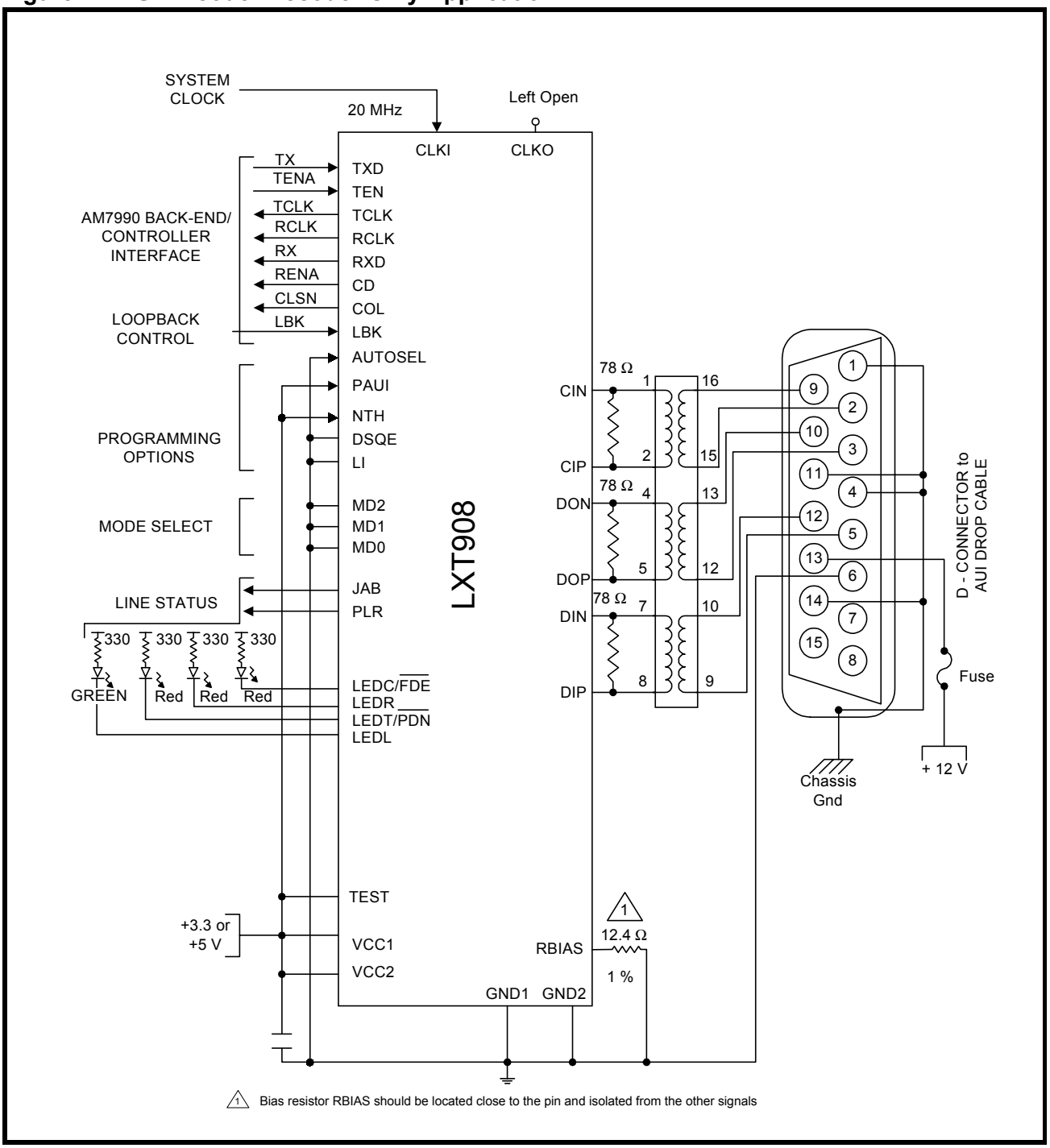
Figure 13: Three Media Application



AUI Encoder/Decoder Only

In the application shown in Figure 14, the DTE is connected to a coaxial network through the AUI. AUTOSEL is tied Low and PAUI is tied High, manually selecting the AUI port. The twisted-pair port is not used. With MD2:0 all tied Low, the LXT908 logic and framing are set to Mode 1 (compatible with AMD and Motorola controllers). The LI pin is tied Low, disabling the link test function. The DSQE pin is also Low, enabling the SQE function. The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

Figure 14: AUI Encoder/Decoder Only Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 14 and Figures 15 through 44 represent the performance specifications of the LXT908 and are guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Ambient operating temperature	TA	0	70	ºC
Storage temperature	TSTG	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	3.135	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	ºC	

1. Voltages with respect to ground unless otherwise specified.

Table 7: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]		VIL	–	–	0.8	V	
Input High voltage[2]		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage (Open drain LED driver)		VOLL	–	–	0.7	V	IOLL = 10 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output rise time TCLK & RCLK	CMOS	–	–	3	12	ns	CLOAD = 20 pF
	TTL	–	–	2	8	ns	
Output fall time TCLK & RCLK	CMOS	–	–	3	12	ns	CLOAD= 20 pF
	TTL	–	–	2	8	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 7: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–		40/60	%	
Supply current	Normal Mode	ICC	–	65	85	mA	Idle Mode
		ICC	–	95	120	mA	Transmitting on TP
		ICC	–	90	120	mA	Transmitting on AUI
	Power Down Mode	ICC	–	0.75	2	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V.

Table 8: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Differential squelch threshold	VDS	150	260	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 9: Twisted-Pair Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance		ZOUT	–	5	–	Ω	
Transmit timing jitter addition[2]		–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]		–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance		ZIN	–	20	–	kΩ	Between TPIP/TPIN, CIP/CIN & DIP/DIN
Differential Squelch Threshold	Normal Threshold NTH = High	VDS	300	395	585	mV	5 MHz square wave input
	Reduced Threshold NTH = Low	VDS	180	250	345	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 10: Switching Characteristics (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10/20	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time	AUI	tDATA	–	900	1100	ns
	TP	tDATA	–	1200	1500	ns
CD turn-on delay	AUI	tCD	–	25	200	ns
	TP	tCD	–	420	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2 through 5	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2 through 5	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3 and Mode 5)		tsws	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Units
RCLK after CD off	Min	tRC	5	1	–	5	–	BT
RXD throughput delay	Max	tRD	400	375	375	375	375	ns
CD turn off delay[2]	Max	tCDOFF	500	475	475	475	475	ns
Receive block out after TEN off	Typ[1]	tIFG	5	50	–	–	–	BT
RCLK switching delay after CD off (Mode 3 and 5)	Typ[1]	tSWE	–	–	120(±80)	–	120(±80)	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.

Table 13: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay - AUI	tSTUD	–	220	450	ns
Transmit start-up delay - TP	tSTUD	–	430	450	ns
Transmit through-put delay - AUI	tTPD	–	–	300	ns
Transmit through-put delay - TP	tTPD	–	305	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

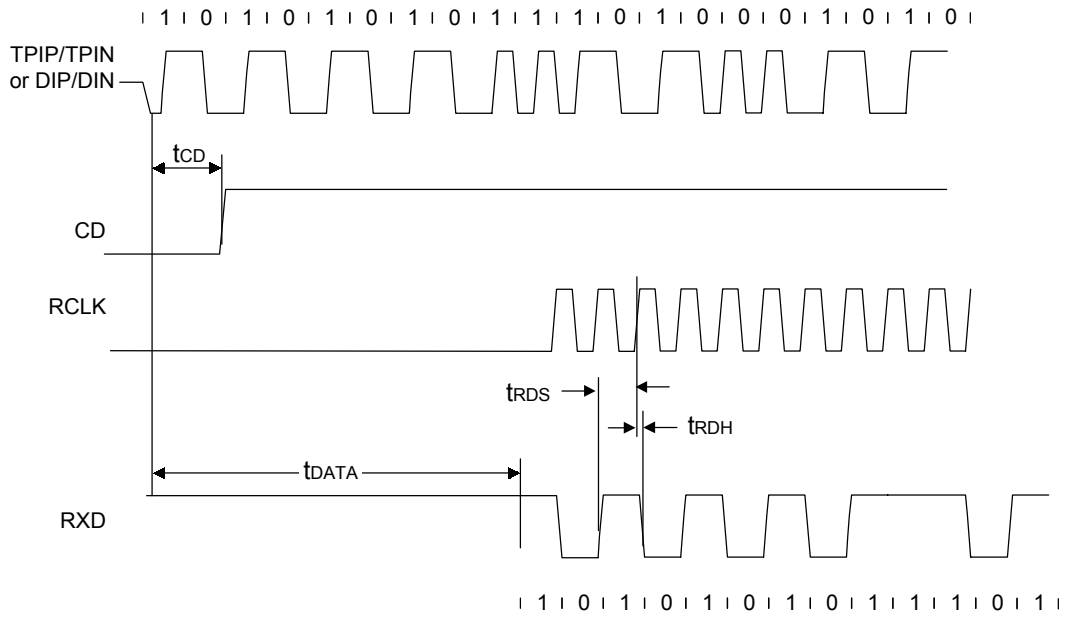
Table 14: Collision, COL/CI Output and Loopback Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL turn-on delay	tCOLD	–	40	500	ns
COL turn-off delay	tCOLOFF	–	420	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	1.2	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	1000	1500	ns
LBK setup from TEN	tKHEH	10	25	–	ns
LBK hold after TEN	tKHEL	10	0	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

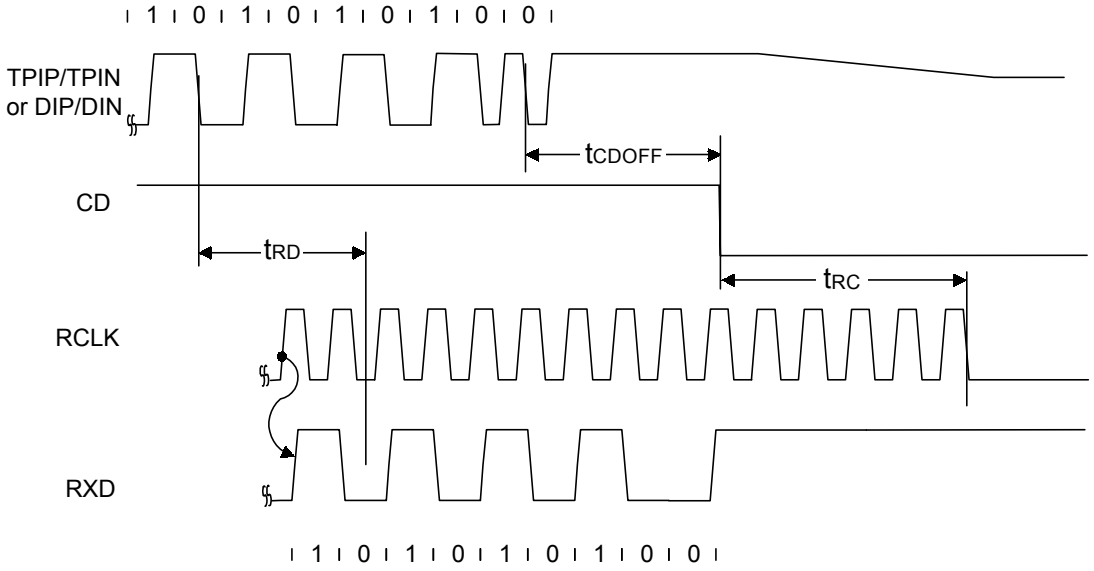
Timing Diagrams for Mode 1 *(MD2, 1, 0 = Low, Low, Low) Figures 15 through 20*

Figure 15: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 16: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 17: Mode 1 Transmit Timing

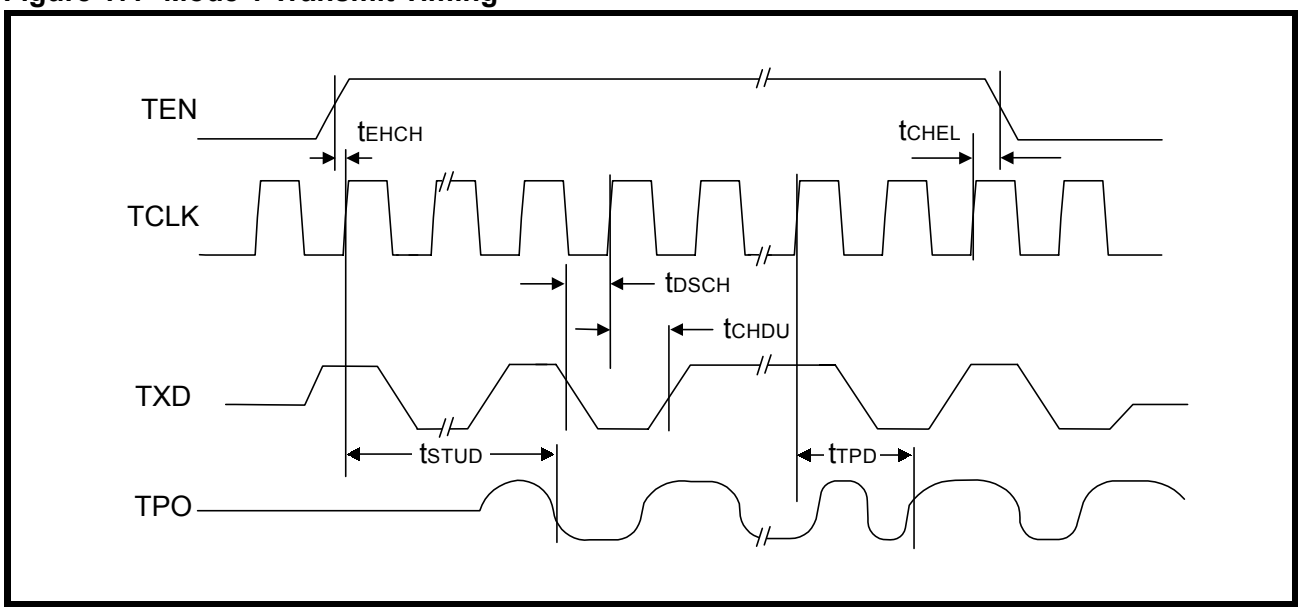


Figure 18: Mode 1 Collision Detect Timing

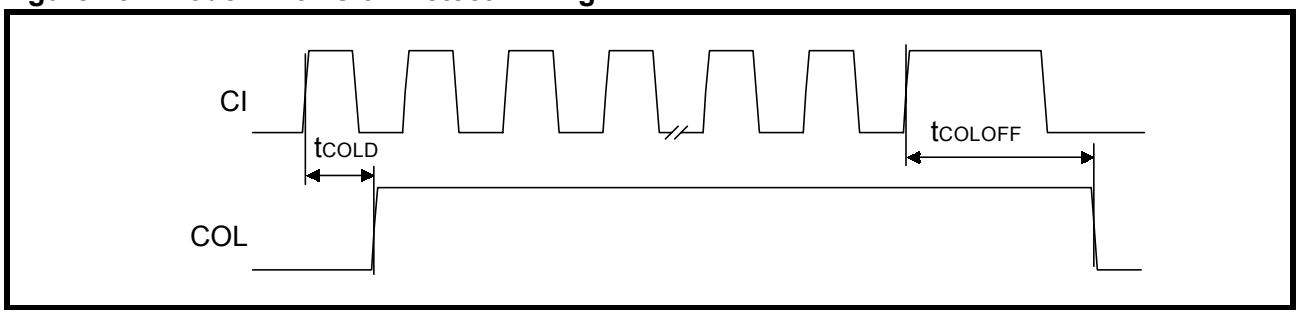


Figure 19: Mode 1 COL/SQE Output Timing/CI Output Timing

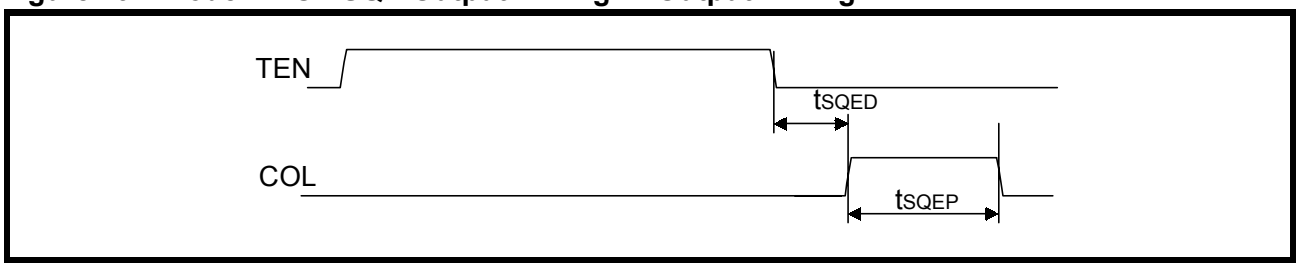
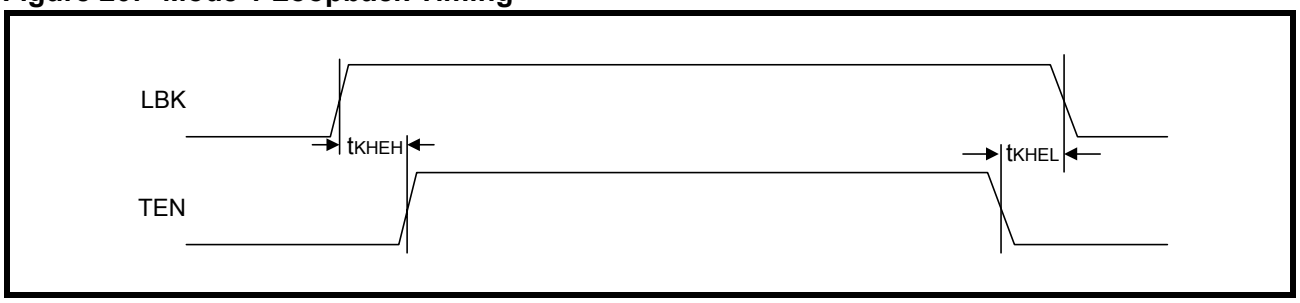
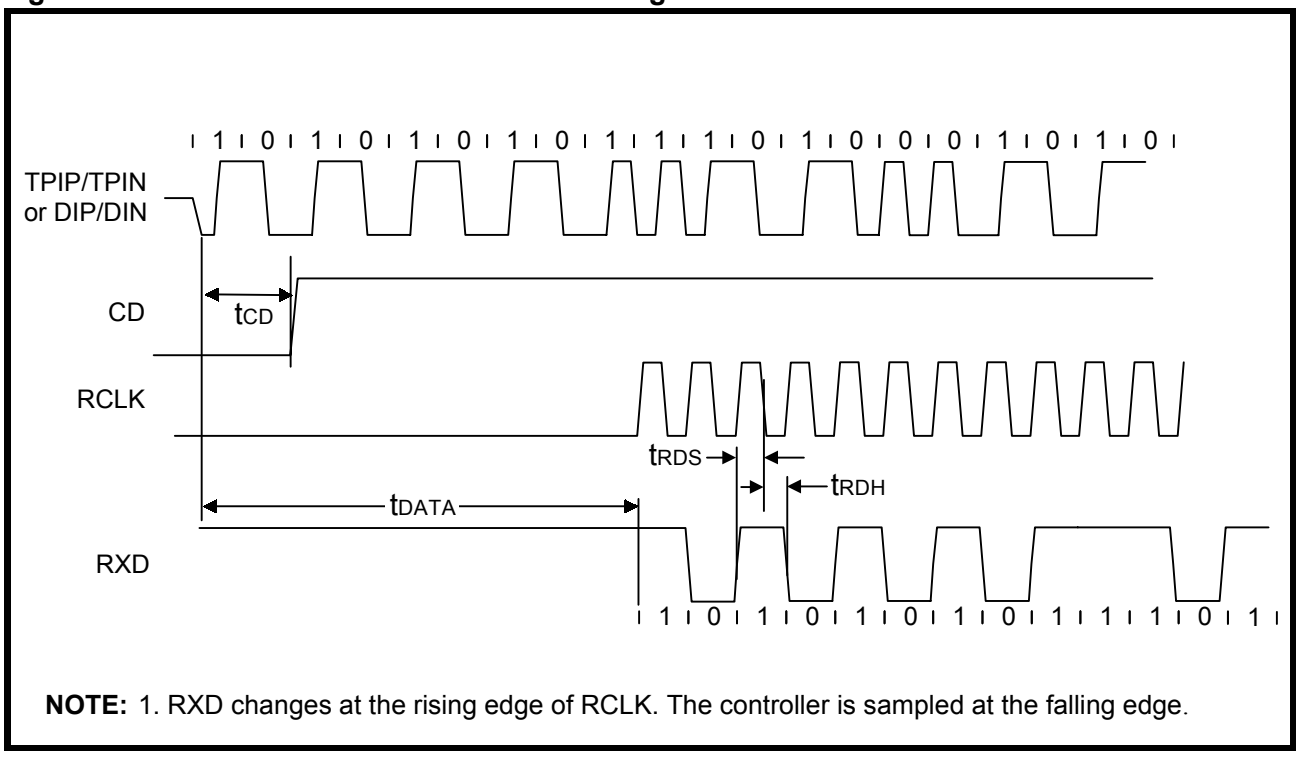


Figure 20: Mode 1 Loopback Timing



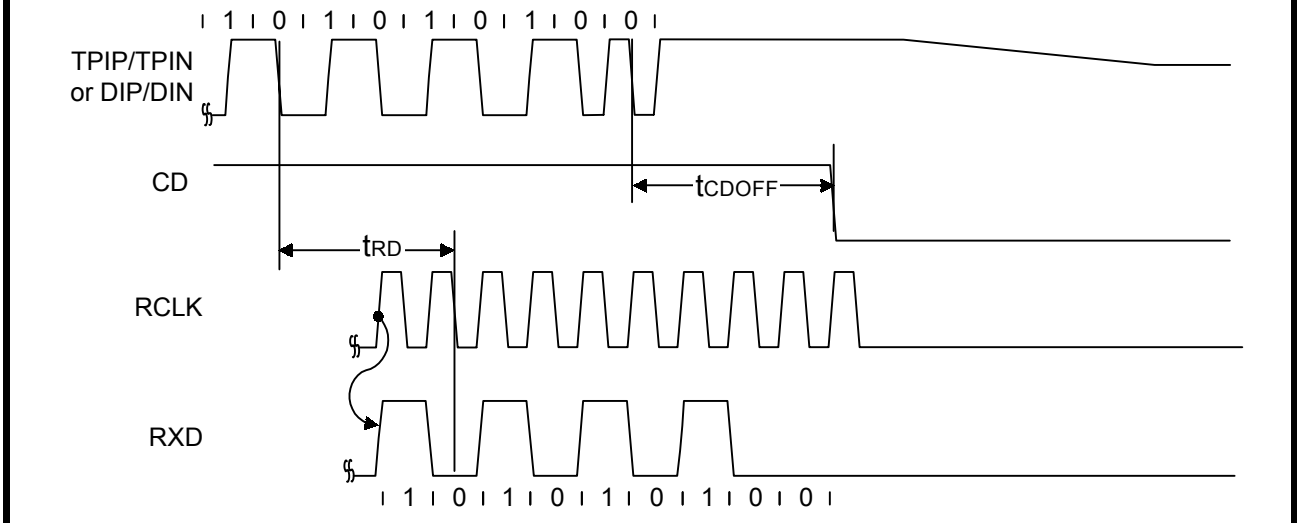
Timing Diagrams for Mode 2 *(MD2, 1, 0 = Low, Low, High) Figures 21 through 26*

Figure 21: Mode 2 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 22: Mode 2 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 23: Mode 2 Transmit Timing

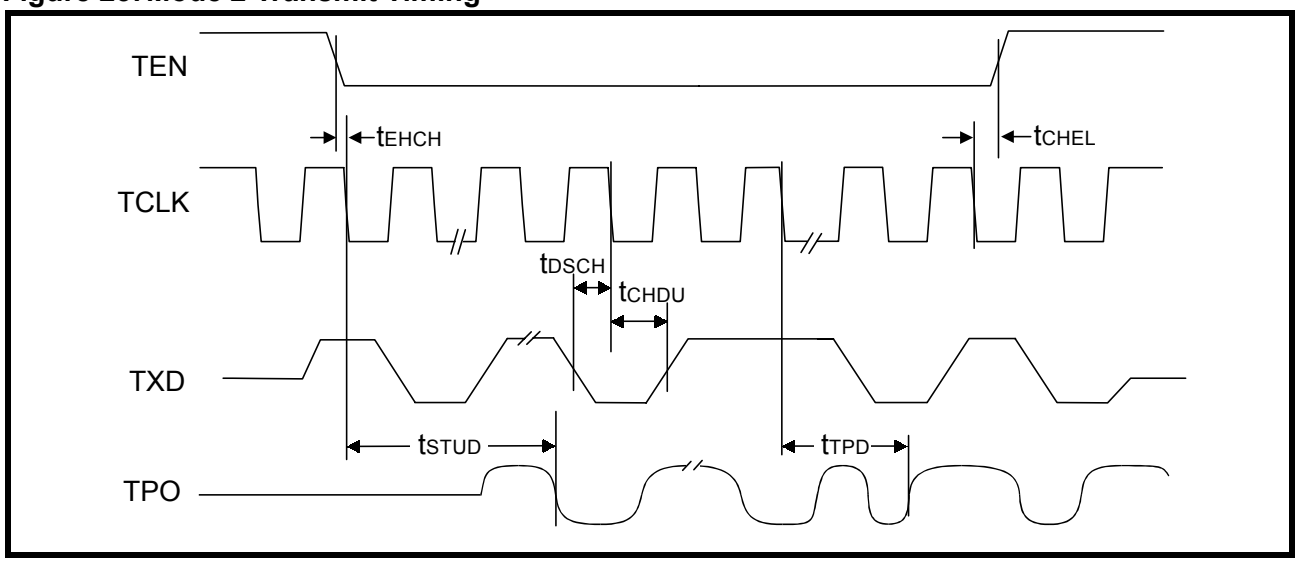


Figure 24: Mode 2 Collision Detect Timing

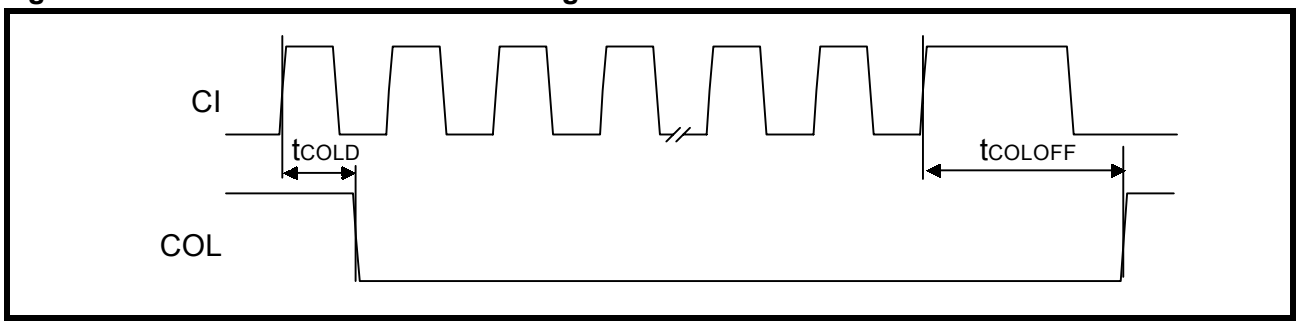
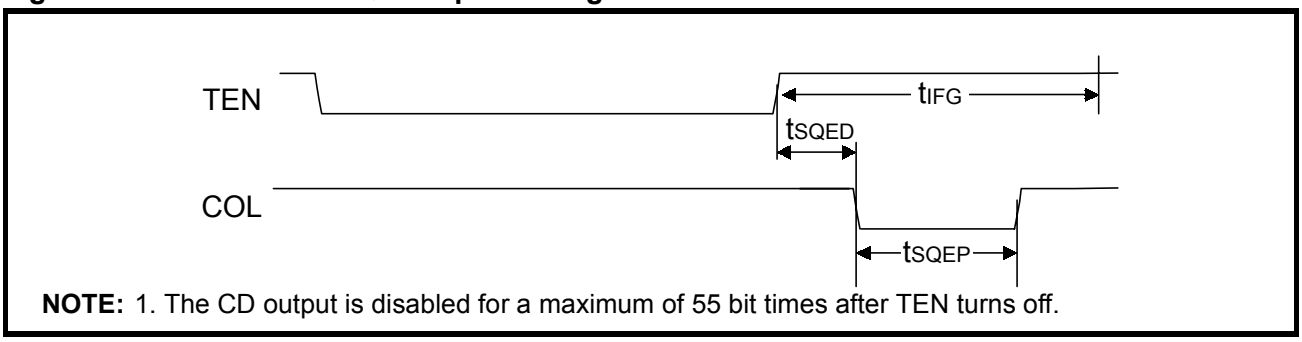
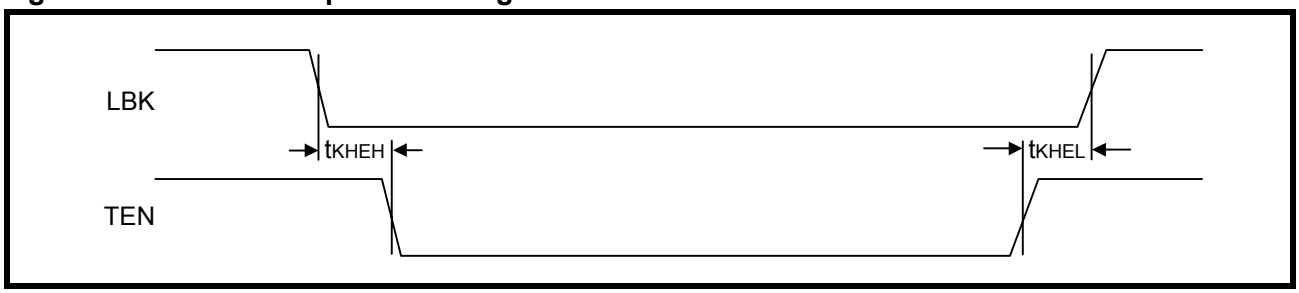


Figure 25: Mode 2 COL/SQE Output Timing



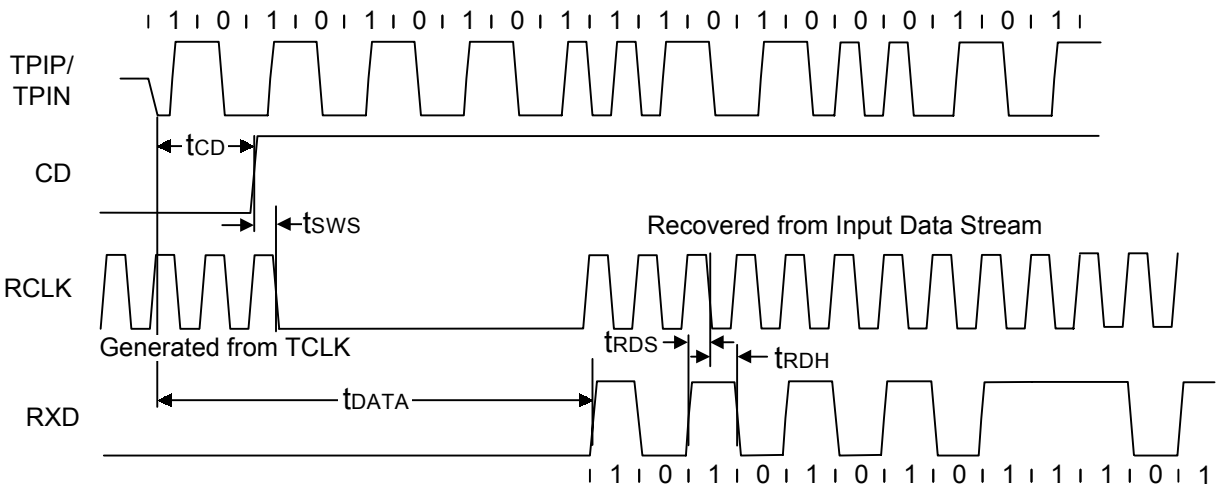
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 26: Mode 2 Loopback Timing



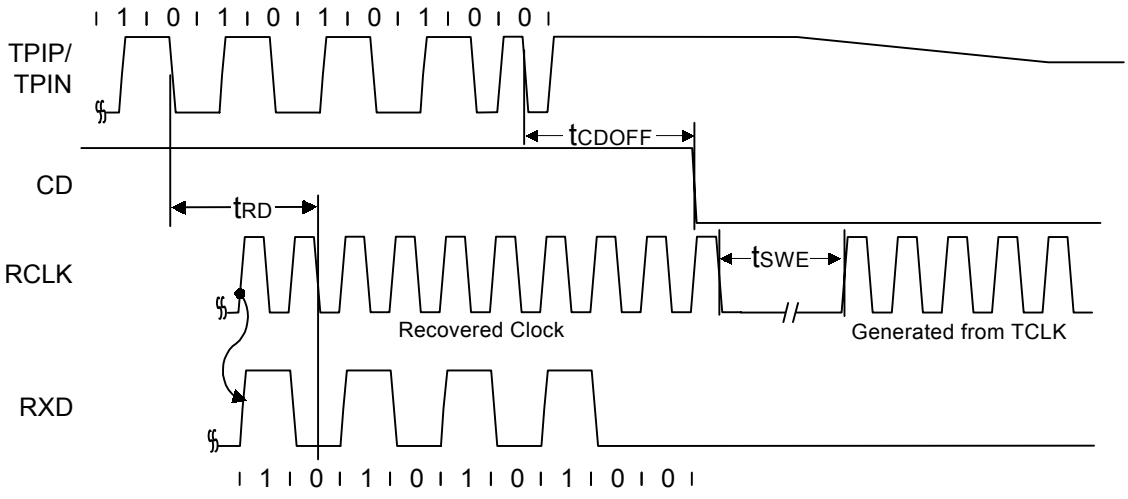
Timing Diagrams for Mode 3 *(MD2, 1, 0 = Low, High, Low) Figures 27 through 32*

Figure 27: Mode 3 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 28: Mode 3 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 29: Mode 3 Transmit Timing

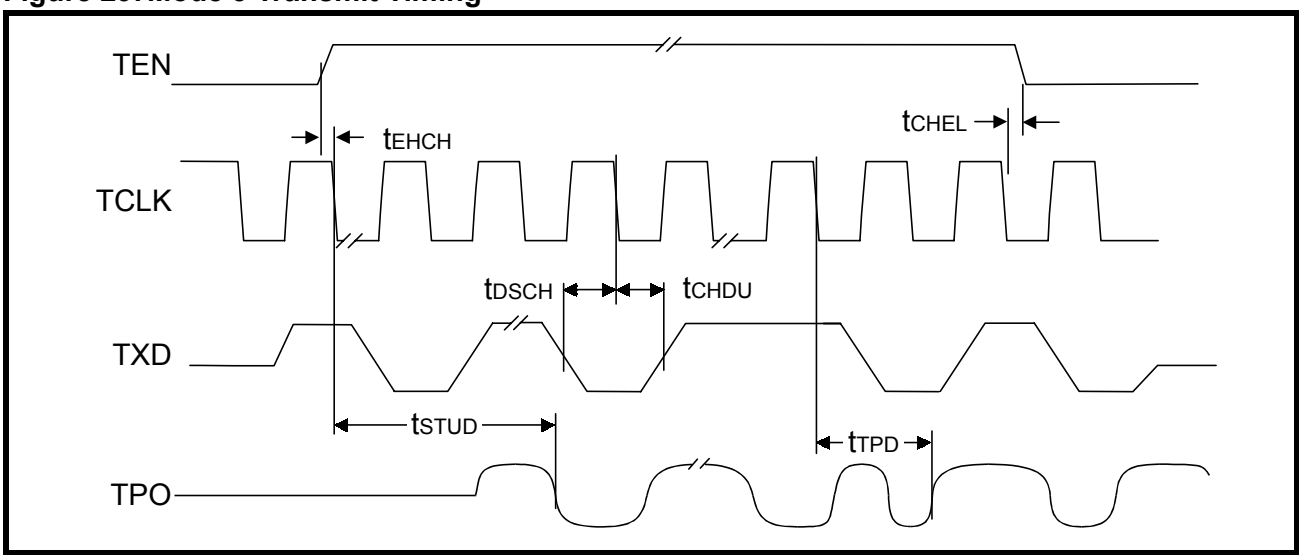


Figure 30: Mode 3 Collision Detect Timing

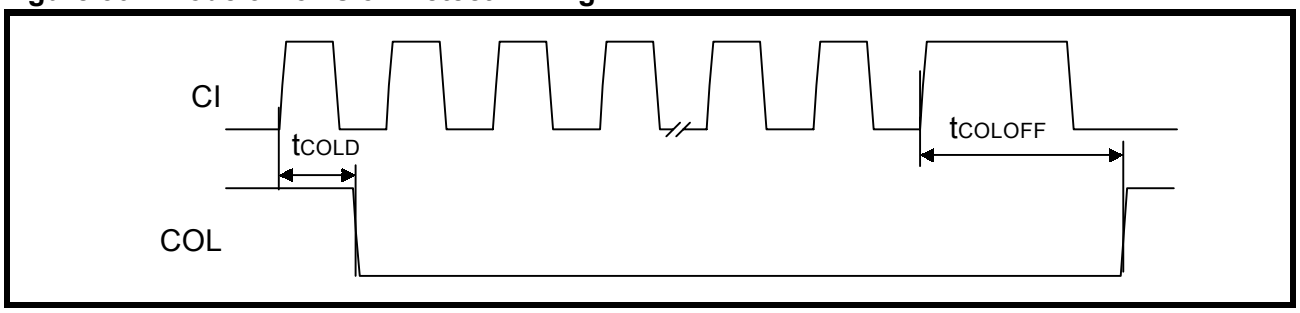
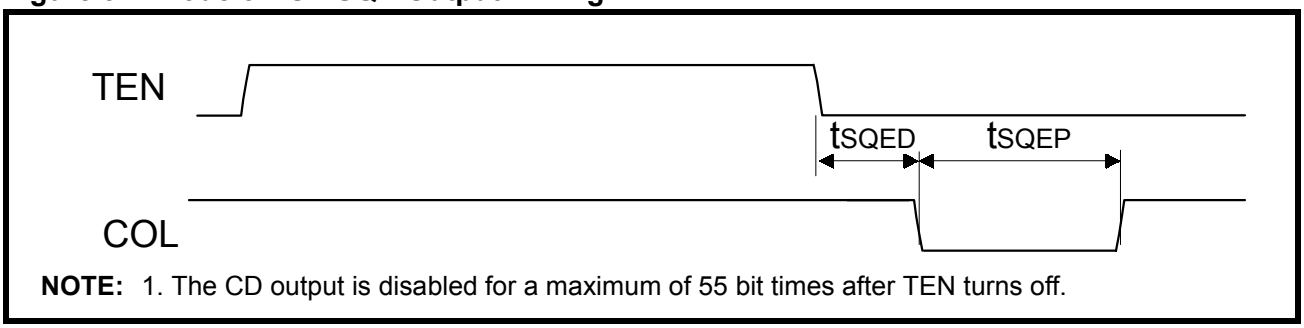
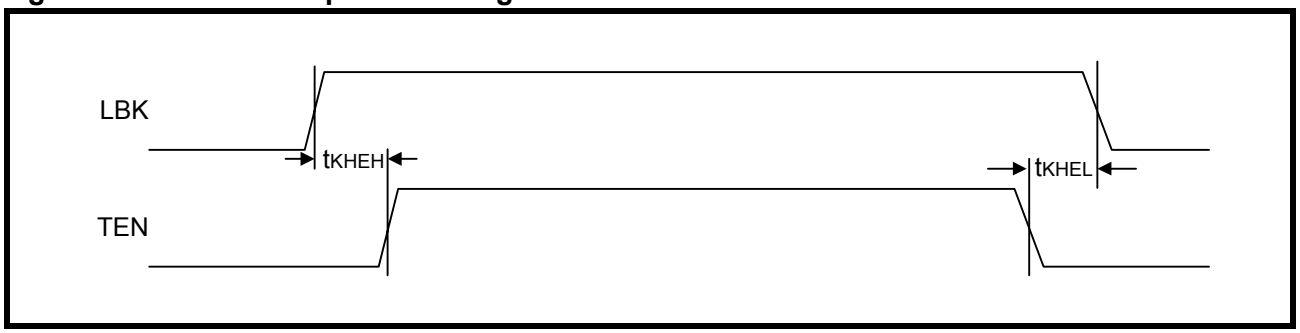


Figure 31: Mode 3 COL/SQE Output Timing



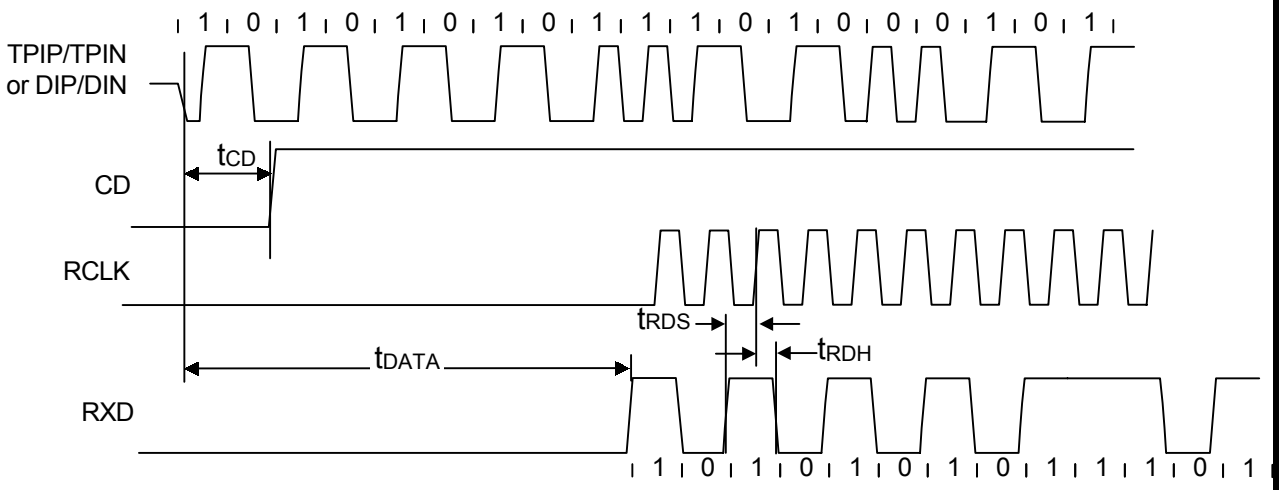
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 32: Mode 3 Loopback Timing



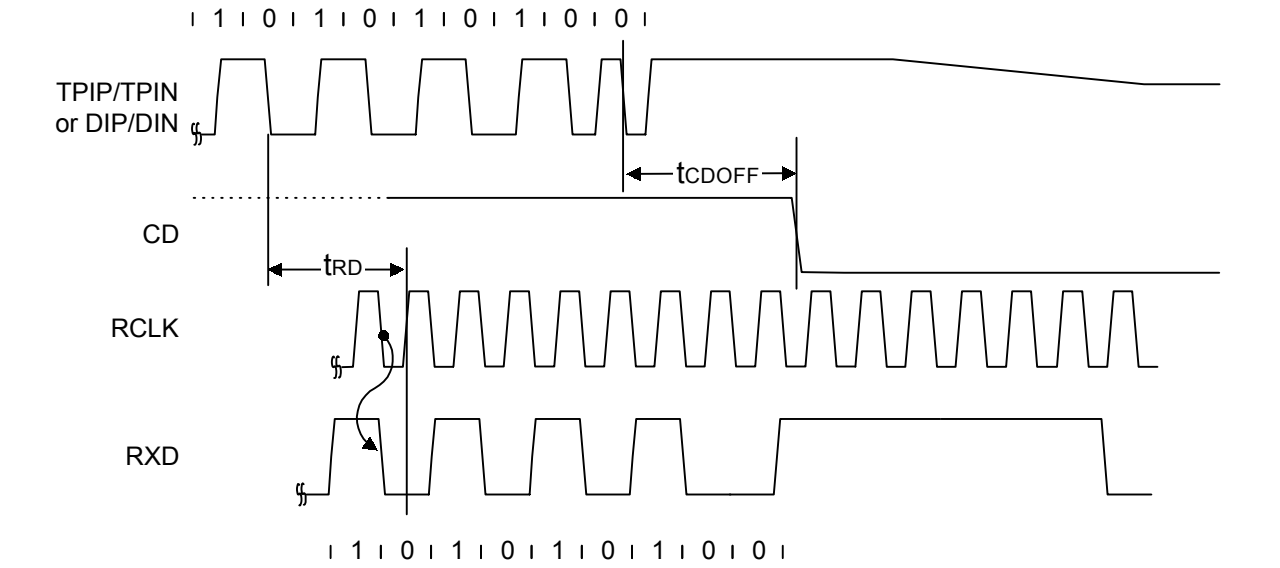
Timing Diagrams for Mode 4 *(MD2, 1, 0 = Low, High, High) Figures 33 through 38*

Figure 33: Mode 4 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 34: Mode 4 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 35: Mode 4 Transmit Timing

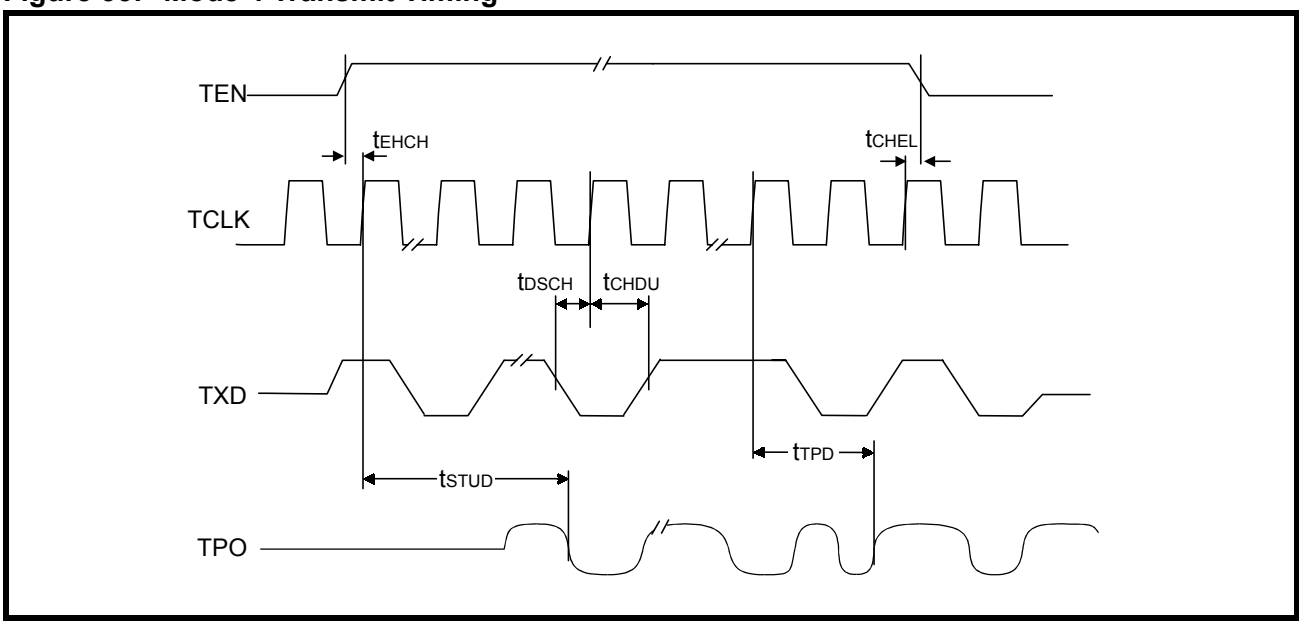


Figure 36: Mode 4 Collision Detect Timing

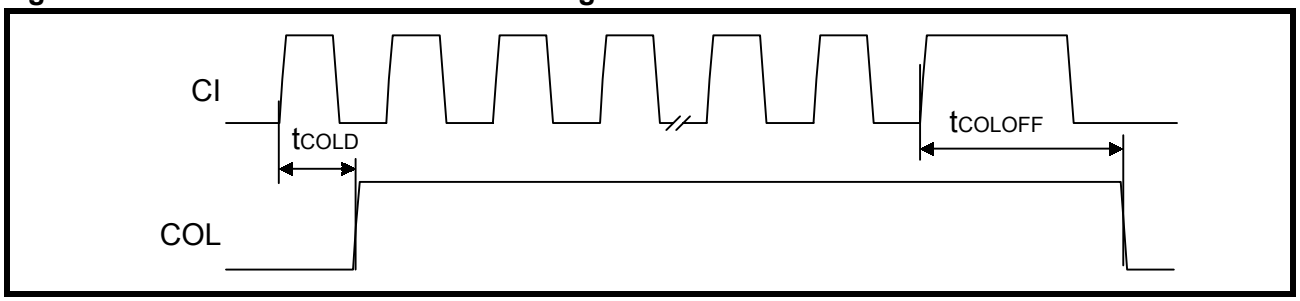


Figure 37: Mode 4 COL/SQE Output Timing

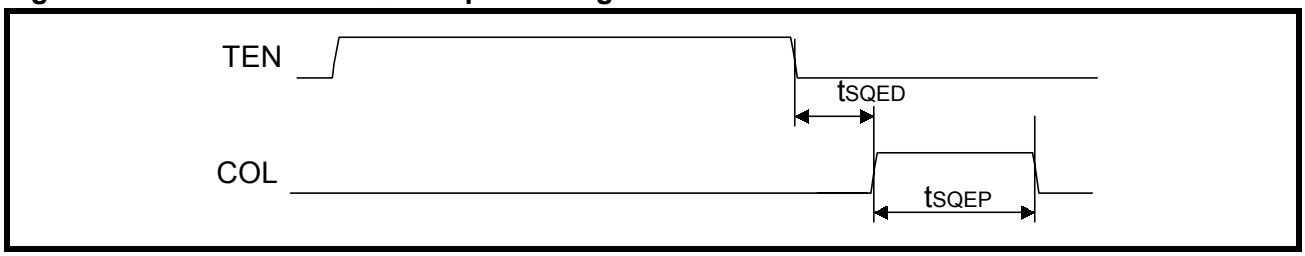
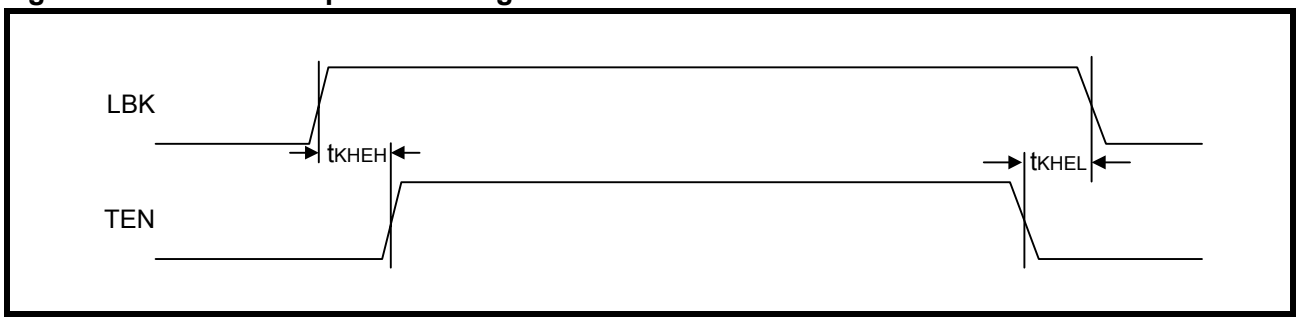
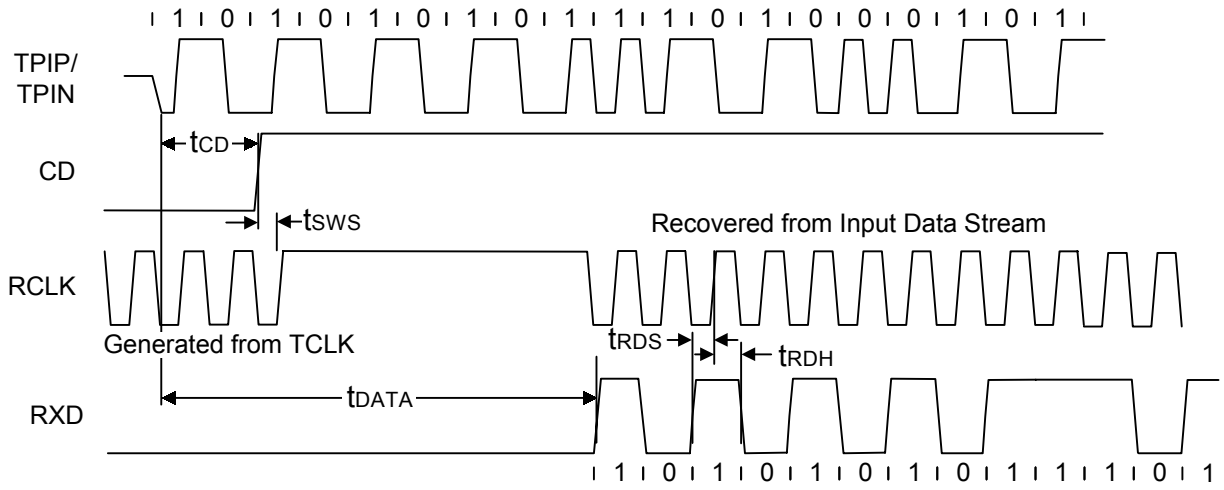


Figure 38: Mode 4 Loopback Timing



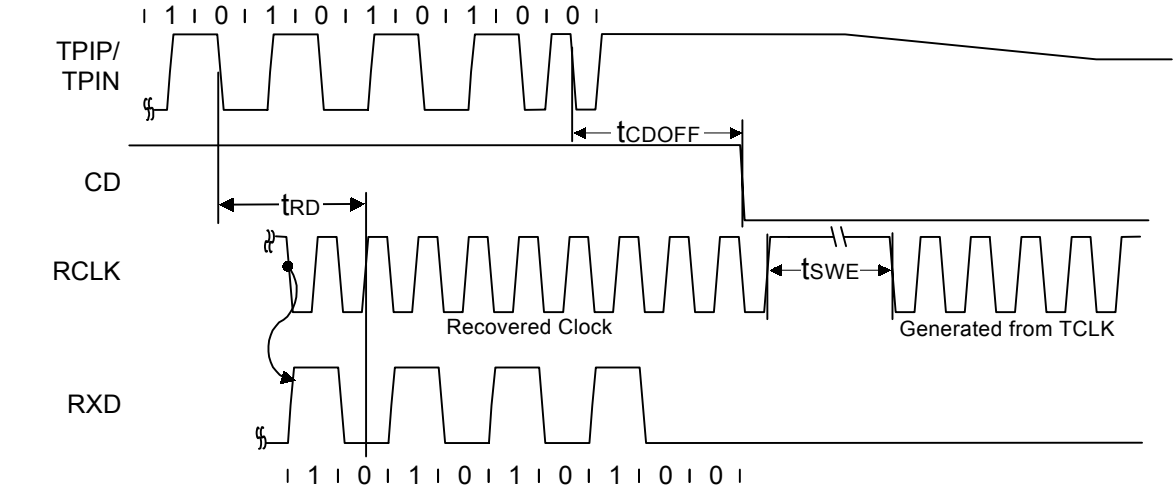
Timing Diagrams for Mode 5 *(MD2, 1, 0 = High, High, Low) Figures 39 through 44*

Figure 39: Mode 5 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 40: Mode 5 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 41: Mode 5 Transmit Timing

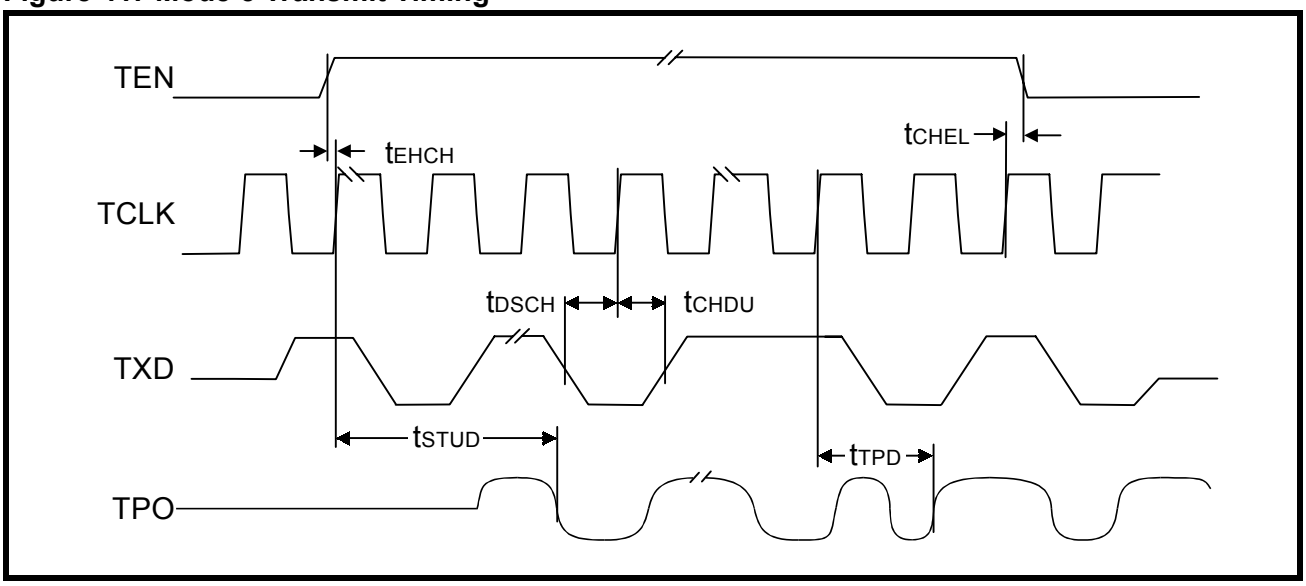


Figure 42: Mode 5 Collision Detect Timing

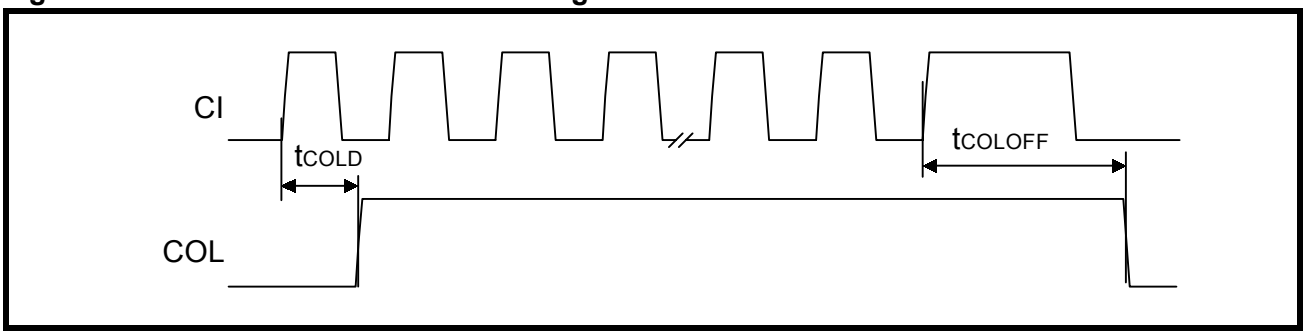


Figure 43: Mode 5 COL/SQE Output Timing

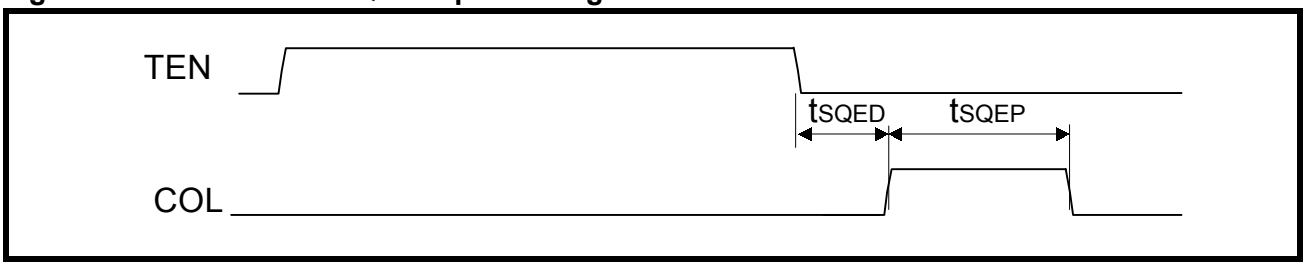
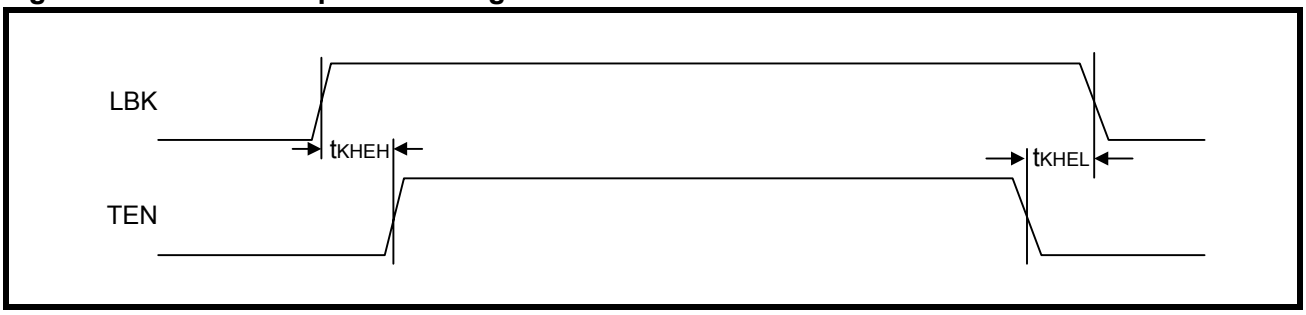


Figure 44: Mode 5 Loopback Timing



NOTES