PCS CDMA LNA / Downconverter 1.8—2.0 GHz

Features

- High Integrated LNA and Downconverter
- Operates over 2.7 V to 5V Supply Voltage
- Low Noise Figure < 2.7 dB
- High Input Intercept Point -12 dBm
- Optional Control of LNA IP_3
- Low LO Drive Level -10 dBm
- Operates in US and Korean PCS Bands
- Miniature TSSOP-16 Plastic Package

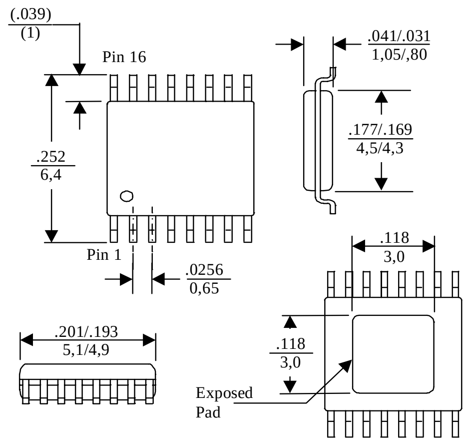
Description

M/A-COM's MD59-0021 is a fully integrated downconverter IC with LNA, RF amplifier, downconverting mixer, IF amplifier and LO buffer amplifier in a miniature TSSOP-16 plastic package with exposed metal lead frame backside for improved high frequency grounding.

The MD59-0021 is ideally suited for CDMA handset applications where wide dynamic range and low power consumption are important receiver requirements.

The MD59-0021 is fabricated using a M/A-COM's 0.5 micron low noise E/D GaAs MESFET process. The process features full passivation for increased performance and reliability.

TSSOP-16 Plastic Package[1]



1. Dimensions are: in / mm

Ordering Information

Part Number	Package
MD59-0021TR	Forward Tape and Reel[1]
MD59-0021RTR	Reverse Tape and Reel[1]
MD59-0021SMB	Sample Board

1. If specific reel size is required, consult factory for part number assignment.

Electrical Specifications T_A = 25°C, V_{DD} = 3.0V, RF = 1.9 GHz, LO = 1.69 GHz

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Low Noise Amplifier					
Gain	Frequency = 1.9 GHz	dB		14	
Noise Figure		dB		1.8	
VSWR In/Out				2:1	
Input IP_3		dBm		+6	
I_{DD}		mA		13	
Complete DownConverter[1]					
Conversion Gain		dB		22.5	25.4
Noise Figure	RF = 1.9 GHz	dB		2.7	
Input IP_3	LO = 1.69 GHz, LO Level = -10 dBm	dBm		-12	
LO-to-RF Isolation		dB		50	
LO-to-IF Isolation		dB		24	
I_{DD}	IF = 210 MHz	mA		32	

1. Complete downconverter measurements taken with 3 dB pad between LNA output and RFA input.

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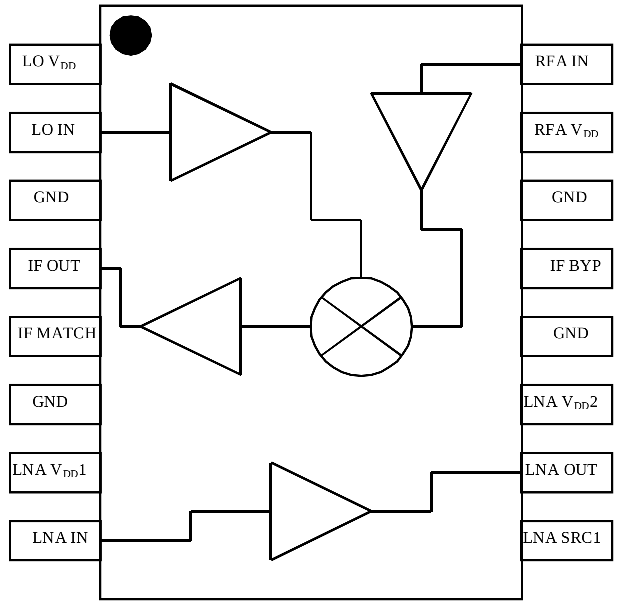
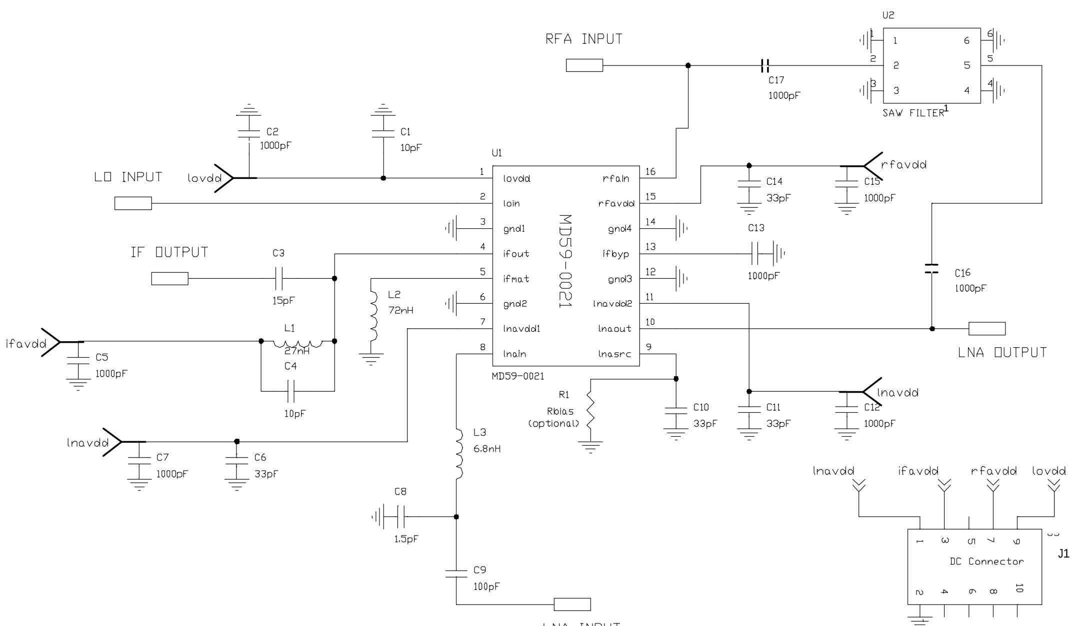
Pin Configuration

PIN No.	PIN	Description
1	LO V_{DD}	LO Amplifier Supply Voltage. RF bypassing required.
2	LO In	Local Oscillator Input (-10 to -7 dBm) (DC blocked)
3	GND	DC and RF ground
4	IF Out	IF Output and Downconverter - must be externally matched to input impedance of IF Filter.
5	IF Match	Matching between I FA and Mixer - requires an inductor to ground.
6	GND	DC and RF ground
7	LNA V_{DD}1	LNA Stage 1 supply voltage. RF bypassing required.
8	LNA In	RF Input to LNA. External matching required.
9	LNA SRC	Source of LNA output stage FET. RF bypassing required. Off-chip resistor may be used to increase IP_3.
10	LNA Out	50Ω Output of LNA. (DC Blocked)
11	LNA V_{DD}2	LNA Stage 2 supply voltage. RF bypassing required.
12	GND	DC and RF ground.
13	IF BYP	IF Bypass of Mixer. Required DC block and RF/IF ground.
14	GND	DC and RF ground
15	RFA V_{DD}	RFA supply voltage. RF bypassing required.
16	RFA In	50Ω Input of RFA. (DC blocking required)

Block Diagrams



Sample Board Schematic



1. Saw filter characteristics to be determined by customer, depending on band of operation. Sample boards are supplied with 3 dB pi pad installed in place of saw filter, to emulate typical worst case loss. Data supplied with sample board is measured over US PCS1900 Rx Band.

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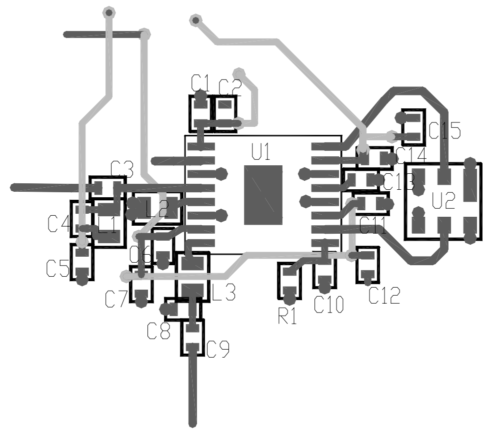
V 2.0

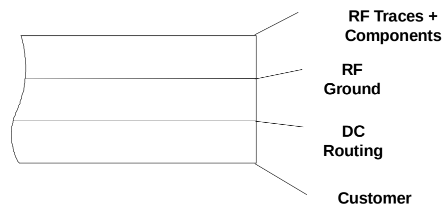
External Circuitry Parts List

Ref. Designation	Value	Purpose
C6, C10, C11, C14	33 pF	RF Bypass
C2, C5, C7, C12, C13, C15-C17	1000 pF	RF / IF Bypass
C3	15 pF	IF Matching
C1, C4	10 pF	Bypass, IF Matching
C8	1.5 pF	LNA Input Matching
C9	100 pF	RF Bypass
L1	27 nH	IF Matching
L2	72 nH	IF Amplifier Input Matching
L3	6.8 nH	LNA Input Matching
R1	R_{bias}	Optional resistor to increase bias current in LNA
U1		MD59-00021 LNA/Downconverter
U2	Saw Filter	Filter TX signals and image
J1	DC Connect	10 PIN DC Connector

Recommended PCB Configuration



Cross Section View



Operating Instructions

The MD59-0021 is a highly integrated MMIC downconverter for the 1.8-2 GHz PCS band. The downconverter provides exceptional RF performance while consuming low DC current and is packaged in a low cost plastic package. It is ideal for light weight battery operated portable radio systems.

The receive chain consists of an LNA, RFA, balanced mixer and single-ended IF output buffer amplifier as shown in the block diagram. Surface mount resistors, inductors and capacitors are used in conjunction with the IC for optimum performance, tunability and ease of use. A schematic showing the IC and required external components is shown on the previous page.

The input of the LNA is matched externally with a series inductor (L3) and a shunt capacitor (C8) to provide a low loss match to the optimum noise impedance in the band of interest. A high Q inductor such as Coilcraft's 0603CS series must be used if the specified noise figures are to be achieved. The series capacitor C9 is a DC blocking capacitor whose value is not critical (it should be ≥ 100pF) The LNA is nominally biased with 13 mA to give an input IP3 of +6 dBm. An external resistor R1, may be used to increase the LNA bias current and thus increase the IP3. An external image reject filter is required between the LNA output and RFA input to prevent downconversion of noise at the image frequency to the IF. This filter should have a 50Ω input and output impedance.

The mixer is a balanced resistive FET mixer which provides exceptional linearity and isolation with low loss and no DC current. An off-chip inductor, L, is required to match the output of the mixer to the input of the IF buffer amplifier.

The IF output port is the open drain of the IF buffer amplifier. This allows maximum flexibility of intermediate frequency and also IF filter characteristics. A matching network such as that shown on page 2 can be used to match from the output impedance of the buffer to the input impedance of the filter at the required frequency. The inductor also acts as a choke for the DC supply line.

The LO input port is internally matched to 50Ω. An LO buffer amplifier amplifies the -10 dBm input signal to the level required to drive the mixer. Performance is optimum with a drive level of -5 dBm

All DC supply lines must be properly bypassed at RF frequencies to obtain optimum performance and at lower frequency to maintain unconditional stability. Capacitors C1, C6, C11 and C14 are RF bypass capacitors for the LNA, RFA and LOA. The value and placement of these capacitors are critical in determining the frequency response of these amplifiers. Capacitor C10 is a source bypass capacitor for the second stage of the low noise amplifier. The placement of this capacitor will affect the gain of the LNA. For best performance, all the RF bypass capacitors should be placed as shown in the PCB drawing shown above. Capacitors C2, C5, C7, C12, C13 and C15 are 1000 pF low frequency DC supply bypass capacitors. Their value and placement are less critical than the other capacitors. However, for best results, these capacitors should be located as close to the package leads as possible.

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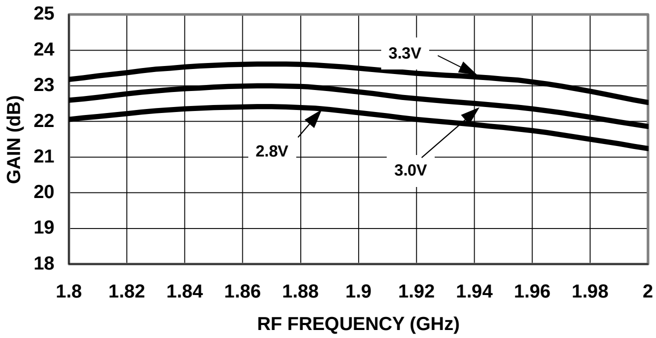
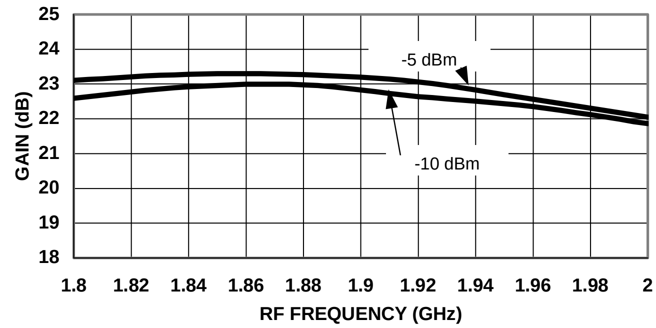
Typical Performance Curves LNA/Downconverter (with 3dB Pad in place of Image Reject Filter)

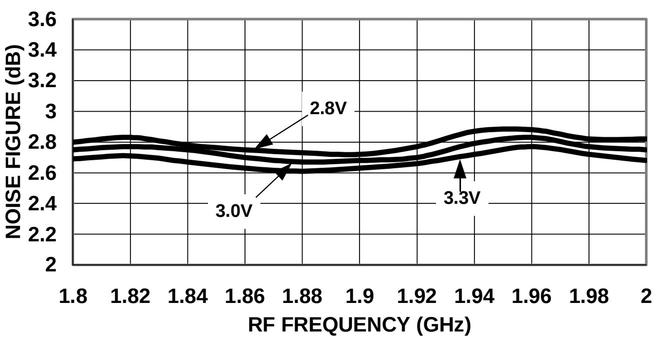
Conversion Gain vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = -10dBm



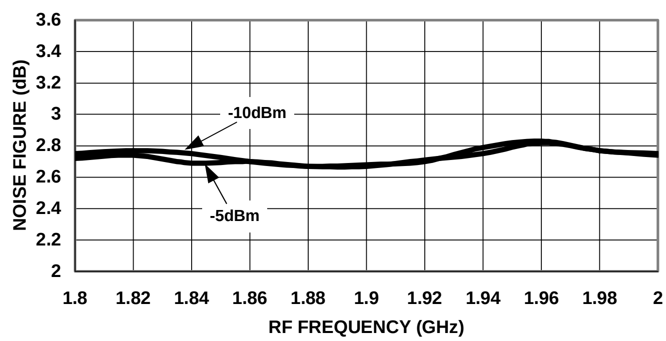
Conversion Gain vs. Frequency
LO = -10 dBm, -5 dBm, V_{DD} = 3.0V



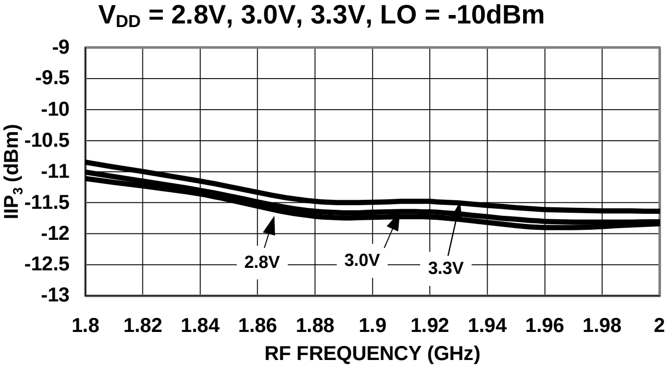
Noise Figure vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = -10dBm



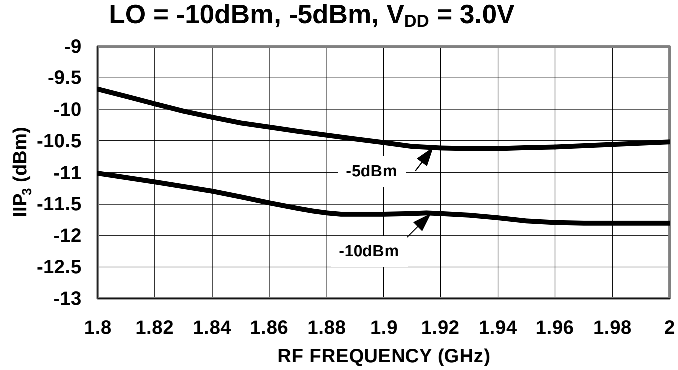
Noise Figure vs. Frequency
LO = -10dBm, -5dBm, V_{DD} = 3.0V



Input IP_3 vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = -10dBm



Input IP_3 vs. Frequency
LO = -10dBm, -5dBm, V_{DD} = 3.0V



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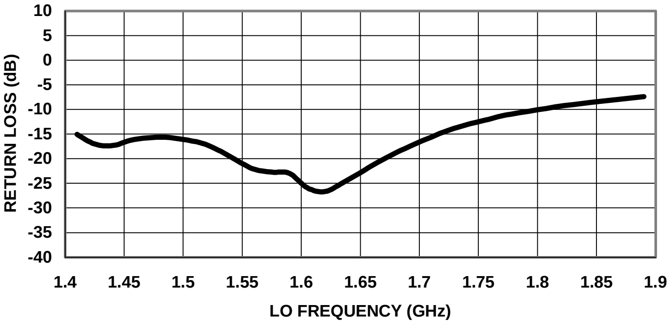
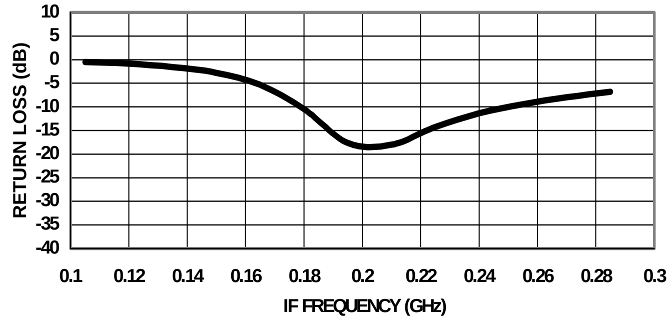
Typical Performance Curves LNA/Downconverter (with 3dB Pad in place of Image Reject Filter) Cont'd)

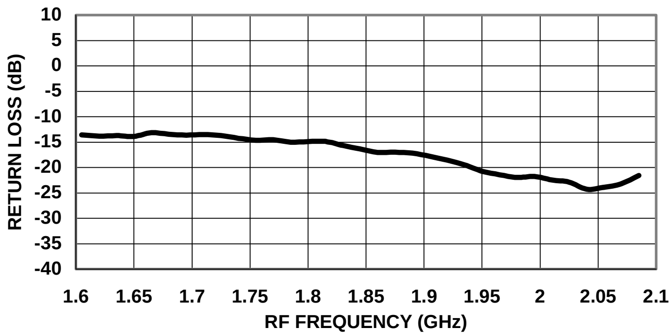
LO Input Return Loss vs. Frequency
LO = -10dBm, V_{DD} = 3.0V



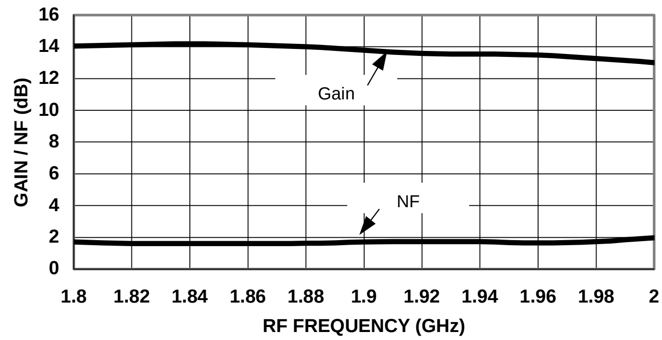
IF Output Return Loss vs. Frequency
LO = -10dBm, V_{DD} = 3.0V



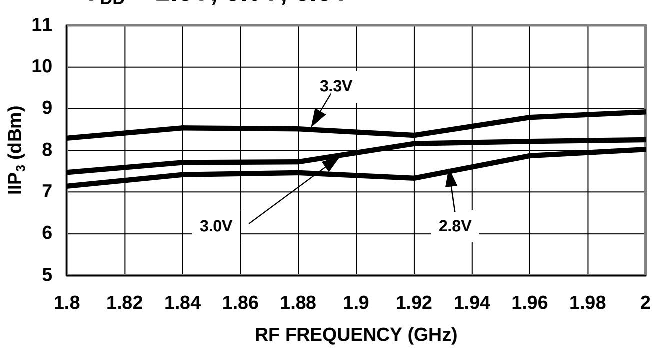
Downconverter Input Return Loss vs. Frequency LO = -10dBm, V_{DD} = 3.0V



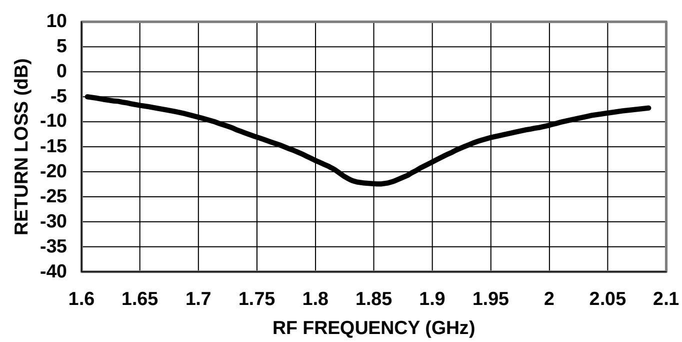
LNA Gain, Noise Figure vs. Frequency
V_{DD} = 3.0V



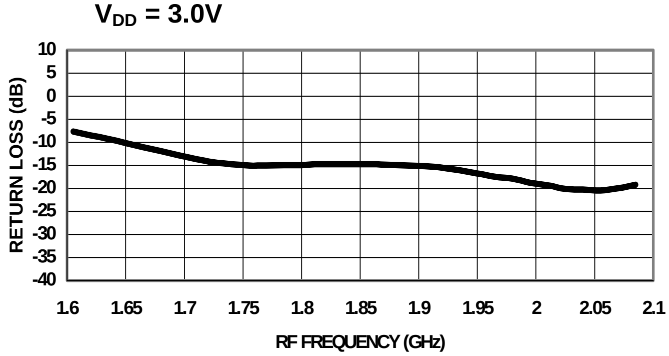
LNA Input IP_3 vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V



LNA Input Return Loss vs. Frequency
V_{DD} = 3.0V



LNA Output Return Loss vs. Frequency
V_{DD} = 3.0V



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