

GaAs Foundry Services

PROCESS PE3

PE3

V2.00

Features

- 0.5 μm MBE MESFET Technology for High Power Applications
- MMICs up to 18 GHz
- 100 mm wafer diameter
- Layout and design assistance
- Space qualification
- Custom test and packaging

Description

M/A-COM's PE3 process utilizes molecular beam epitaxy (MBE) to implement a MESFET active layer structure that achieves high efficiency and breakdown for multi-watt power applications thru 18GHz. The focus is on products for moderate to high volume applications. M/A-COM offers a full compliment of foundry services to meet the requirements for custom designing a MMIC-based die or packaged product.

Typical RF Performance

FC06 (6X150) 900 μm FET

Param.	Test Conditions	Freq.	Typ. Val.
MAG	$V_{DS} = 8V, I_{DS} = .40I_{DSS}$	2/12GHz	22/13.5dB
P_{SAT}	$V_{DS} = 8V, I_{DS} = .40I_{DSS}$	2/12GHz	680/525mW/mm
PAE	$V_{DS} = 8V, I_{DS} = .40I_{DSS}$	2/12GHz	50/41%
ft	$V_{DS} = 8V, I_{DS} = .40I_{DSS}$	-----	20GHz

Ordering Information

Part Number	Description
FE43-0001	PE3 Wafer
SVC6310	Mask Set

Electrical Specifications: $T_A = +25\text{ }^\circ\text{C}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
200 μm PCM FET					
IDSS	$V_{DS} = 3V, V_{GS} = 0V$	mA/mm	180	240	310
DC GM	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	mS/mm	125	150	185
Vp	$V_{DS} = 3V, I_{DS} = 0.025IDSS$	V	-1.2	-1.8	-2.2
BVgd	$I_G = 0.1\text{mA/mm}$	V	-11	-15	-
RF GM	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	mS	25	32	45
Cgs	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	pF	.140	.200	.280
Cgd	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	pF	.015	.022	.028
Cds	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	pF	.025	.038	.050
Ft	$V_{DS} = 3V, I_{DS} = 0.5IDSS$	GHz	20	26	34
Sheet Resistances					
NDRS (N- GaAs)	$I = 20\text{mA}$	Ohms/sq	340	375	410
NCRS (NiCr)	$I = 10\text{mA}$	Ohms/sq	42	50	58
GFRS (Gate Metal)	$I = 20\text{mA}$	Ohms/sq	-	.027	.040
MIM Capacitors					
Capacitance/unit area	$f = 1\text{MHz}$	pF/mm^2	360	400	440
Capacitor Leakage	$V = 10V$	μA	-	-	0.5

Specifications Subject to Change Without Notice.

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Normalized Nominal Models

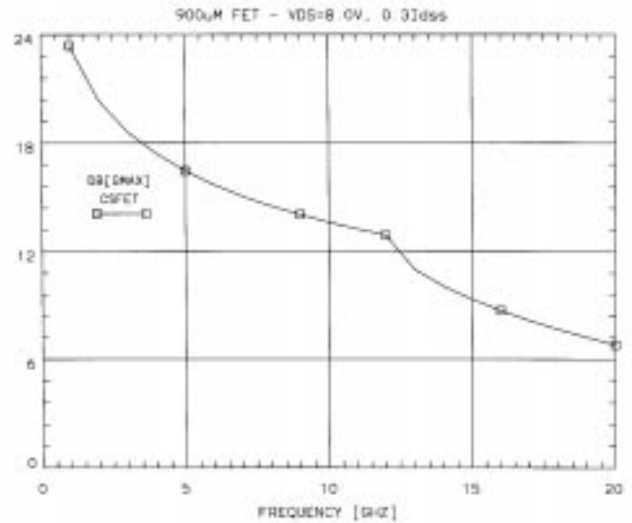
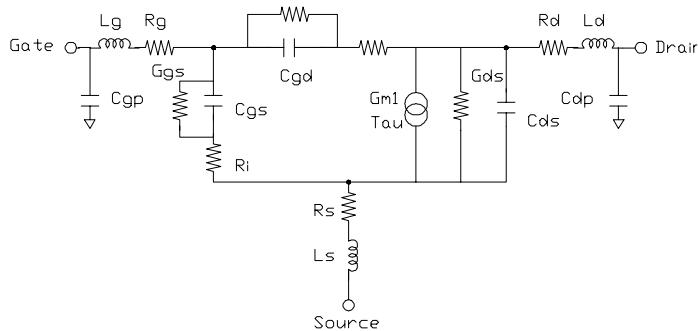
Parameter	25% I _{DSS} 8 V _{DS}	50% I _{DSS} 8 V _{DS}
I _{DS} mA/mm	62.62	127.96
g _m mS/mm	140.37	155.44
C _{gs} pF/mm	1.178	1.303
C _{gd} pF/mm	0.072	0.059
C _{ds} pF/mm	0.172	0.185
T _d pS	5.574	5.502
R _i Ohms-mm	2.093	1.729
G _{ds} mS/mm	9.214	7.929
G _{gs} mS/mm	0.168	0.093
R _g Ohms/mm	47.996	47.996
R _s Ohms-mm	0.827	0.827
R _d Ohms-mm	0.865	0.865
L _g nH/Finger	0.108	0.108
L _d nH/Finger	0.108	0.108
C _{gp} pF/mm	0.148	0.148
C _{dp} pF/mm	0.148	0.148

Mask Layer Assignments

LAYER	PROCESS CODE	PROCESS DESCRIPTION
3	OH	Ohmic
4	BI	Boron Isolation
5	RD	Resistor Deposition
7	GF	Gate Finger
8	GL	Gate Interconnect
10	TV	Top via
11	OL	Overlay
12	AP	Air-post
13	AS	Air-Span
25	BV	Back-via
28	FP	Final Passivation
29	ST	Saw Street

NOTE: Unused layer numbers are reserved for future use.

GMAX - 900um FET



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