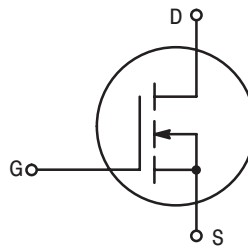


The RF MOSFET Line  
**RF Power**  
**Field-Effect Transistors**  
N-Channel Enhancement-Mode

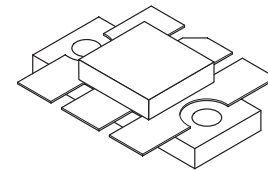
Designed for broadband commercial and military applications using single ended circuits at frequencies to 400 MHz. The high power, high gain and broadband performance of each device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance  
MRF175LU @ 28 V, 400 MHz ("U" Suffix)  
Output Power — 100 Watts  
Power Gain — 10 dB Typ  
Efficiency — 55% Typ  
MRF175LV @ 28 V, 225 MHz ("V" Suffix)  
Output Power — 100 Watts  
Power Gain — 14 dB Typ  
Efficiency — 65% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low  $C_{RSS}$  — 20 pF Typ @  $V_{DS} = 28$  V



**MRF175LU**  
**MRF175LV**

100 W, 28 V, 400 MHz  
N-CHANNEL  
BROADBAND  
RF POWER FETs



CASE 333-04, STYLE 2

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Vdc
Drain Current — Continuous	$I_D$	13	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	270 1.54	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 50$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28$ V, $V_{GS} = 0$ )	$I_{DSS}$	—	—	2.5	mAdc
Gate-Body Leakage Current ( $V_{GS} = 20$ V, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

(continued)

**Handling and Packaging** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ V}$ , $I_D = 100\text{ mA}$ )	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ V}$ , $I_D = 5.0\text{ A}$ )	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$ )	$g_{fs}$	2.0	3.0	—	mhos

**DYNAMIC CHARACTERISTICS**

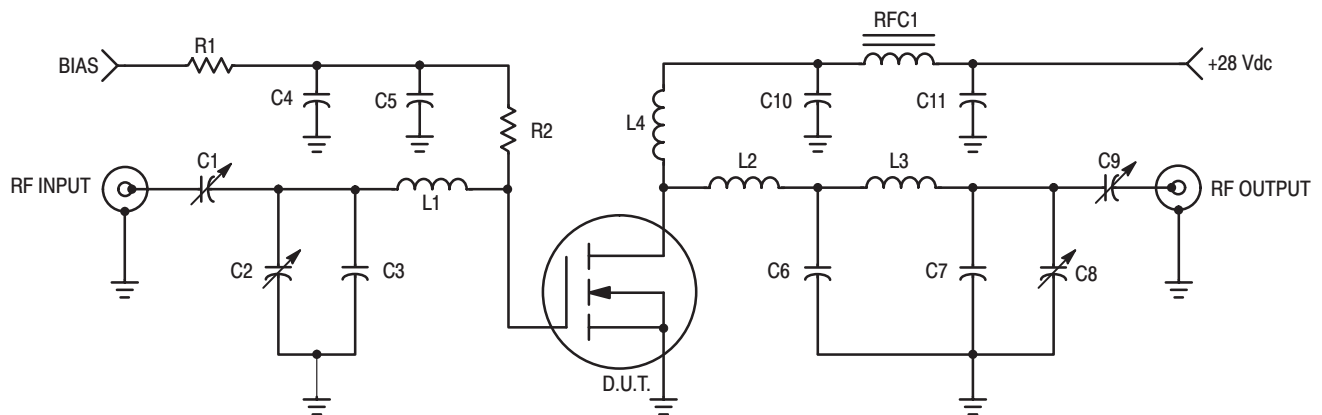
Input Capacitance ( $V_{DS} = 28\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	—	180	—	pF
Output Capacitance ( $V_{DS} = 28\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{oss}$	—	200	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28\text{ V}$ , $V_{GS} = 0$ , $f = 1.0\text{ MHz}$ )	$C_{rss}$	—	20	—	pF

**FUNCTIONAL CHARACTERISTICS — MRF175LV (Figure 1)**

Common Source Power Gain ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ )	$G_{ps}$	12	14	—	dB
Drain Efficiency ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ )	$\eta$	55	65	—	%
Electrical Ruggedness ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 225\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ , VSWR 30:1 at all Phase Angles)	$\psi$	No Degradation in Output Power			

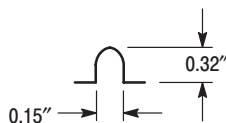
**FUNCTIONAL CHARACTERISTICS — MRF175LU (Figure 2)**

Common Source Power Gain ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ )	$G_{ps}$	8.0	10	—	dB
Drain Efficiency ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ )	$\eta$	50	55	—	%
Electrical Ruggedness ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 100\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DQ} = 100\text{ mA}$ , VSWR 30:1 at all Phase Angles)	$\psi$	No Degradation in Output Power			



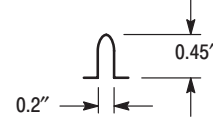
C1, C2, C8 — Arco 463 or Equivalent  
 C3, C7 — 25 pF Unelco Cap  
 C4 — 1000 pF Chip Cap  
 C5 — 0.01  $\mu\text{F}$  Chip Cap  
 C6 — 250 pF Unelco Cap  
 C9 — Arco 462 or Equivalent  
 C10 — 1000 pF ATC Chip Cap  
 C11 — 10  $\mu\text{F}$  100 V Electrolytic

L1 — Hairpin Inductor #18 Wire



L2 — Stripline Inductor 0.200" x 0.500"

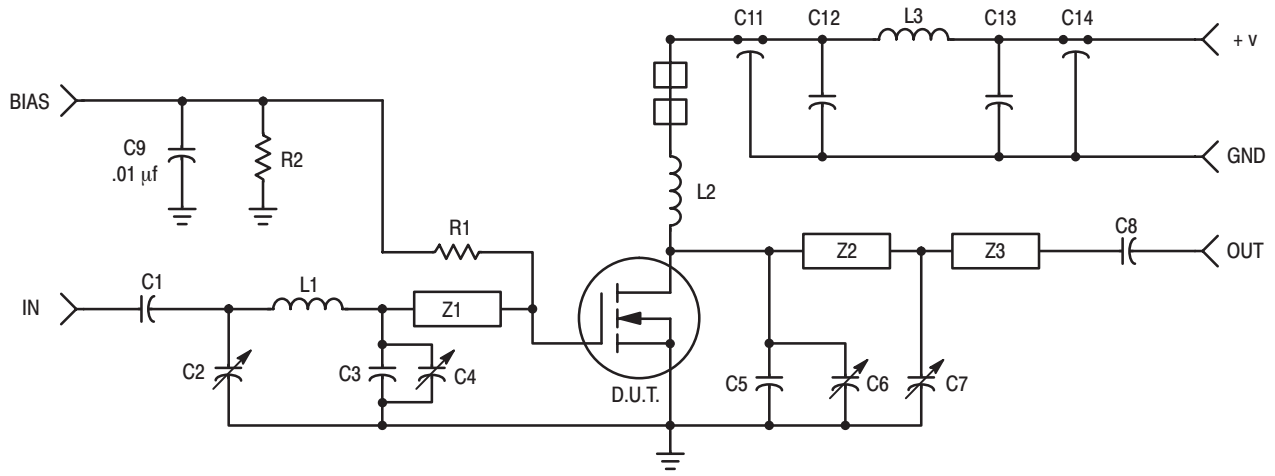
L3 — Hairpin Inductor #16 Wire



L4 — 2 Turns #16 Wire 5/16" ID

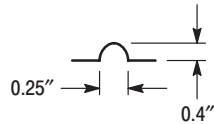
RFC1 — VK200-4B  
 R1 — 1.0 k 1/4 W Resistor  
 R2 — 100  $\Omega$  Resistor

**Figure 1. 225 MHz Test Circuit**



- C1, C8 — 270 pF ATC Chip Cap
- C2, C4, C6, C7 — 1.0–20 pF Trimmer Cap
- C3 — 15 pF Mini Unelco Cap
- C5 — 33 pF Mini Unelco Cap
- C9, C12 — 0.1  $\mu$ F Ceramic Cap
- C11, C14 — 680 pF Feed Thru Cap
- C13 — 50  $\mu$ F Tantalum Cap

L1 — Hairpin Inductor #18 Wire



L2 — 12 Turns #18 Wire 0.450" ID

L3 — Ferroxcube VK200 20/4B

R1 — 10 k 1/4 W Resistor

R2 — 1 k 1/4 W Resistor

R3 — 1.5 k 1/4 W Resistor

Z1 — Microstrip Line 0.950" x 0.250"

Z2 — Microstrip Line 1" x 0.250"

Z3 — Microstrip Line 0.550" x 0.250"

Board Material — 0.062" Teflon — fiberglass,  $\epsilon_r = 2.56$ , 1 oz. copper clad both sides

Figure 2. 400 MHz Test Circuit

### TYPICAL CHARACTERISTICS

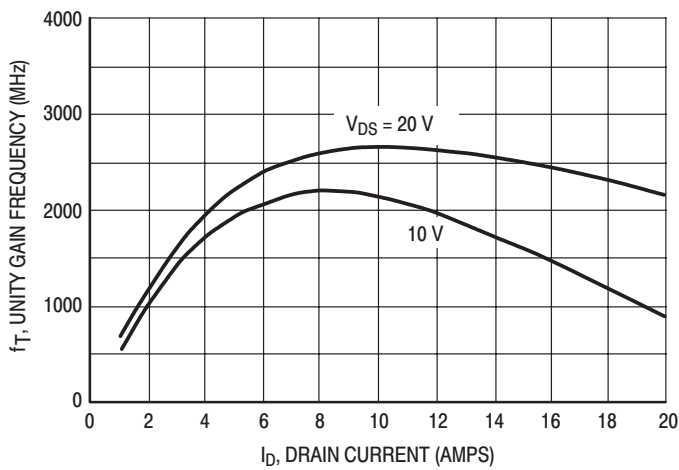


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

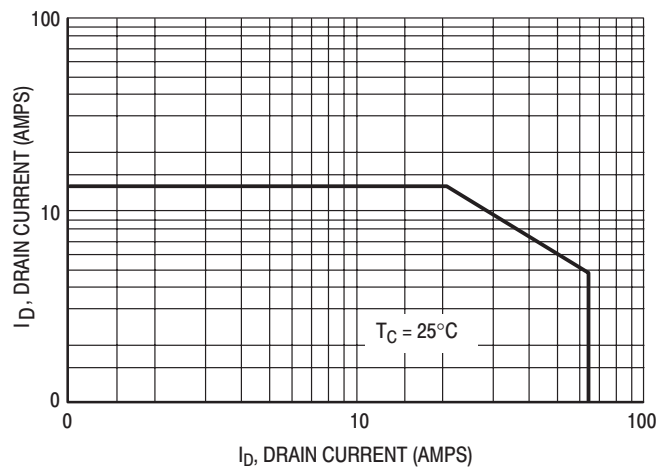
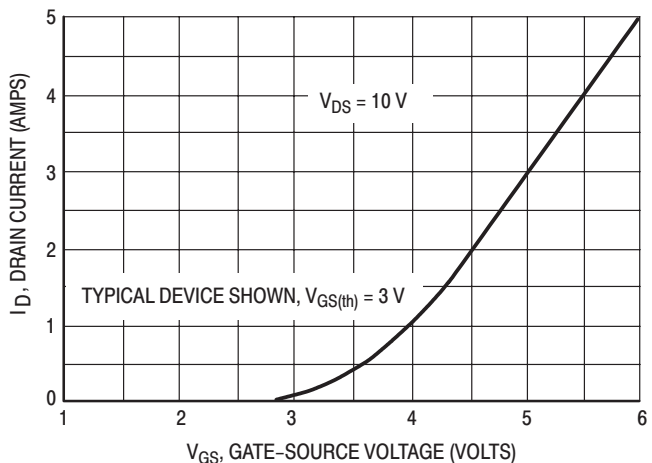
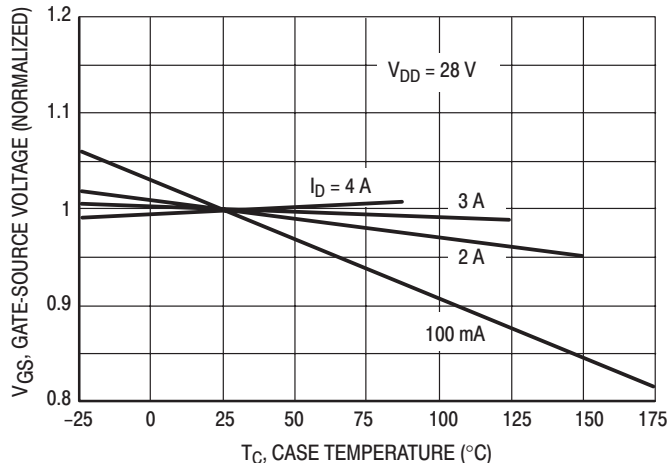


Figure 4. DC Safe Operating Area

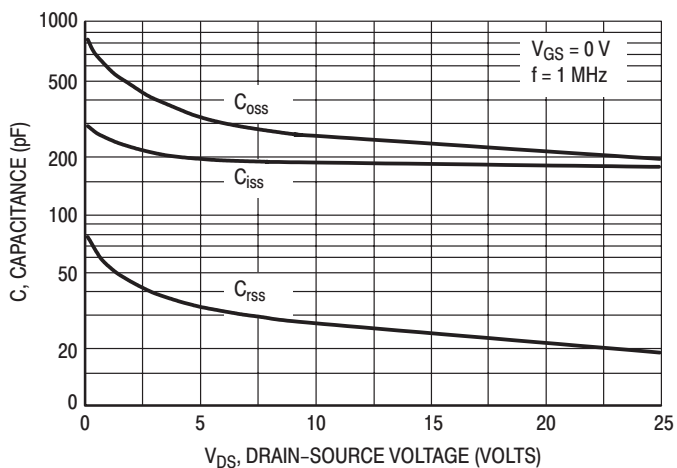
## TYPICAL CHARACTERISTICS



**Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)**



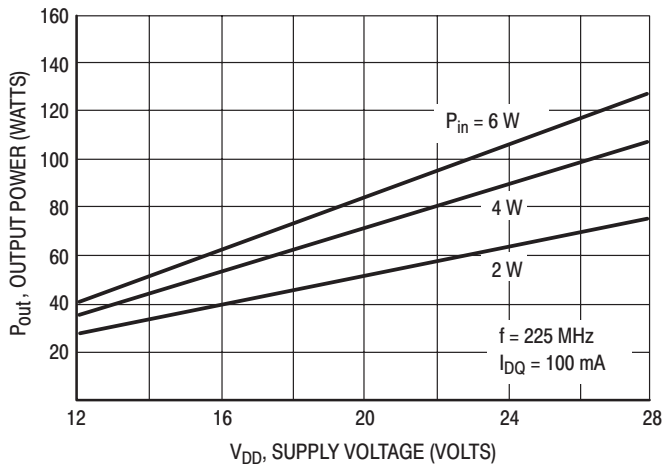
**Figure 6. Gate-Source Voltage versus Case Temperature**



**Figure 7. Capacitance versus Drain-Source Voltage**

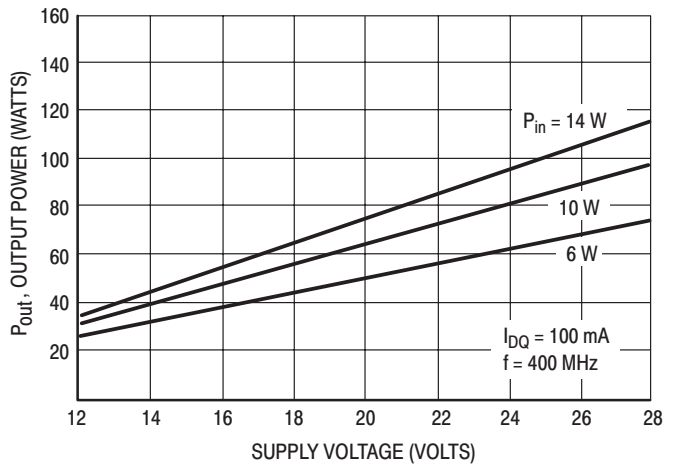
## TYPICAL CHARACTERISTICS

### MRF175LV

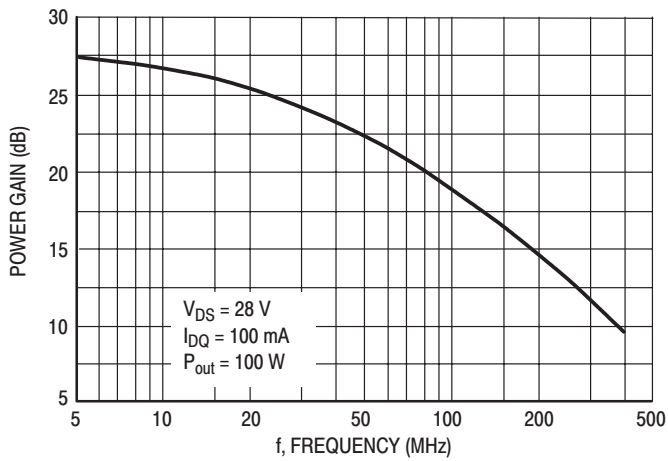


**Figure 8. Output Power versus Supply Voltage**

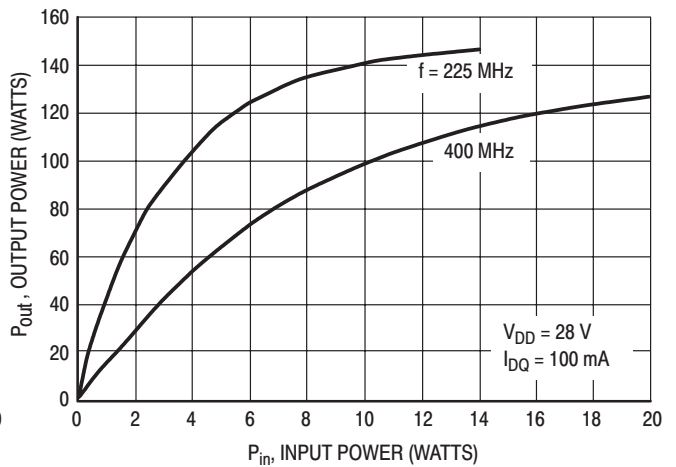
### MRF175LU



**Figure 9. Output Power versus Supply Voltage**

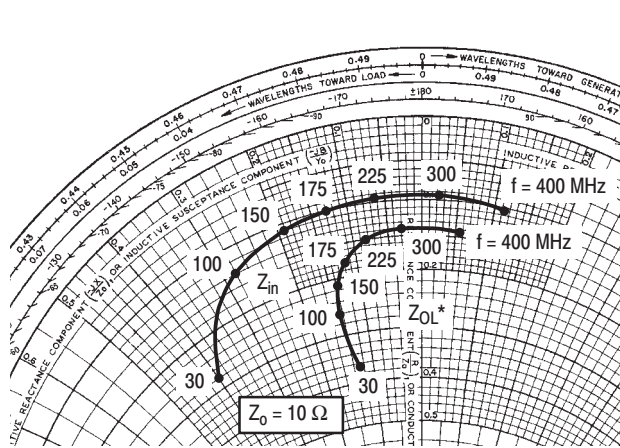


**Figure 10. Power Gain versus Frequency**



**Figure 11. Output Power versus Input Power**

## INPUT AND OUTPUT IMPEDANCE



$V_{DD} = 28 \text{ V}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  
( $P_{out} = 100 \text{ W}$ )

f MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
30	$2.80 - j4.00$	$3.65 - j1.30$
100	$1.40 - j2.80$	$2.60 - j1.50$
150	$1.10 - j1.90$	$2.10 - j1.40$
175	$1.00 - j1.25$	$1.80 - j1.20$
225	$0.95 - j0.65$	$1.50 - j0.80$
300	$0.95 + j0.20$	$1.35 - j0.30$
400	$1.05 + j1.15$	$1.45 + j0.55$

$Z_{OL}^*$  = CONJUGATE OF THE OPTIMUM  
LOAD IMPEDANCE INTO WHICH THE  
DEVICE OUTPUT OPERATES AT A GIVEN  
OUTPUT POWER, VOLTAGE AND FREQUENCY.

Figure 12.

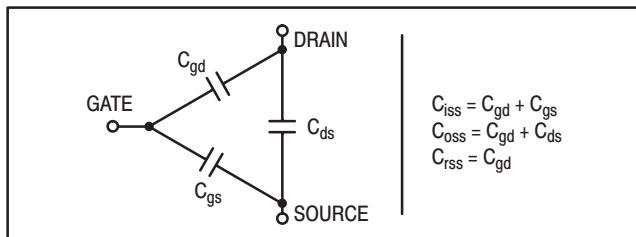
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during the fabrication of the FET results in a junction capacitance from drain-to-source ( $C_{ds}$ ).

These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain cur-

rent level. This is equivalent to  $f_T$  for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

### DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $V_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

### GATE CHARACTERISTICS

The gate of the FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9$  ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

#### **HANDLING CONSIDERATIONS**

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

#### **DESIGN CONSIDERATIONS**

The MRF175L is a RF power N-channel enhancement mode field-effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola FETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

#### **DC BIAS**

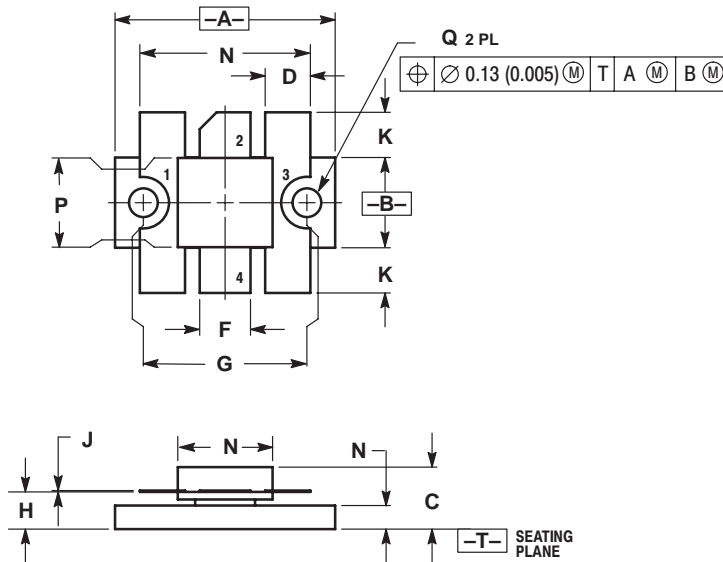
The MRF175L is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ( $I_{DQ}$ ) is not critical for many applications. The MRF175L was characterized at  $I_{DQ} = 100$  mA, each side, which is the suggested minimum value of  $I_{DQ}$ . For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

#### **GAIN CONTROL**

Power output of the MRF175L may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.965	0.985	24.51	25.02
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.73	7.36
D	0.190	0.210	4.83	5.33
E	0.095	0.115	2.42	2.92
F	0.215	0.235	5.47	5.96
G	0.725 BSC		18.42 BSC	
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.10	0.15
K	0.195	0.205	4.95	5.21
L	0.740	0.770	18.80	19.55
N	0.415	0.425	10.54	10.80
P	0.390	0.400	9.91	10.16
Q	0.120	0.135	3.05	3.42

- STYLE 1:  
 PIN 1. EMITTER  
 2. COLLECTOR  
 3. EMITTER  
 4. BASE

**CASE 333-04  
 ISSUE E**

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**INTERNET:** http://Design-NET.com

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MRF175LU/D

