MAS9316

16-BIT DAC, BUFFERED

- **+/- 0.006% DNL and INL**
- **No Laser Trimming**
- **Fast Interface Timing**

DESCRIPTION

The MAS9316 is a 16-bit, monolithic CMOS, multiplying digital-to-analog converter (DAC) designed for direct microprocessor interface. Its high relative accuracy and monotonicity is achieved without laser trimming. This is made possible by the use of highly accurate, low TCR thin film resistor process and a 4 MSB to 15 decoding design technique. Hidden errors are eliminated by testing all the 65536 different input codes.The device offers advantages like high stability over time and temperature and low sensitivity to output amplifier offset combined to excellent performance-to-cost ratio. The fast input data latches are designed as two 8-bit segments providing data storage when latched or transparent operation when unlatched. All digital inputs have high ESD protection up to 2 kV.

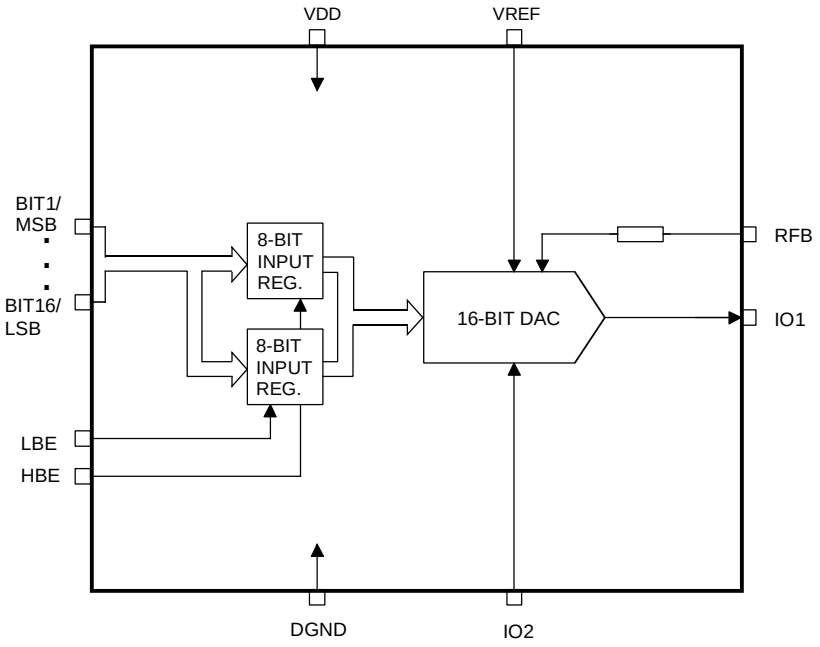
FEATURES

- Linearity TC 0.5 ppm/C
- 2 kV ESD Protection on Digital Inputs
- D4 MSB's Decoded
- All 65536 Codes Tested
- Monolithic CMOS Replacement for SIPEX
- DAC 9331-16-4 and SP9316C-4
- 24-pin PDIP Package

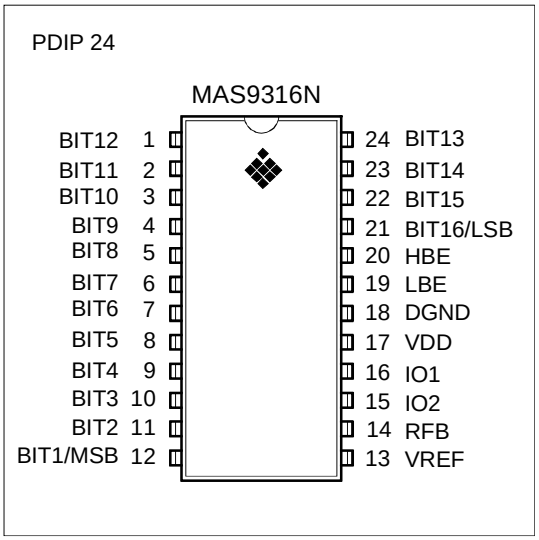
APPLICATION

- Audio applications
- Instrumentation
- uP Controlled systems

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin name	PDIP	I/O	Function
BIT 12	1	I	Data bit 12, MSB
BIT 11	2	I	Data bit 11
BIT 10	3	I	Data bit 10
BIT 9	4	I	Data bit 9
BIT 8	5	I	Data bit 8
BIT 7	6	I	Data bit 7
BIT 6	7	I	Data bit 6
BIT 5	8	I	Data bit 5
BIT 4	9	I	Data bit 4
BIT 3	10	I	Data bit 3
BIT 2	11	I	Data bit 2
BIT 1	12	I	Data bit 1
VREF	13	I	Reference voltageiInput
RFB	14	I	Feedback resistor
IO2	15	O	Current output
IO1	16	O	Current output
VDD	17	P	Positive Supply voltage
DGND	18	G	Digital ground
LBE	19	I	Low byte enable
HBE	20	I	High byte enable
BIT 16	21	I	Data bit 16, LSB
BIT 15	22	I	Data bit 15
BIT 14	23	I	Data bit 14

PIN DESCRIPTION

Pin name	PDIP	I/O	Function
BIT 13	24	I	Data bit 13

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VDD		-0.3	+17	V
Vref or RFB to DGND			-25	+25	V
Output Voltage (Pin 15, 16)			-0.3	VDD+0.3	V
Power Dissipation	PD	Any package at 75°C		459	mW
Derates above 75°C by				6	mW/ °C
Die Junction Temperature				+150	°C
Storage Temperature	Ts				°C

CAUTION:
1.Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2.The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Use proper anti-static handling procedures.
3.Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

RECOMMEDED OPERATION CONDITIONS

(conditions)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		+5	+15	+16	V
Supply Current	IDD	All digital inputs VIL or VIH		2.0	4.0	mA
Supply Current	IDD	All digital inputs 0V or 5V		0.2	1.0	mA
Power Dissipation	Pd				60	mW
Storage Temperature	Ts		0		+70	°C

ELECTRICAL CHARACTERISTICS

◆ Static Performance

(test conditions Ta=+25C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution	N	Relative accuracy 13 bits Monotonic to 14 bits Measured Using Internal Rfb DAC Register Loaded With All 1s	16			Bits
Integral Nonlinearity[1]	INL			±0.004	±0.006	%
Differential Nonlinearity[2]	DNL			±0.003	±0.006	%
Gain error	Gfse			±0.1	±0.2	%
Output Leakage Current at IO1 (pin 16)	Iilk				10	nA
Offset Error					±0.0005	%

◆ Temperature Stability

(test conditions Ta=+25C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gain error	TCTCGFSE			±1.0	±2.0	pm/C
Integral Nonlinearity TC	TCINL			±0.1	±0.5	pm/C
Differential Nonlinearity TC	TCDNL			±0.1	±0.5	pm/C

◆ Reference Input

(test conditions Ta=+25C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Resistance	Rref		2.5	5	7.5	kΩ
Voltage Range[3]					±25	v

◆ Switching Characteristics

(test conditions Ta=+25C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Strobe Width	t_{SW}	HBE and LBE Inputs	80	60		ns
Data Setup Time	t_{DS}	Bit 1 to Bit 16	80	70		ns
Data Hold Time	t_{DH}	Bit 1 to Bit 16	40	20		ns

NOTES:
1. Integral Nonlinearity is measured as the arithmetic mean value of magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3.Guaranteed by design but not production tested.
4.Logic inputs are MOS gates. Iin typical is less than 1 nA at 25C.

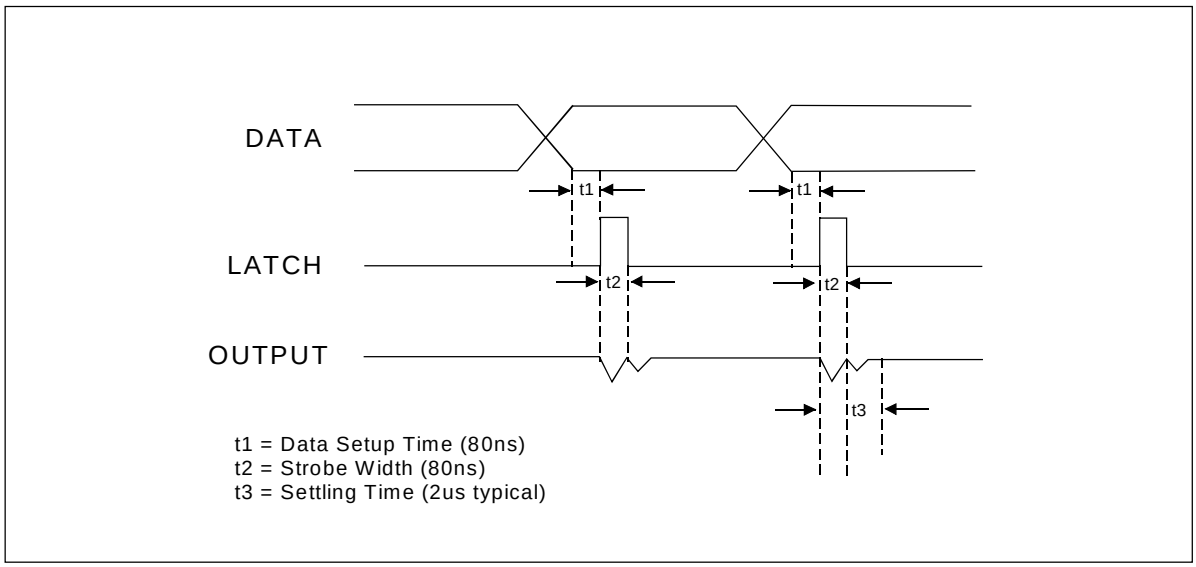
AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are subject to sample testing only. VDD=+15V, VREF=10V, IO1=IO2=DGND=0V except where stated. Output Amp is HOS-050.

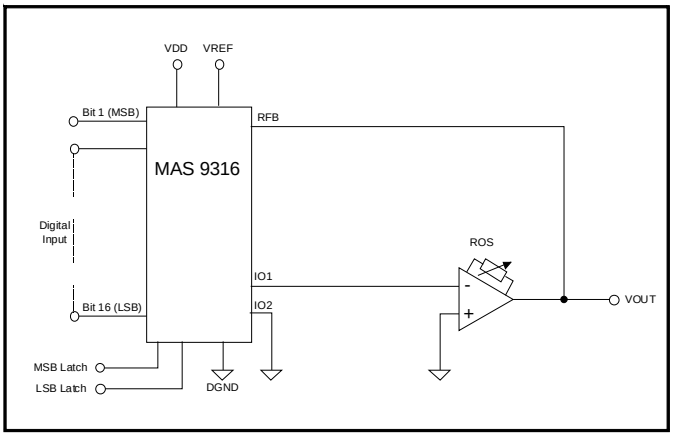
(test conditions Ta=+25C)

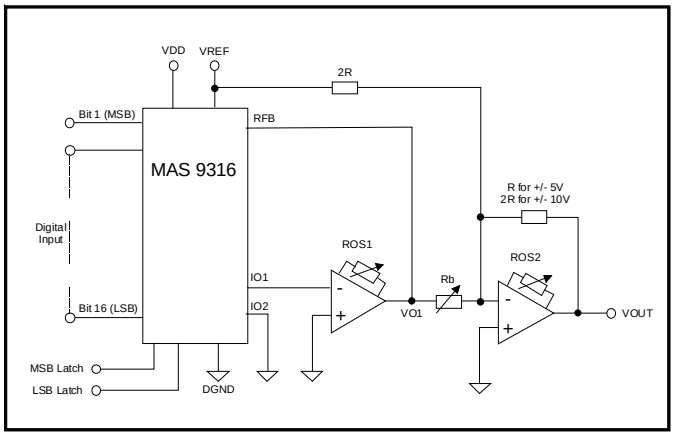
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Propagation Delay	t_{PD}	IO1 load R=100Ω, Cext=13pF All Data Inputs 0V to VDD or VDD to 0V From 50% digital input change to 90% of final analog output.		300		ns
CURRENT SETTLING Major Code Transition Full Scale Transition	ts	TIMESettling to +0.01% FSR (strobed). 0111111111111111 to 1000000000000000 or 1000000000000000 to 0111111111111111 All Data Inputs 0V to VDD or VDD to 0V		1.5 3.0		μS μs
OUTPUT CAPACITANCE CIO1 (Pin 16)170 CIO2 (Pin 15) CIO1 (Pin 16) CIO2 (Pin 15)	Co	 Digital inputs VIH Digital inputs VIH Digital inputs VIL Digital inputs VIL		 170 30 80 100		 pF pF pF pF
Digital to Analog Glitch Energy	Q	VREF =0V DAC register alternately loaded with all 0s and all 1s		250		nVs
Multiplying Feedthrough Error at IO1	FT	VREF=20Vpp; f=10kHz sine wave VREF=20Vpp, f=1kHz sine wave		3.0 0.3		mVpp mVpp
Power Supply Rejection Ratio	PSRR	VDD = 14 to 16V		±0.000 1	±0.00 2	%/%

TIMING DIAGRAM



APPLICATION INFORMATION





UNIPOLAR OPERATION, Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	-VREF ($1-2^{-N}$)
100...001	-VREF ($1/2-2^{-N}$)
100...000	-VREF 1/2
011...111	-VREF ($1/2-2^{-N}$)
000...001	-VREF (2^{-N})
000...000	0

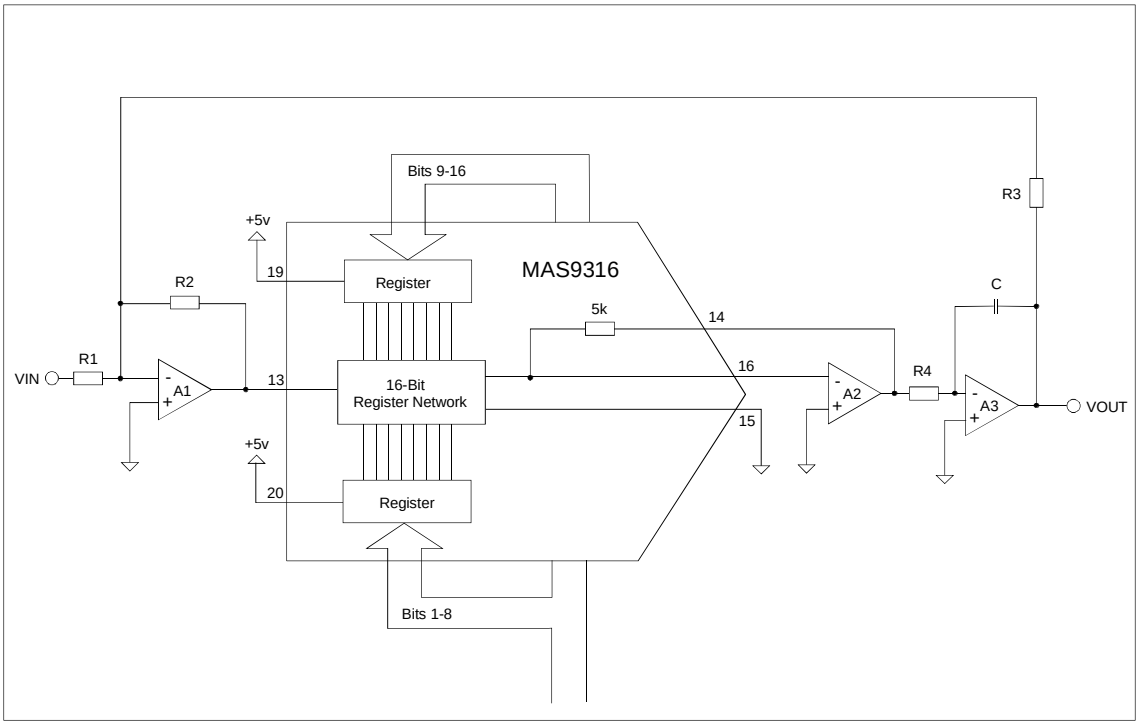
Note:
To maintain specified linearity, the external amplifier (A) must be nulled. Apply an 'all zeroes' digital input and adjust ROS for VOUT = 0 +/- 1mv.

BIPOLAR OPERATION Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	-VREF ($1-2^{-(N-1)}$)
100...001	-VREF ($2^{-(N-1)}$)
100...000	0
011...111	+VREF ($2^{(N-1)}$)
000...001	-VREF ($1-2^{-(N-1)}$)
000...000	+VREF

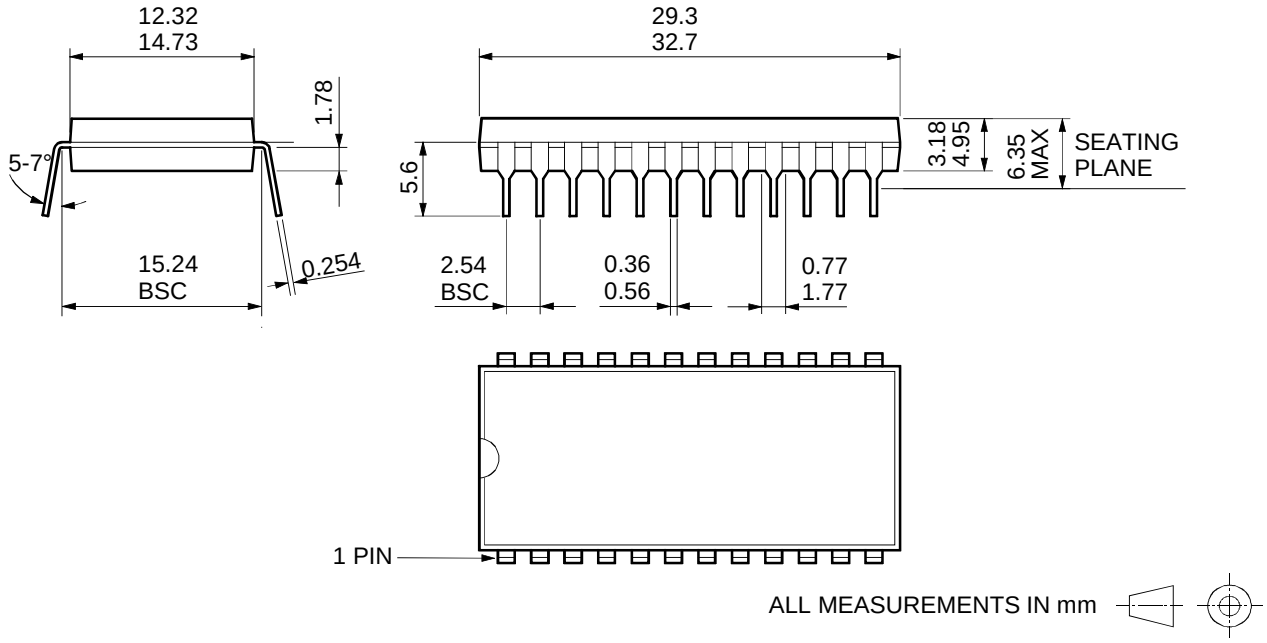
Note:
To maintain specified linearity, the external amplifier (A1 and A2) must be nulled. With a digital input of 10...0 and VREF set to zero:
a) set ROS1 for VO1 =0, b) set ROS2 for VOUT = 0
c) set VREF to +10v and adjust Rb for VOUT to be 0 volts.

DIGITALLY CONTROLLED LOW PASS FILTER



PACKAGE OUTLINES

24 LEAD PDIP OUTLINE (600 MIL BODY)



ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9316N	16-bit DAC, Buffered	24 Pin PDIP	

LOCAL DISTRIBUTOR

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