19-3519; Rev 0; 3/91

MAXIM

8-Channel Latchable Multiplexers

General Description

Maxim's DG528/DG529 are monolithic, 8-channel, CMOS multiplexers with on-board address and control latches that simplify design and reduce board space in microprocessor-based applications. The DG528 is a single-ended, 1-of-8 multiplexer, while the DG529 is a differential, 2-of-8 multiplexer. These devices can operate as multiplexers or demultiplexers.

The DG528/DG529 have break-before-make switching to prevent momentary shorting of the input signals. Each device operates with dual supplies (±4.5V to ±20V) or a single supply (+5V to +30V). All logic inputs are TTL and CMOS compatible. The Maxim DG528/DG529 are pin and electrically compatible with the industry-standard DG528/DG529.

Applications

Data-Acquisition Systems
Automatic Test Equipment
Avionics and Military Systems
Communication Systems
Microprocessor-Controlled Systems
Audio-Signal Multiplexing

Features

- **Low-Power, Monolithic CMOS Design**
- **On-Board Address Latches**
- **Break-Before-Make Input Switches**
- **TTL and CMOS Logic Compatible**
- **Microprocessor-Bus Compatible**
- **$r_{DS(ON)}$ < 400Ω**
- **Pin and Electrically Compatible with the Industry-Standard DG528/DG529 and ADG528/ADG529**

Ordering Information

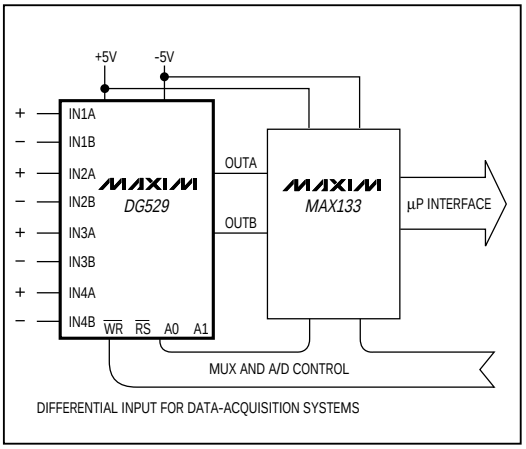
PART	TEMP. RANGE	PIN-PACKAGE
DG528CJ	0°C to +70°C	18 Plastic DIP
DG528CWN	0°C to +70°C	18 Wide SO
DG528CK	0°C to +70°C	18 CERDIP
DG528C/D	0°C to +70°C	Dice*
DG528DJ	-40°C to +85°C	18 Plastic DIP
DG528DN	-40°C to +85°C	20 PLCC
DG528EWN	-40°C to +85°C	18 Wide SO
DG528DK	-40°C to +85°C	18 CERDIP
DG528AZ	-55°C to +125°C	20 LCC**
DG528AK	-55°C to +125°C	18 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

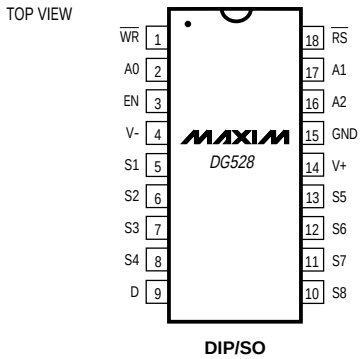
*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



DIFFERENTIAL INPUT FOR DATA-ACQUISITION SYSTEMS

Pin Configurations



DIP/SO

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ .....+44V
GND .....+25V
Digital Inputs V_S, V_D .....V- -2V to V+ +2V
or 20mA, whichever occurs first.
Current (any terminal, except S or D) 30mA
Continuous Current, S or D
Peak Current, S or D 20mA
(pulsed at 1ms, 10% duty cycle max) 50mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C)...889mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C)....842mW
20-Pin PLCC (derate 10.00mW/°C above +70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
DG52_C_ .....0°C to +70°C
DG52_D_/E_ .....-40°C to +85°C
DG52_A_ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_{EN} = 2.4V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			DG52_A MIN	DG52_A TYP	DG52_A MAX	DG52_C/D/E MIN	DG52_C/D/E TYP	DG52_C/D/E MAX	UNITS
SWITCH											
Analog-Signal Range	V_{ANALOG}	(Note 2)			-15		15	-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V_D = ±10V, V_{AL} = 0.8V, I_S = -200µA, V_{AH} = 2.4 (Note 3)		T_A = +25°C, T_{MIN}		270	400		270	450	Ω
				T_A = T_{MAX}			500			500	
Greatest Change in Drain-Source On-Resistance Between Channels	$\Delta r_{DS(ON)}$	-10V < V_S < 10V		T_A = +25°C		6			6		%
Source-Off Leakage Current	$I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ±10V		T_A = +25°C	-1	-0.005	1	-5	-0.005	5	nA
				T_A = T_{MAX}	-50	-0.005	50	-50	-0.005	50	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ±10V	DG528	T_A = +25°C	-10	-0.015	10	-20	-0.015	20	nA
				T_A = T_{MAX}	-200	-0.015	200	-200	-0.015	200	
			DG529	T_A = +25°C	-10	-0.008	10	-20	-0.008	20	
				T_A = T_{MAX}	-100	-0.008	100	-100	-0.008	100	
Drain-On Leakage Current (Notes 3, 4)	$I_{D(ON)}$	V_{AH} = 2.4V, V_S = V_D = ±10V, V_{AL} = 0.8V, V_{EN} = 2.4V	DG528	T_A = +25°C	-10	-0.03	10	-20	-0.03	20	nA
				T_A = T_{MAX}	-200	-0.03	200	-200	-0.03	200	
			DG529	T_A = +25°C	-10	-0.015	10	-20	-0.015	20	
				T_A = T_{MAX}	-100	-0.015	100	-100	-0.015	100	
INPUT											
Address Input Current, Input Voltage High	I_{AH}	V_A = 2.4V		T_A = +25°C	-1	-0.002	1	-1	-0.002	1	µA
				T_A = T_{MAX}	-30			-30			
		V_A = 15V		T_A = +25°C	-1	-0.006	1	-1	-0.006	1	
				T_A = T_{MAX}			30			30	
Address Input Current, Input Voltage Low	I_{AL}	V_A = $\overline{RS}$ = $\overline{WR}$ = 0V, V_{EN} = 0V or 2.4V		T_A = +25°C	-1	-0.002	1	-1	-0.002	1	µA
				T_A = T_{MAX}	-30	-0.01		-30	-0.01		

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_{EN} = 2.4V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			DG52_A MIN	DG52_A TYP	DG52_A MAX	DG52_C/D/E MIN	DG52_C/D/E TYP	DG52_C/D/E MAX	UNITS
DYNAMIC											
Switching Time of Multiplexer	t_{TRANS}	Figure 1		T_A = +25°C		0.4	1			1.5	µs
Break-Before-Make Interval	t_{OPEN}	Figure 2		T_A = +25°C		0.2			0.2		µs
Enable, Write Turn-On Time	$t_{ON(EN, \overline{WR})}$	Figures 3, 4		T_A = +25°C		1.0	1.5			1.5	µs
Enable, Reset Turn-Off Time	$t_{OFF(EN, \overline{RS})}$	Figures 3, 5		T_A = +25°C		0.4	1			1.5	µs
Charge Injection	Q	Figure 6		T_A = +25°C		4			4		pC
Off Isolation	O_{IRR}	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 500kHz		T_A = +25°C		68			68		dB
Logic-Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		2.5			2.5		pF
Source-Off Capacitance	$C_{S(OFF)}$	V_{EN} = 0V, f = 140kHz, V_S = 0V		T_A = +25°C		5			5		pF
Drain-Off Capacitance	$C_{D(OFF)}$	V_{EN} = 0V, f = 140kHz, V_S = 0V	DG528	T_A = +25°C		25			25		pF
			DG529	T_A = +25°C		12			12		
SUPPLY											
Positive Supply Current	I+	V_{EN} = V_{AH} = 0V		T_A = +25°C		0.003	2.5		0.003	2.5	mA
Negative Supply Current	I-	V_{EN} = V_{AH} = 0V		T_A = +25°C	-1.5	0.01		-1.5	0.01		mA
MINIMUM INPUT TIMING											
$\overline{WR}$ Pulse Width	t_{WW}	Figure 7			300	150		300	15		ns
AX, EN Data Valid to $\overline{WR}$	t_{DW}	(Stabilization Time) Figure 7			180	120		180	12		ns
AX, EN Data Valid after $\overline{WR}$	t_{WD}	(Hold Time) Figure 7			30	10		30	10		ns
$\overline{RS}$ Pulse Width	$t_{\overline{RS}}$	Figure 7; V_S = 5V (Note 5)			500	150		500	150		ns

Note 2: Guaranteed by design.
Note 3: Sequence each switch on.
Note 4: $I_{D(ON)}$ is leakage from driver into on switch.
Note 5: Reset pulse period must be at least 50µs during or after power-on.

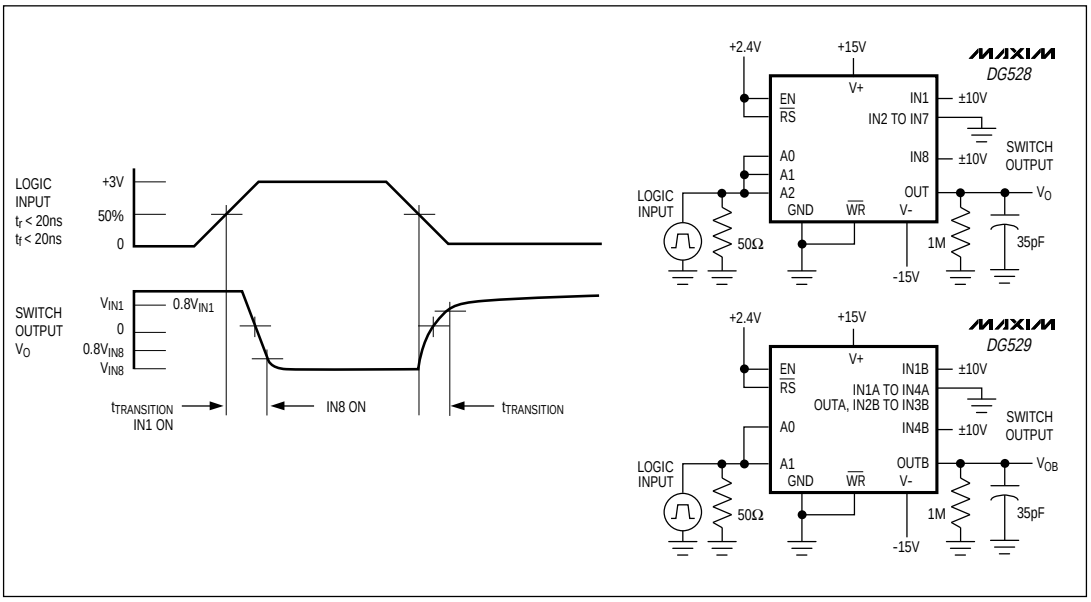


Figure 1. Transition-Time Test Circuits

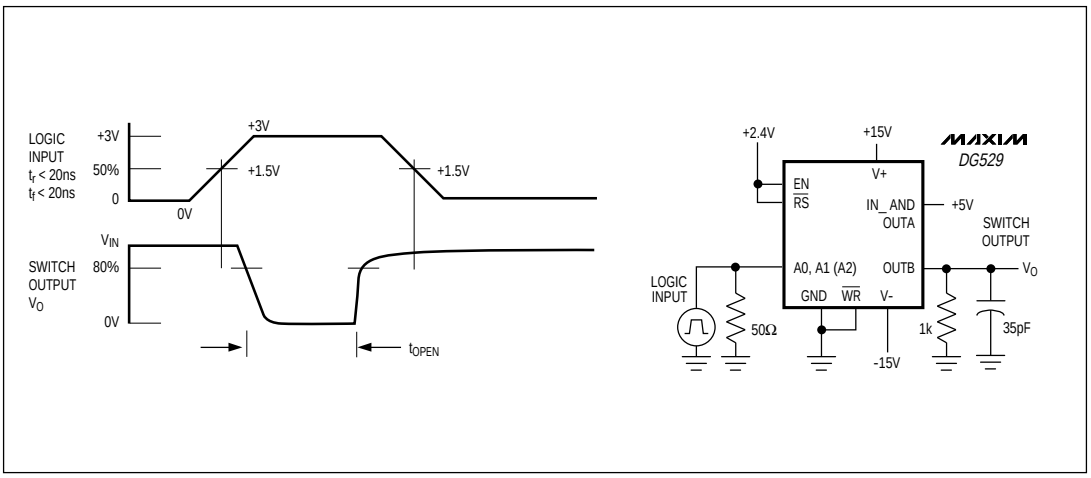


Figure 2. Open-Time (B.B.M.) Interval Test Circuit

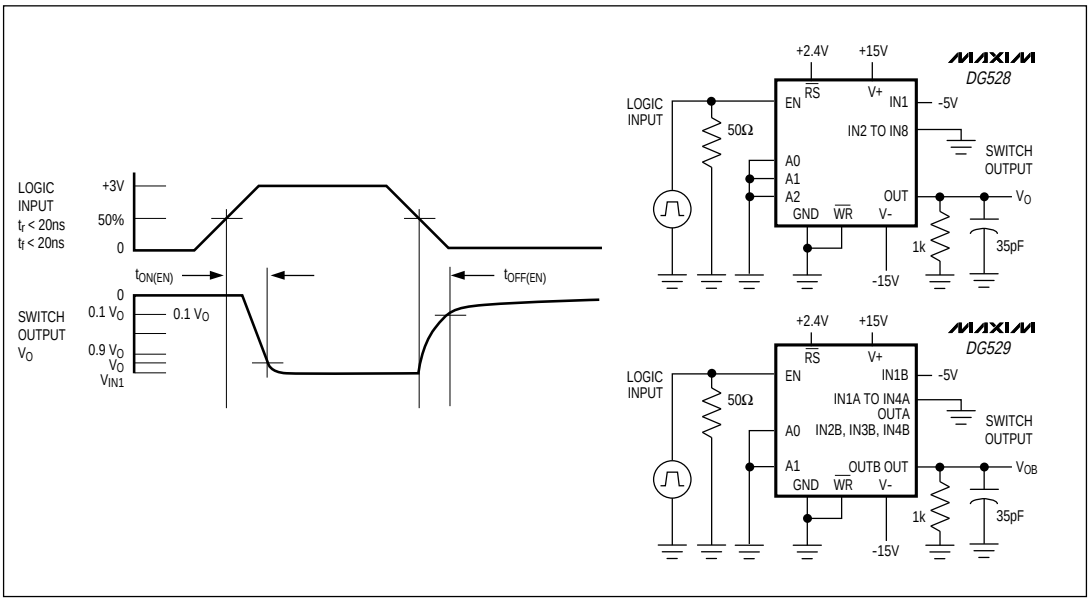


Figure 3. Enable t_{ON}/t_{OFF} Time Test Circuit

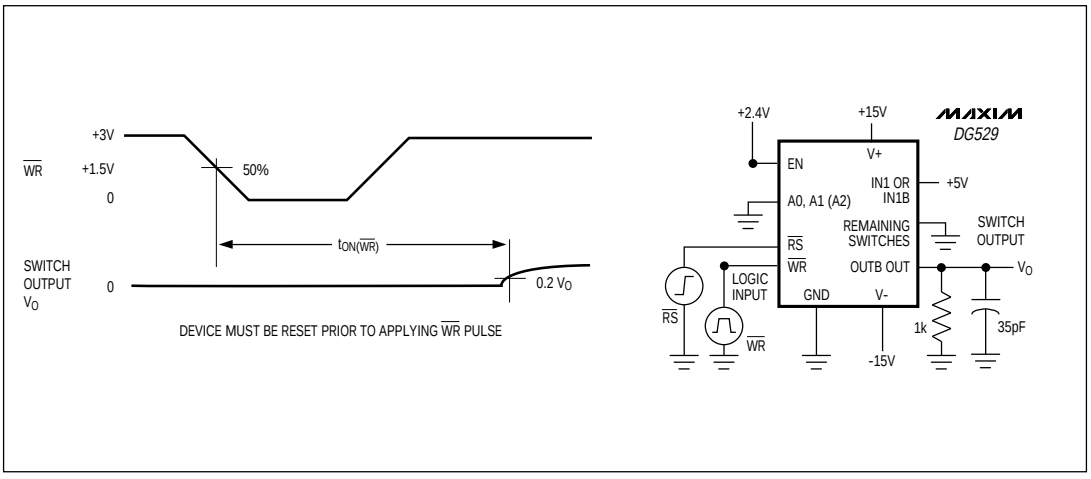


Figure 4. Write Turn-On Time $t_{ON(\overline{WR})}$ Test Circuit

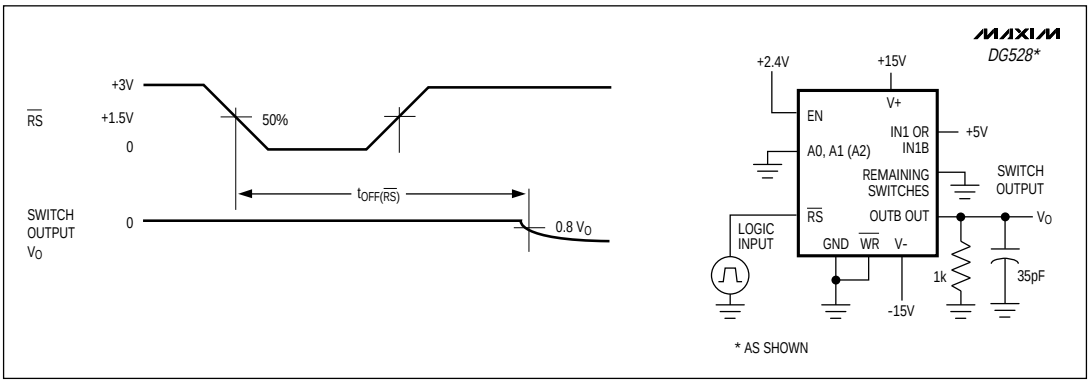


Figure 5. Reset Turn-Off Time $t_{OFF(\overline{RS})}$ Test Circuit

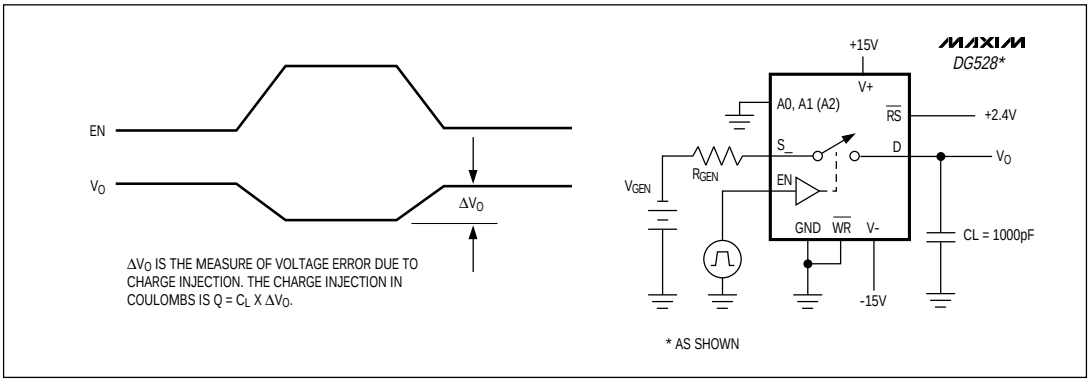


Figure 6. Charge-Injection Test Circuit

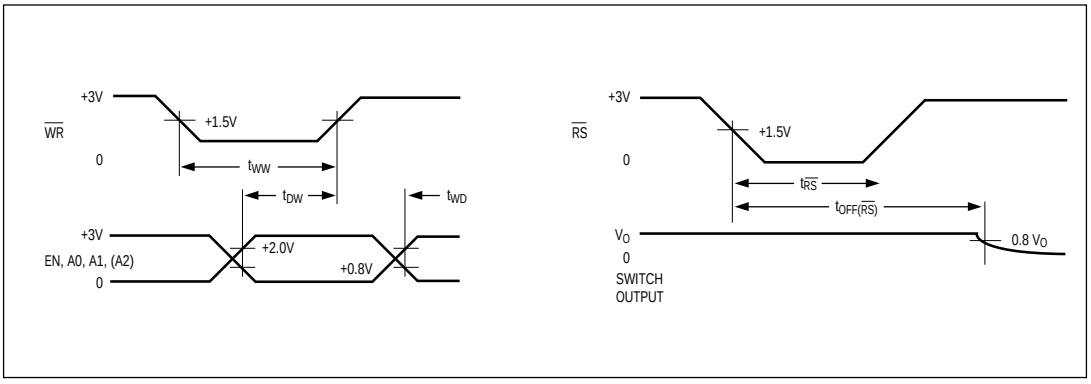


Figure 7. Typical Timing Diagrams for DG528/DG529

Table 1. DG528 Logic States

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Table 2. DG529 Logic States

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching					
X	X	X	↑	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Note: Logic "1": $V_{AH} \geq 2.4V$, Logic "0": $V_{AL} \leq 0.8V$.

Detailed Description

The internal structures of the DG528/DG529 include translators for the A2/A1/A0/EN/$\overline{WR}$/$\overline{RS}$ digital inputs, latches, and a decode section for channel selection (Truth Tables). The gate structures consist of parallel combinations of N and P MOSFETs.

$\overline{WRITE}$ ($\overline{WR}$) and $\overline{RESET}$ ($\overline{RS}$) strobes are provided for interfacing with µP-bus lines (Figure 9), alleviating the need for the µP to provide constant address inputs to the mux to hold a particular channel.

When the $\overline{WR}$ strobe is in the low state (less than 0.8V) and the $\overline{RS}$ strobe is in the high state (greater than 2.4V), the muxes are in the transparent mode—they act similarly to nonlatching devices, such as the DG508A/DG509A or the HI508/HI509.

When the $\overline{WR}$ goes high, the previous BCD address input is latched and held in that state indefinitely. To pull the mux out of this state, either $\overline{WR}$ must be taken low to the transition state, or $\overline{RS}$ must be taken low to turn off all channels.

$\overline{RS}$ turns off all channels when it is low, which resets channel selection to the channel 1 mode.

The DG528/DG529 work with both single and dual supplies and function over the +5V to +30V single-supply range. For example, with a single +15V power supply, analog signals in the 0V to +15V range can be switched normally. If negative signals around 0V are expected, a negative supply is needed. However, only -5V is needed to normally switch signals in the -5V to +15V range (-5V, +15V supplies). No current is drawn from the negative supply, so Maxim's MAX635 DC-DC converter is an ideal choice.

The EN latch allows all switches to be turned off under program control. This is useful when two or more DG528s are cascaded to build 16-line and larger analog-signal multiplexers.

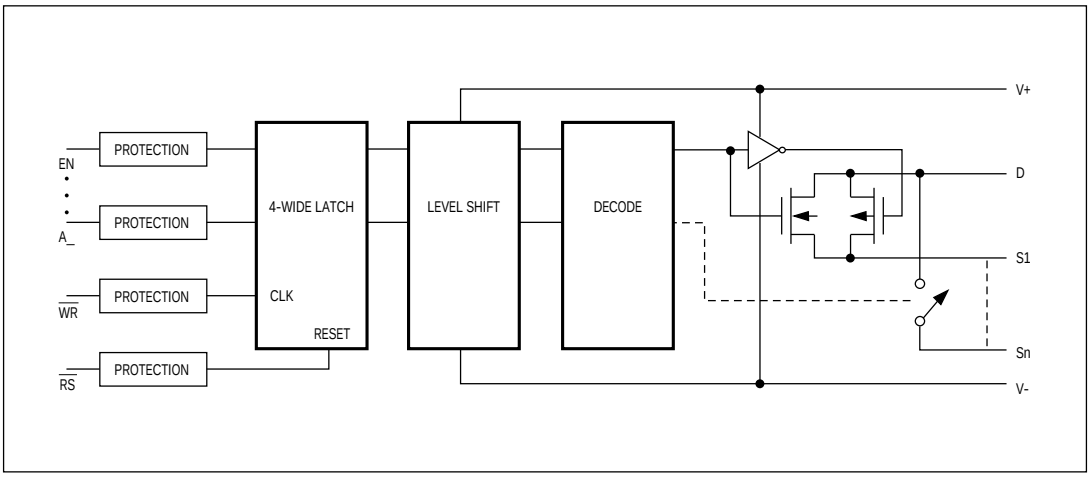


Figure 8. Simplified Internal Structure

Applications

Operation with Supply Voltages Other Than ±15V

Maxim guarantees the DG528/DG529 for operation from ±4.5V to ±20V supplies. The switching delays increase by about a factor of two at ±5V, and break-before-make action is preserved.

The DG528/DG529 can operate with a single +5V to +30V supply as well as asymmetrical power supplies like +15V and -5V. The digital threshold will remain approximately 1.6V above the GND pin, and the analog characteristics such as $r_{DS(ON)}$ are determined by the total voltage difference between V+ and V-. Connect V- to 0V when operating with a +5V to +30V single supply.

Digital Interface Levels

The typical digital threshold of both the address lines and EN is 1.6V with a temperature coefficient of approximately -3mV/°C, ensuring compatibility with TTL logic over the temperature range. The digital threshold is relatively independent of the power-supply voltages, going from a typical 1.6V when V+ is 15V to 1.5V typical with V+ = 5V. Therefore, Maxim's DG528/DG529 operate with standard TTL logic levels, even with ±5V power supplies. In all cases, EN's threshold is the same as the other logic inputs and is referenced to GND.

The digital inputs can also be driven with CMOS logic levels swinging from either V+ to V- or from V+ to GND. The digital input current is just a few nanoamps of leakage at all input-voltage levels with a guaranteed maximum of 1µA. The digital inputs are protected from ESD by a 30V zener diode between the input and V+ and can be driven ±2V beyond the supplies without drawing excessive current.

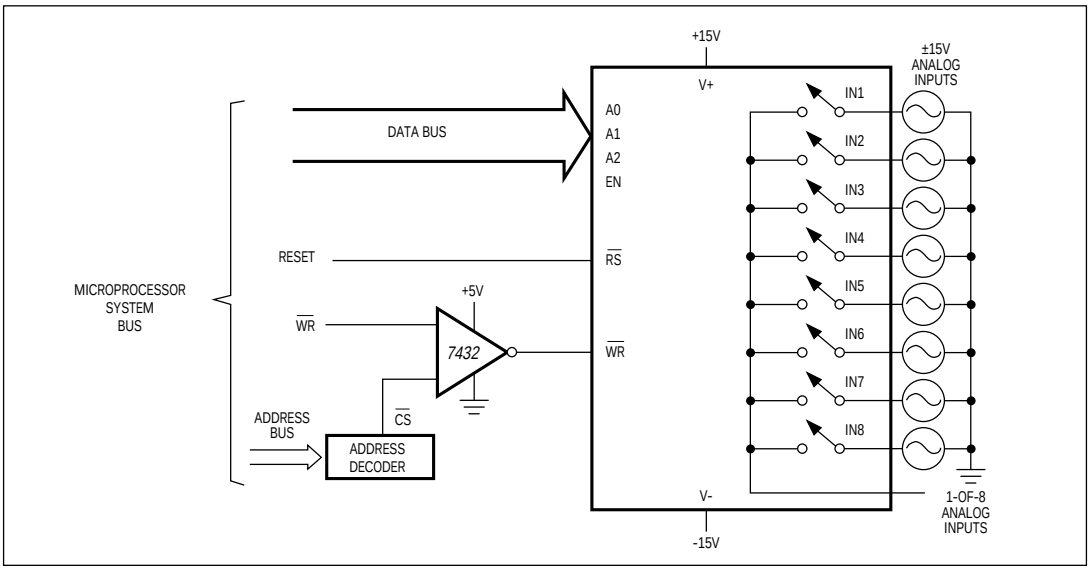
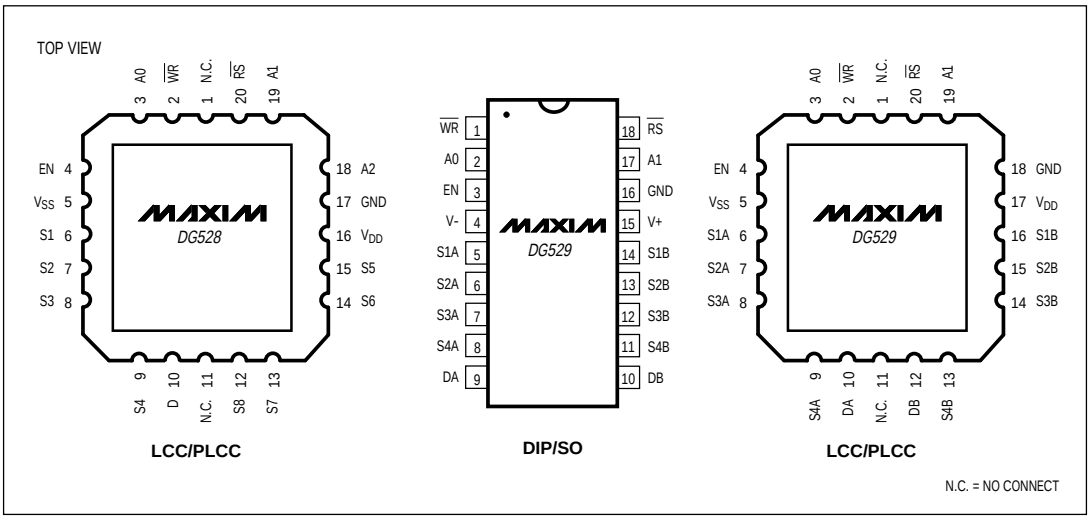


Figure 9. Bus Interface

Pin Configurations (continued)



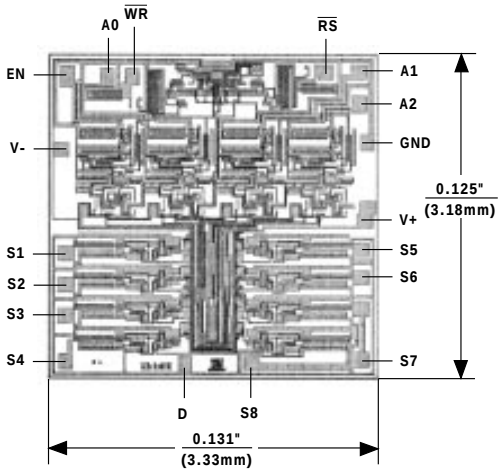
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
DG529CJ	0°C to +70°C	18 Plastic DIP
DG529CWN	0°C to +70°C	18 Wide SO
DG529CK	0°C to +70°C	18 CERDIP
DG529C/D	0°C to +70°C	Dice*
DG529DJ	-40°C to +85°C	18 Plastic DIP
DG529DN	-40°C to +85°C	20 PLCC
DG529EWN	-40°C to +85°C	18 Wide SO
DG529DK	-40°C to +85°C	18 CERDIP
DG529AZ	-55°C to +125°C	20 LCC**
DG529AK	-55°C to +125°C	18 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

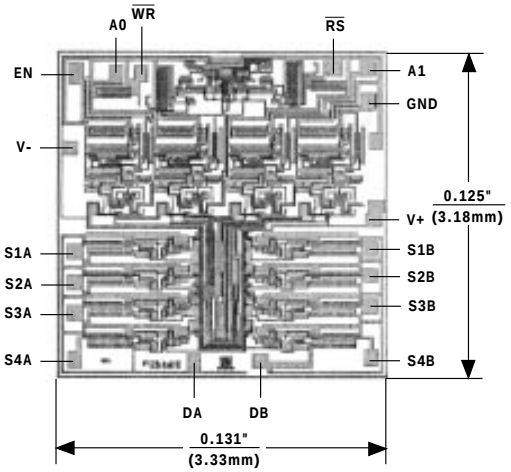
_____Chip Topographies

DG528



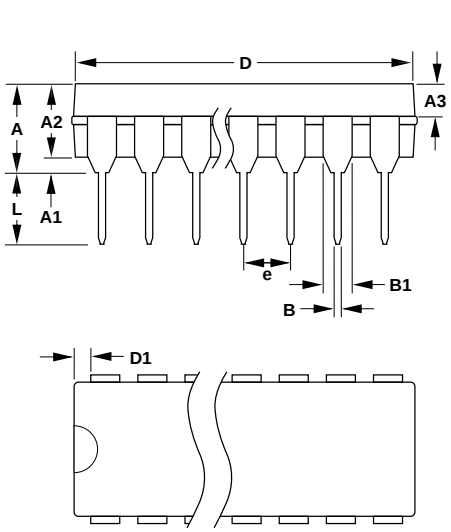
TRANSISTOR COUNT: 200
SUBSTRATE CONNECTED TO V+

DG529



TRANSISTOR COUNT: 200
SUBSTRATE CONNECTED TO V+

Package Information

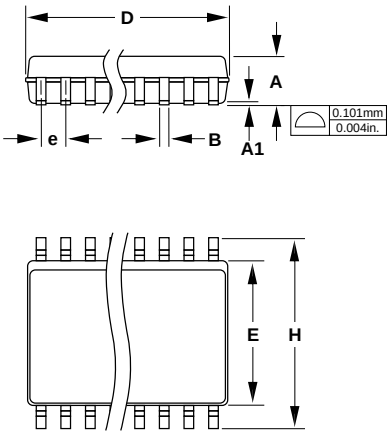


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



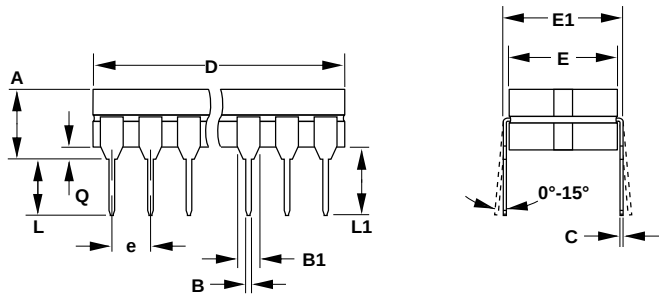
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

Package Information (continued)



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

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