



# +3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

MAX3680

## General Description

The MAX3680 deserializer is ideal for converting 622Mbps serial data to 8-bit-wide, 77Mbps parallel data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial-clock and data inputs, and delivers TTL clock and data outputs. It also provides a TTL synchronization input that enables data realignment and reframing.

The MAX3680 is available in the extended-industrial temperature range (-40°C to +85°C), in a 28-pin SSOP package.

## Applications

- 622Mbps SDH/SONET Transmission Systems
- 622Mbps ATM/SONET Access Nodes
- Add/Drop Multiplexers
- Digital Cross Connects

## Features

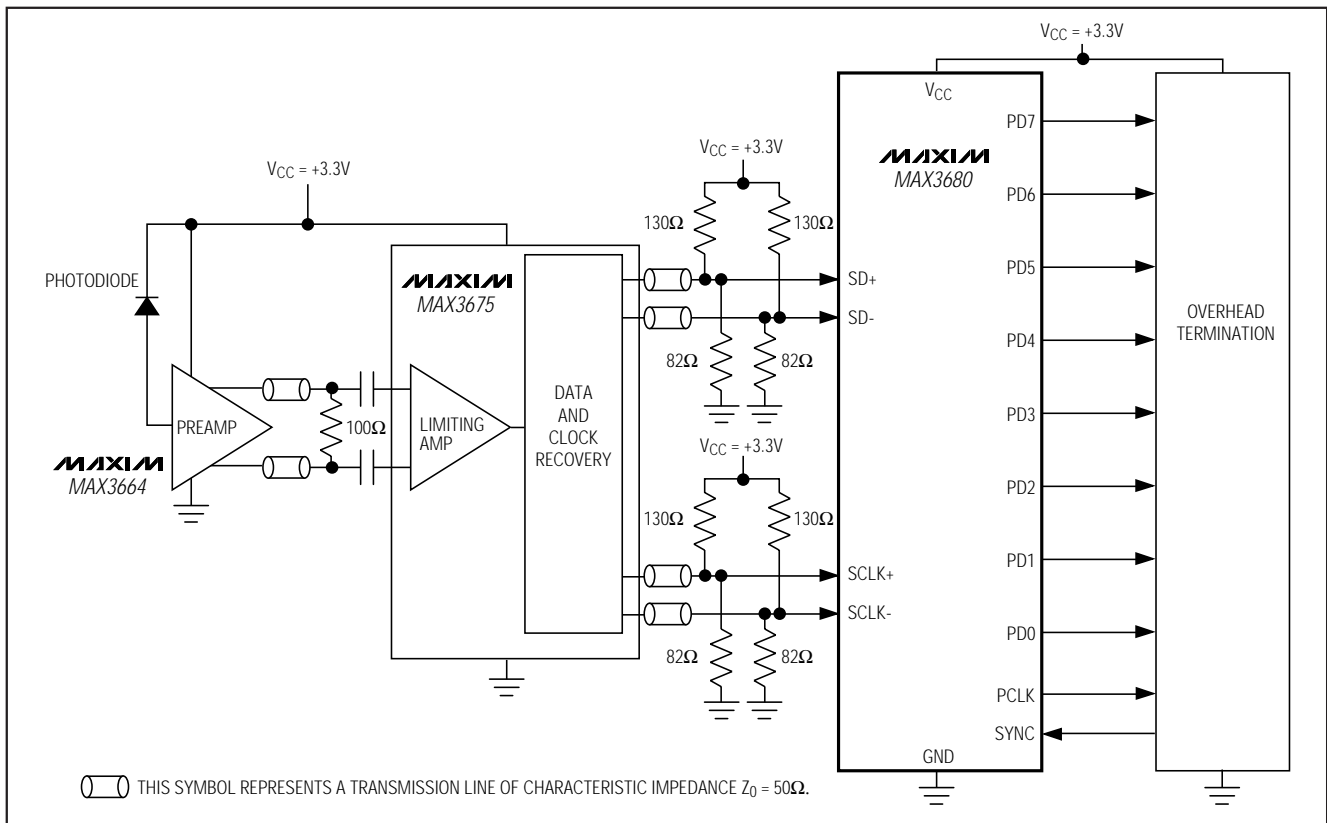
- ◆ Single +3.3V Supply
- ◆ 622Mbps Serial to 77Mbps Parallel Conversion
- ◆ 165mW Power
- ◆ Synchronization Input for Data Realignment and Reframing
- ◆ Differential 3.3V PECL Clock and Data Inputs
- ◆ TTL Data Outputs and Synchronization Input

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3680EAI	-40°C to +85°C	28 SSOP

Pin Configuration appears at end of data sheet.

## Typical Operating Circuit



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## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)		Continuous Power Dissipation ( $T_A = +85^\circ\text{C}$ )
$V_{CC}$ .....	-0.5V to 5V	SSOP (derate 9.52mW/ $^\circ\text{C}$ above $+85^\circ\text{C}$ ) .....
PECL Inputs (SD+/-, SCLK+/-) .....	-0.5V to ( $V_{CC} + 0.5\text{V}$ )	Operating Temperature Range .....
TTL Input (SYNC) .....	-0.5V to ( $V_{CC} + 0.5\text{V}$ )	Storage Temperature Range .....
TTL Outputs (PCLK, PD_) .....	-0.5V to ( $V_{CC} + 0.5\text{V}$ )	Lead Temperature (soldering, 10sec) .....

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3\text{V}$ ,  $T_A = +25^\circ\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$I_{CC}$	TTL outputs = high	25	50	90	mA
<b>PECL INPUTS (SD+/-, SCLK+/-)</b>						
Input High Voltage	$V_{IH}$		$V_{CC} - 1.16$		$V_{CC} - 0.88$	V
Input Low Voltage	$V_{IL}$		$V_{CC} - 1.81$		$V_{CC} - 1.48$	V
Input High Current	$I_{IH}$	$V_{IN} = V_{IH}(\text{MAX})$	-10		10	$\mu\text{A}$
Input Low Current	$I_{IL}$	$V_{IN} = V_{IL}(\text{MAX})$	-10		10	$\mu\text{A}$
<b>TTL INPUT AND OUTPUTS (SYNC, PCLK, PD_)</b>						
Input High Voltage	$V_{IH}$		2.0			V
Input Low Voltage	$V_{IL}$				0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{IH}(\text{MAX})$	-10		10	$\mu\text{A}$
Input Low Current	$I_{IL}$	$V_{IN} = V_{IL}(\text{MAX})$	-10		10	$\mu\text{A}$
Output High Voltage	$V_{OH}$	Output sourcing = $400\mu\text{A}$	2.4		$V_{CC}$	V
Output Low Voltage	$V_{OL}$	Output sinking = $400\mu\text{A}$	0		0.44	V

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	$f_{SCLK}$		622			MHz
Serial Data Setup Time	$t_{SU}$		800			ps
Serial Data Hold Time	$t_H$		50			ps
Parallel Clock to Data Output Delay	$t_{CLK-Q}$	$V_{CC} = 3.3\text{V}$ , $C_L = 18\text{pF}$	-200	500	1300	ps

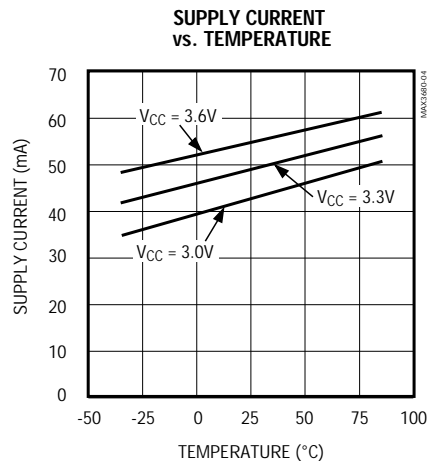
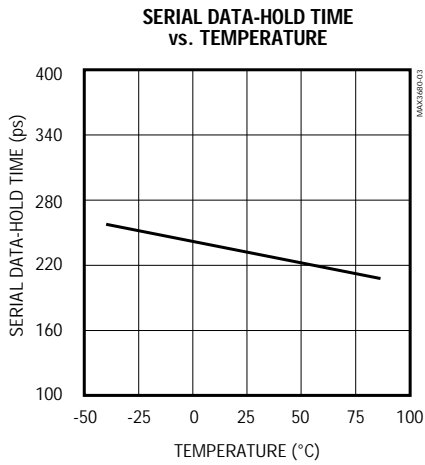
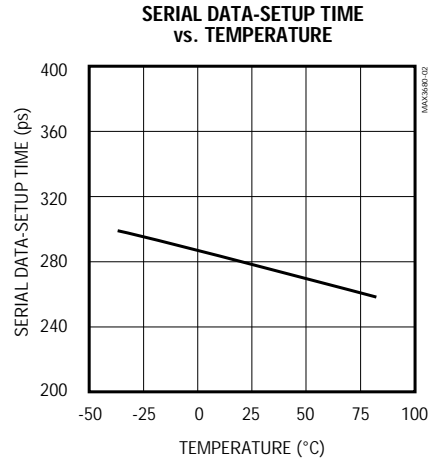
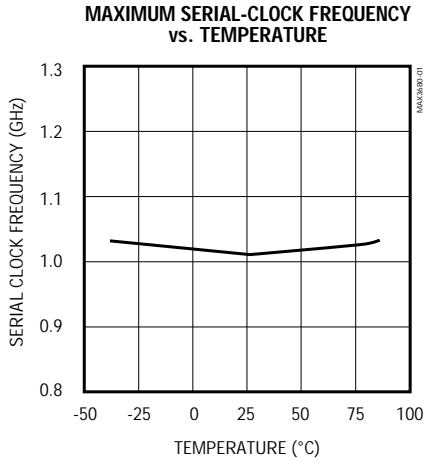
**Note 1:** AC characteristics guaranteed by design and characterization.

# +3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

## Typical Operating Characteristics

(V<sub>CC</sub> = +3.0V to +3.6V, unless otherwise noted.)

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## Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 8, 14, 18, 25	VCC	+3.3V Supply Voltage
3	SD+	Noninverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
4	SD-	Inverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
6	SCLK+	Noninverting PECL Serial Clock Input
7	SCLK-	Inverting PECL Serial Clock Input
9, 11, 12, 16, 20, 23, 27	GND	Ground
10	SYNC	TTL Synchronization Pulse Input. Pulse high for at least two SCLK periods to shift the data alignment by dropping one bit in the serial input data stream.
13	PCLK	TTL Parallel Clock Output
15, 17, 19, 21, 22, 24, 26, 28	PD0–PD7	TTL Parallel Data Outputs. Data is updated on the falling edge of PCLK. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.

## Detailed Description

The MAX3680 deserializer uses an 8-bit shift register, 8-bit parallel output register, 3-bit counter, PECL input buffers, and TTL input/output buffers to convert 622Mbps serial data to 8-bit-wide, 77Mbps parallel data (Figure 1).

The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 3-bit counter generates a parallel output clock (PCLK) by dividing down the serial clock frequency. The PCLK signal is used to clock the parallel output register. During normal operation, the counter divides the SCLK frequency by eight, causing the output register to latch every eight bits of incoming serial data.

The synchronization input (SYNC) is used for data realignment and reframing. When the SYNC signal is pulsed high for at least two SCLK cycles, PCLK is delayed by one SCLK cycle, causing the first incoming bit of the serial input data stream to be dropped. This realignment is guaranteed to occur within two PCLK cycles of the SYNC rising edge.

See Figure 2 for the functional timing diagrams and Figure 3 for the timing parameters diagram.

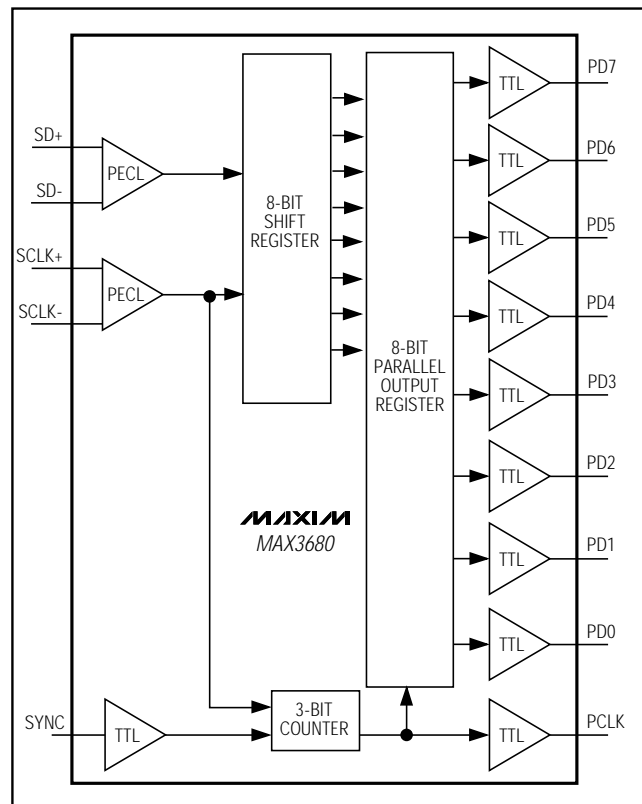


Figure 1. Functional Diagram

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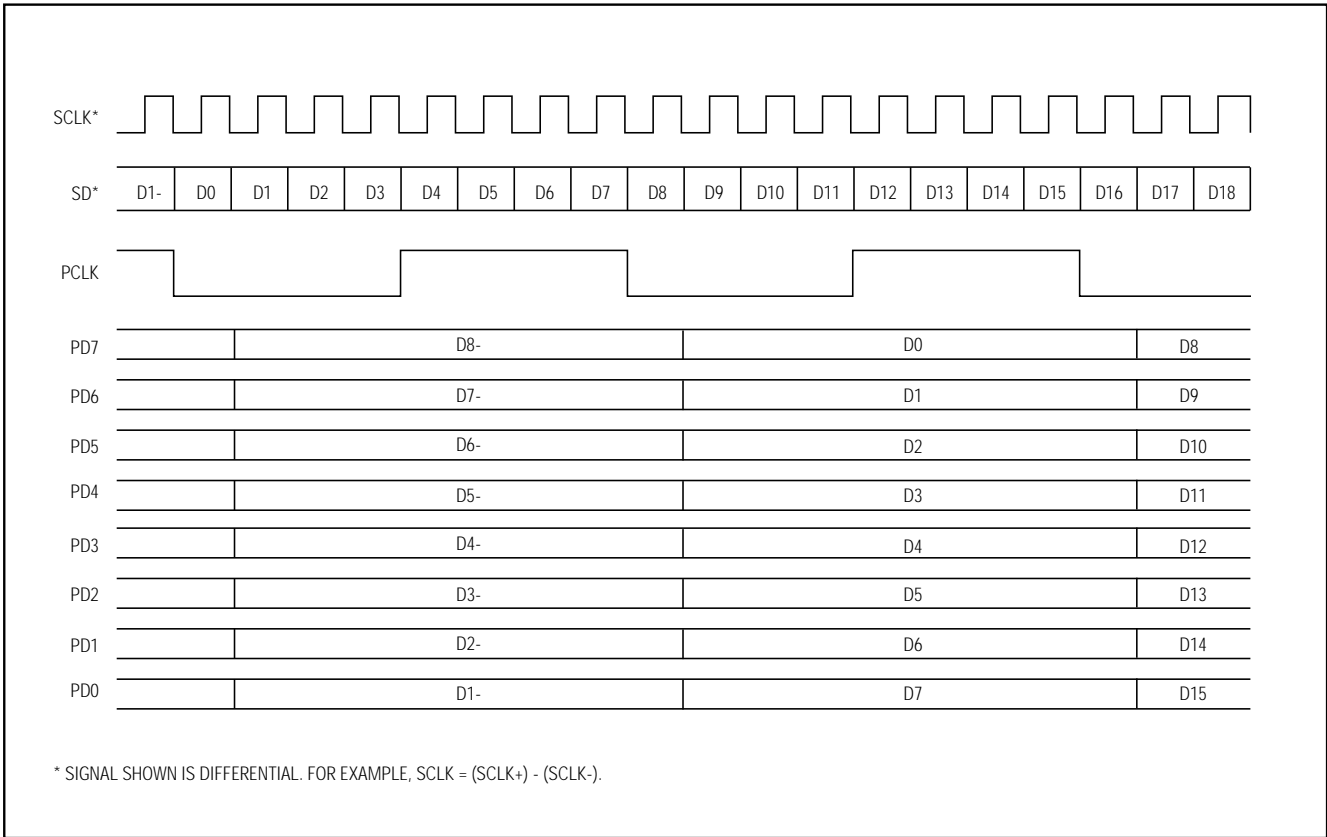


Figure 2a. Functional Timing Diagram—Normal Operation

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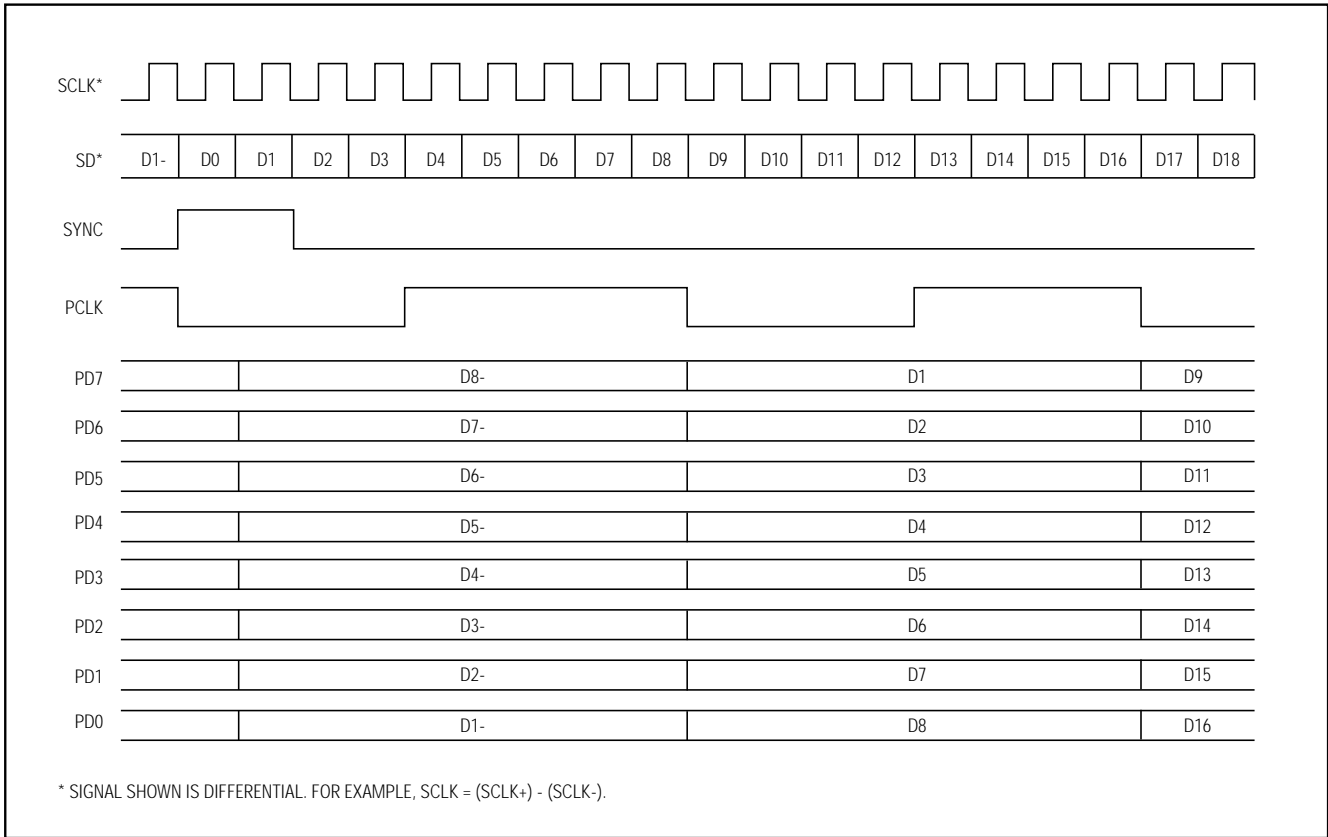


Figure 2b. Functional Timing Diagram—SYNC Operation

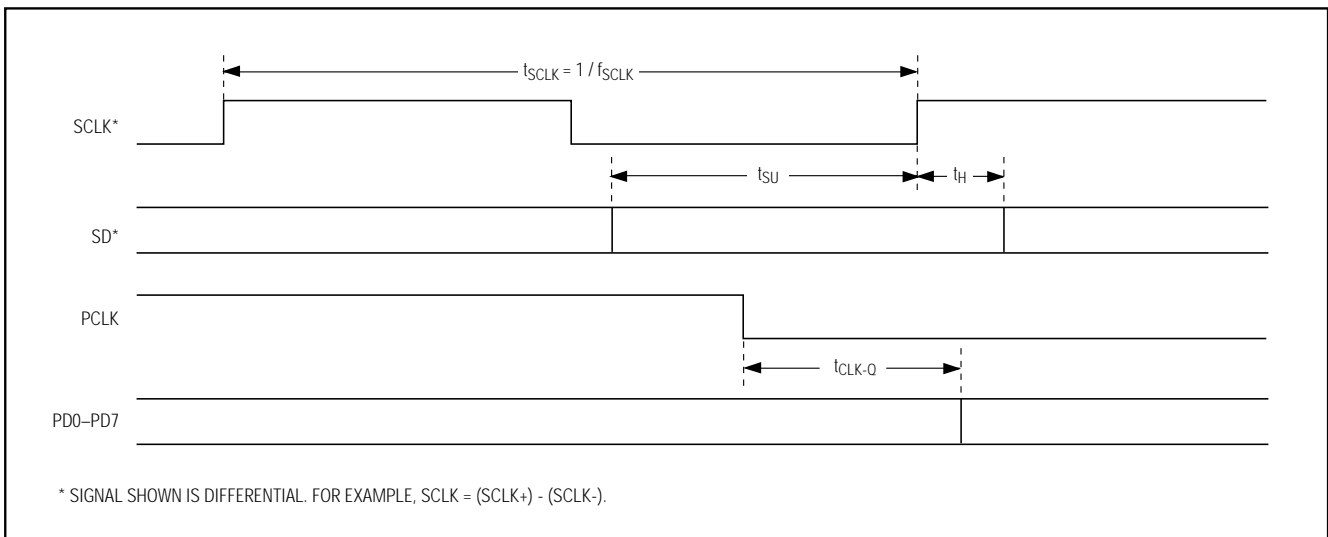


Figure 3. Timing Parameters

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## PECL Inputs

The serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require  $50\Omega$  termination to ( $V_{CC} - 2V$ ) when interfacing with a PECL source (see *Alternative PECL Input Termination*).

## Applications Information

### Alternative PECL Input Termination

Figure 4 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a ( $V_{CC} - 2V$ ) termination voltage is not available. If AC coupling is necessary, such as when interfacing with an ECL-output device, use the ECL AC-coupling termination.

### Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3680 data inputs.

## Pin Configuration

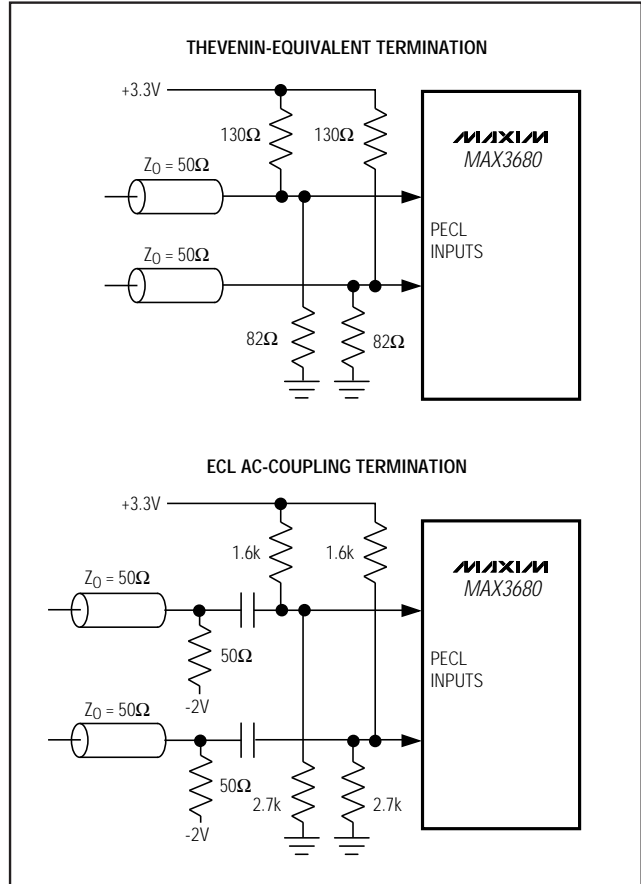
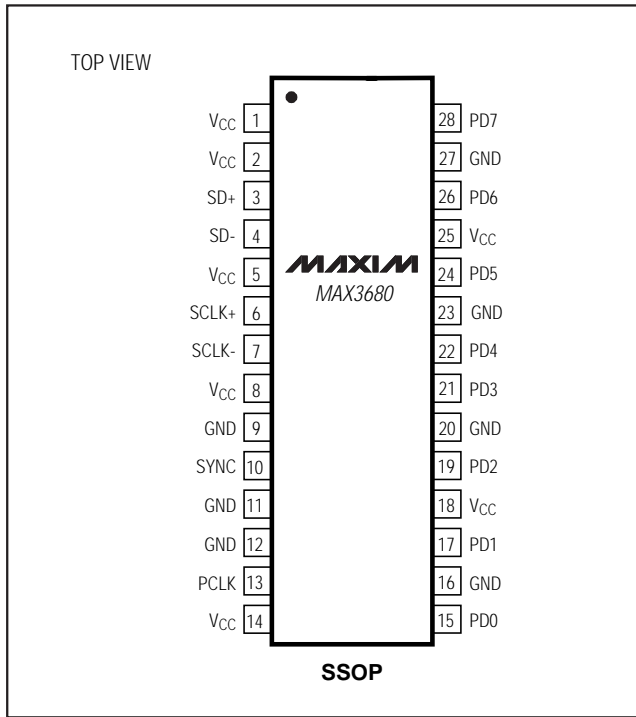


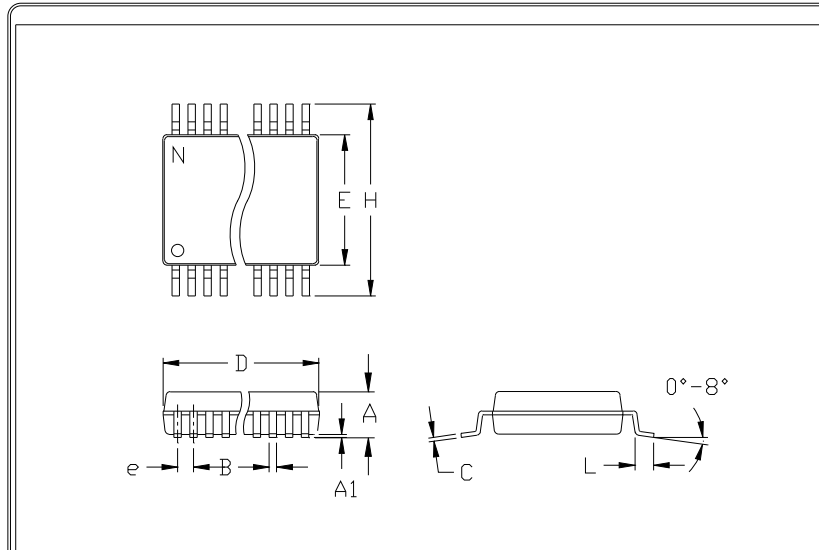
Figure 4. Alternative PECL Input Termination

## Chip Information

TRANSISTOR COUNT: 1346

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## Package Information



\*\*\*ADDED TO SSOP.DWG FILE\*\*\*

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
e	0.0256		0.65	
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95

	INCHES		MILLIMETERS		N
	MIN	MAX	MIN	MAX	
D	0.278	0.289	7.07	7.33	20
D	0.317	0.328	8.07	8.33	24
D	0.397	0.407	10.07	10.33	28

- NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
  2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
  3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
  4. CONTROLLING DIMENSION: MILLIMETER
  5. N = NUMBER OF PINS

 <small>120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737-7754</small> <small>PROPRIETARY INFORMATION</small>	PACKAGE FAMILY OUTLINE: SSOP .200" x .65mm <small>TITLE</small>		21-0039	A
			<small>DOCUMENT CONTROL NUMBER</small>	<small>REV</small>

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