

EVALUATION KIT
AVAILABLE**MAXIM**

622Mbps, Low-Noise Transimpedance Pre-amplifier for LAN and WAN Optical Receivers

General Description

The MAX3760 is a transimpedance preamplifier for 622Mbps ATM applications. It operates from a single +5V supply and typically consumes only 100mW power. The preamplifier converts a small photodiode current to a differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion.

6.5k Ω transimpedance gain and 560MHz bandwidth, combined with low 73nA input-referred noise, provide -31.5dBm typical sensitivity in 1300nm receivers. The circuit accepts a 1mA_{p-p} input current, resulting in a typical optical overload of -3dBm. The device operates over an extended temperature range of -40°C to +85°C.

The MAX3760 is internally compensated and requires few external components. In die form it includes a space-saving filter connection, which provides positive bias for the photodiode through a 1k Ω resistor to V_{CC}. These features, combined with the die aspect ratio and dimensioning, allow the MAX3760 to assemble easily into a TO-style header with a photodiode.

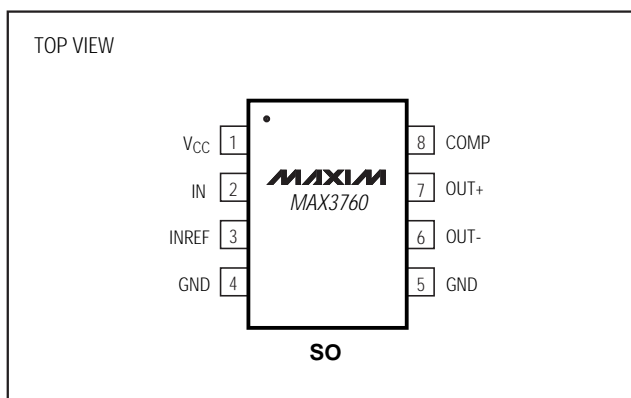
The MAX3760 is designed to be used with either the MAX3761 or the MAX3762 limiting-amplifier ICs. When combined with a photodiode, the chipset forms a complete 5V, 622Mbps receiver. The MAX3760 is available in die form and in an 8-pin SO package.

Applications

622Mbps ATM LAN Optical Receivers

622Mbps WAN Optical Receivers

Pin Configuration



Features

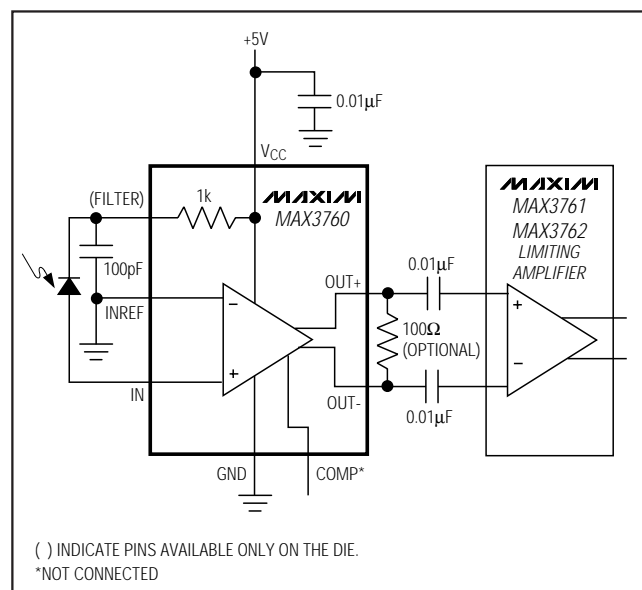
- ◆ 73nA RMS Input-Referred Noise
- ◆ 560MHz Bandwidth
- ◆ 1mA Peak Input Current
- ◆ 6.5k Ω Gain
- ◆ Operation from -40°C to +85°C
- ◆ 100mW Typical Power Consumption
- ◆ Single +5V Supply

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3760ESA	-40°C to +85°C	8 SO
MAX3760E/D	-40°C to +85°C	Dice*

*Dice are designed to operate over a -40°C to +100°C junction temperature (T_j) range, but are tested and guaranteed at $T_A = +25^\circ\text{C}$.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.5V to +7.0V	Continuous Power Dissipation (T _A = +85°C) SO (derate 5.88mW/°C above +85°C)	383mW
Continuous Current IN, FILTER	-5mA to +5mA	Storage Temperature Range	-65°C to +160°C
OUT+, OUT-	-25mA to +25mA	Lead Temperature (soldering, 10sec)	+300°C
Voltage at INREF	-0.5V to +0.5V	Operating Junction Temperature Range (die)	-55°C to +150°C
Voltage at COMP	-0.5V to (V _{CC} + 0.5V)	Processing Temperature (die)	+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, COMP = GND, 100Ω load between OUT+ and OUT-, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V _{IN}	Input = open		0.8	0.95	V
Supply Current	I _{CC}	Input = open		20	30	mA
Small-Signal Transimpedance	Z ₂₁	Differential output, input <10μA	5.2	6.5	7.8	kΩ
Output Common-Mode Level				V _{CC} - 2.0		V
Differential Output Offset	V _{OS}	I _{IN} = 500μA, COMP = open	-25		25	mV
Output Impedance (per side)	Z _{OUT}		40	50	60	Ω
Maximum Differential Output Voltage	V _{OUT(MAX)}	I _{IN} = 500μA, total peak-to-peak, differential signal		550	950	mV
FILTER Resistance	R _{FILTER}		800	1000	1200	Ω
Power-Supply Rejection Ratio	PSRR	f < 1MHz, referred to output	20	45		dB

Note 1: Dice are tested at T_A = +25°C.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, COMP = open, C_{IN} = 0.75pF, outputs terminated differentially into 100Ω, 8-pin SO package in MAX3760 EV kit, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW		455	565		MHz
Low-Frequency Cutoff		20μA average input current		50		kHz
Pulse-Width Distortion	PWD	(Note 4)		75	200	ps
RMS Noise Referred to Input	i _n	C _{IN} = 0.75pF (Notes 3, 5)		73	93.5	nA
Data-Dependent Jitter	DDJ			200		ps

Note 2: AC characteristics are guaranteed by design and characterization.

Note 3: C_{IN} is the source capacitance presented to the die. Includes package parasitic, photo diode, and parasitic interconnect capacitance.

Note 4: Input is a 622Mbps 1-0 pattern, signal amplitude = 0 to 1mA, extinction ratio (r_e) = 10.

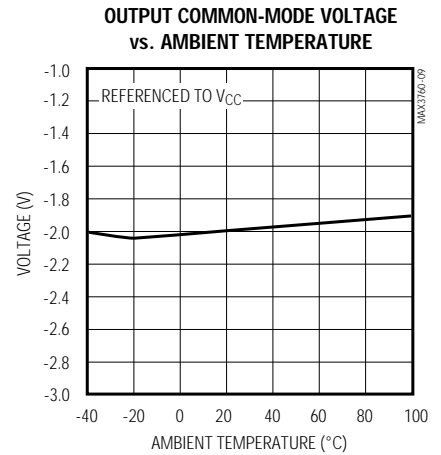
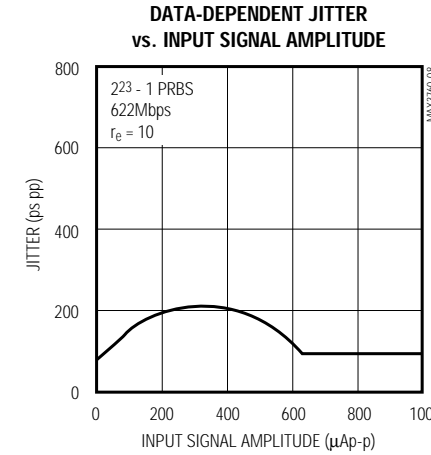
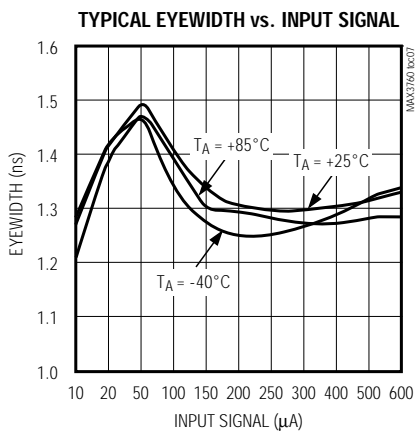
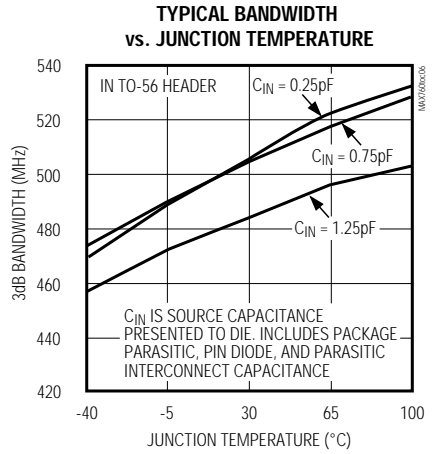
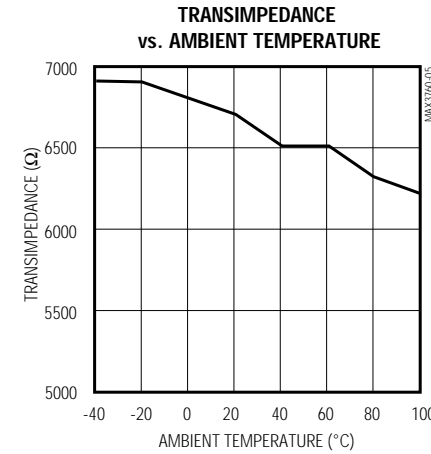
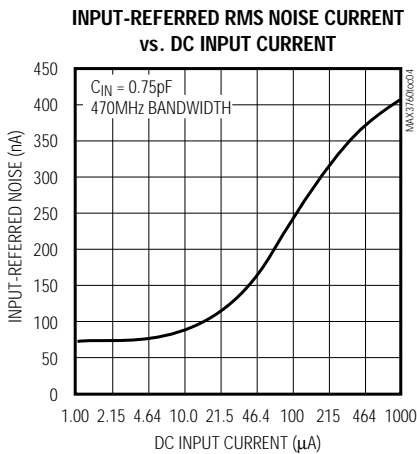
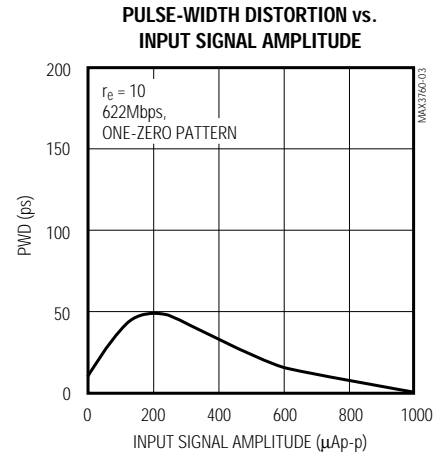
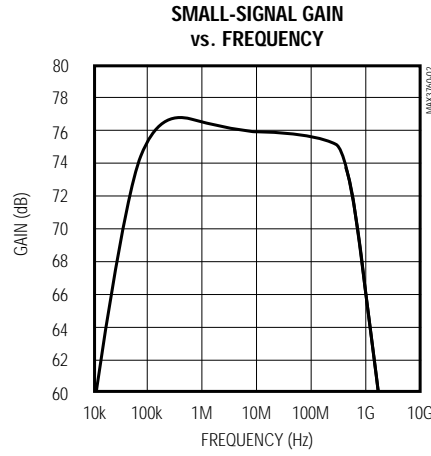
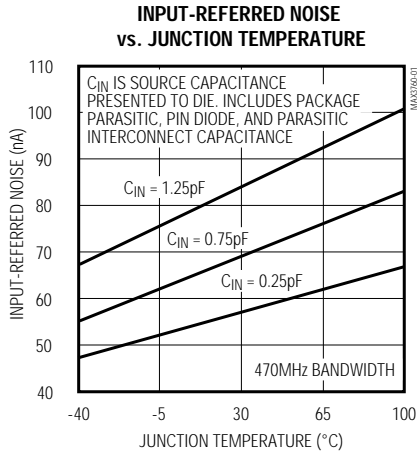
Note 5: Measured with a 4-pole, 470MHz Bessel filter.

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MAX3760

Typical Operating Characteristics

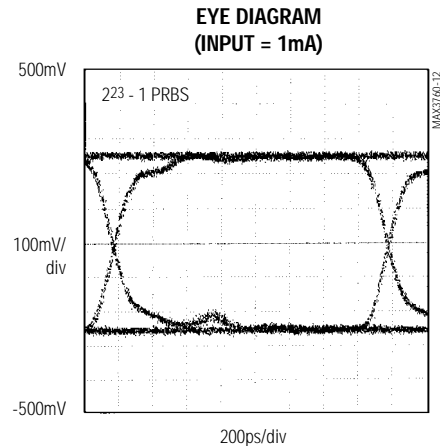
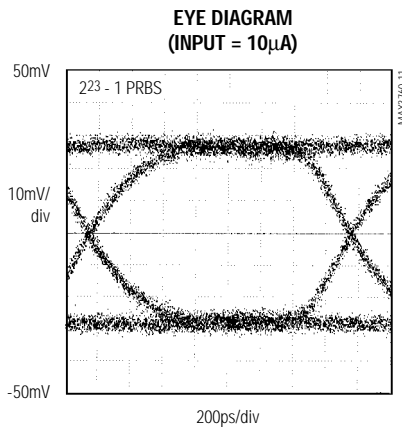
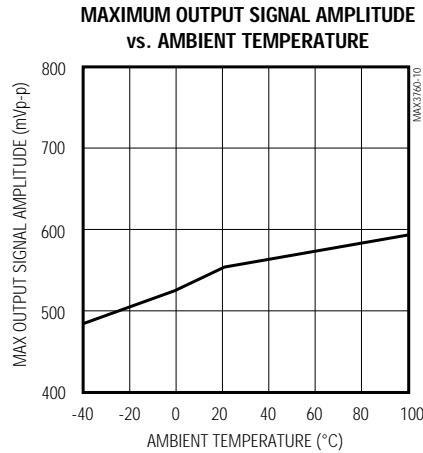
(MAX3760 EV kit, $V_{CC} = +5.0V$, COMP = open, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

(MAX3760 EV kit, $V_{CC} = +5.0V$, COMP = open, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	VCC	Supply-Voltage Input
2	IN	Signal Input
3	INREF	Input Reference Connection. Connect to photodetector AC ground.
4, 5	GND	Ground
6	OUT-	Inverting Voltage Output. Current flowing into the input causes OUT- to decrease.
7	OUT+	Noninverting Voltage Output. Current flowing into the input causes OUT+ to increase.
8	COMP	Compensation Capacitor Connection. Connection for optional external compensation capacitor for DC-cancellation circuit. Add capacitance here to reduce the low-frequency cutoff of the DC cancellation circuit. Connect COMP directly to GND to disable the DC cancellation circuit.
—	FILTER	Filter Connection. Provides positive bias for photodiode through a 1k Ω resistor to VCC (see the <i>Designing Filters</i> section). Available on the die only.

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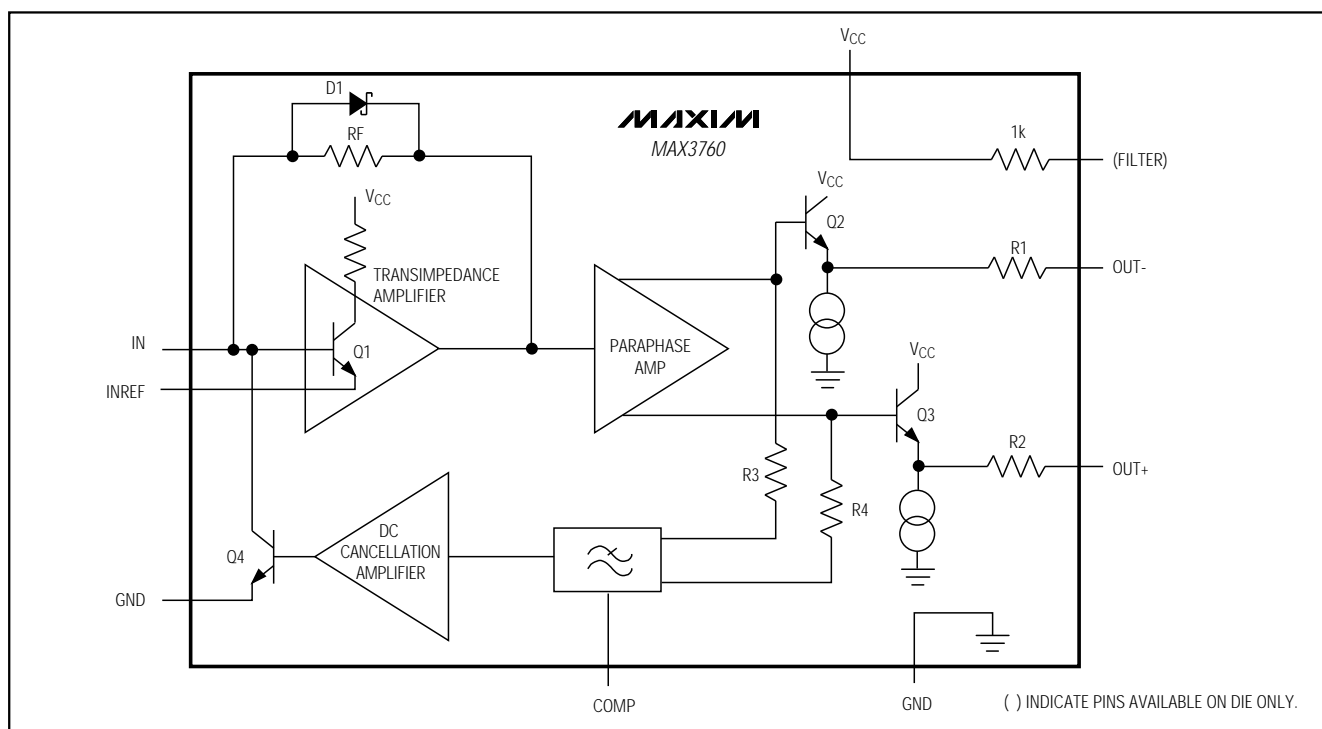


Figure 1. Functional Diagram

Detailed Description

The MAX3760 is a transimpedance amplifier designed for 622Mbps fiber optic applications. As shown in the Functional Diagram (Figure 1), it comprises a transimpedance amplifier, a paraphase amplifier with emitter-follower outputs, and a DC cancellation circuit.

Transimpedance Amplifier

The signal current at the input flows into a high-gain amplifier's summing node. Shunt feedback through RF converts this current to a voltage with $6.5\text{k}\Omega$ gain. Diode D1 clamps the output voltage for large input currents. INREF is a direct connection to the input transistor's emitter, and must be connected directly to the photodetector AC ground return for best performance.

Paraphase Amplifier

The paraphase amplifier converts single-ended signals to differential signals and introduces a voltage gain of 2. This signal drives a pair of internally biased emitter followers, Q2 and Q3, which form the output stage. Resistors R1 and R2 provide back-termination at the output, delivering a 100Ω differential output impedance. The output emitter followers are designed to drive a 100Ω differential load between OUT+ and OUT-. The MAX3760 can also

be terminated with higher output impedances for increased gain and output voltage swing. *The MAX3760 will not drive a 50Ω load to ground.* For best noise rejection, terminate the MAX3760 with differential loads.

DC Cancellation Circuit

The DC cancellation circuit removes the input signal's DC component by employing low-frequency feedback. This feature centers the input signal within the transimpedance amplifier's dynamic range, thereby reducing pulse-width distortion on large input signals.

The paraphase amplifier's output is sensed through resistors R3 and R4, then filtered, amplified, and fed back to the base of transistor Q4. The transistor draws the input signal's DC component away from the transimpedance amplifier's summing node.

The MAX3760 DC cancellation loop is internally compensated and does not require external capacitors in most 622Mbps applications. Add external capacitance at the COMP pin to reduce the DC cancellation circuit's frequency response and improve data-dependent jitter. Connecting the COMP pin directly to GND disables the circuit. The DC cancellation circuit can sink up to 1mA at the input.

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The MAX3760 minimizes pulse-width distortion for data sequences exhibiting a 50% duty cycle. A duty cycle significantly different from 50% will cause the MAX3760 to generate pulse-width distortion.

DC cancellation current is drawn from the input and creates noise. This is not a problem for low-level signals with little or no DC component. Preamplifier noise increases for signals with significant DC component (see *Typical Operating Characteristics*).

The MAX3760 operates with the photodetector cathode connected to VCC, as shown in the *Typical Application Circuit*. Connecting the photodetector anode to GND and the cathode to IN defeats the DC cancellation circuit and causes pulse-width distortion.

Input Reference

INREF is the reference point for IN. Connect it as close as possible to the photodetector diode's AC ground. The photodetector's AC ground is usually the ground of the photodetector's filter capacitor. The total length from INREF, through the filter capacitor and the diode, and back to the input should be no more than 2cm.

Applications Information

Optical Power Definitions

Many of the MAX3760's specifications relate to the input signal amplitude. When working with fiber optic receivers, the optical input is usually expressed in terms of average optical power and extinction ratio. Use the relations given in Table 1 to convert optical power to input signal when designing with the MAX3760.

Calculating Sensitivity, Overload, and Linear Range

Sensitivity Calculation

The MAX3760's input-referred RMS noise current (i_n) generally dominates the receiver sensitivity. In a system where the bit error rate (BER) is $1E-10$, the signal-to-noise ratio must always exceed 12.7. The sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{12.7i_n(r_e + 1)}{2\rho(r_e - 1)}1000\right)\text{dBm}$$

Where ρ is the photodiode responsivity in A/W.

Input Overload

The overload is the largest input that the MAX3760 accepts while meeting specifications. It is calculated as:

$$\text{Overload} = 10\log\left(\frac{1\text{mA}}{2\rho}1000\right)\text{dBm}$$

Linear Range

The MAX3760 has high gain, which limits the output when the input signal exceeds $20\mu\text{A}$ p-p. It operates with 90% linearity for inputs not exceeding the following:

$$10\log\left(\frac{20\mu\text{A}(r_e + 1)}{\rho(r_e - 1)}1000\right)\text{dBm}$$

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P_0 + P_1) / 2$
Extinction Ratio	r_e	$r_e = P_1 / P_0$
Optical Power of a "1"	P_1	$P_1 = 2P_{AVE} \frac{r_e}{(r_e + 1)}$
Optical Power of a "0"	P_0	$P_0 = 2P_{AVE} / (r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P_1 - P_0 = 2P_{AVE} \frac{(r_e - 1)}{(r_e + 1)}$

Note: Assuming a 50% average input duty cycle.

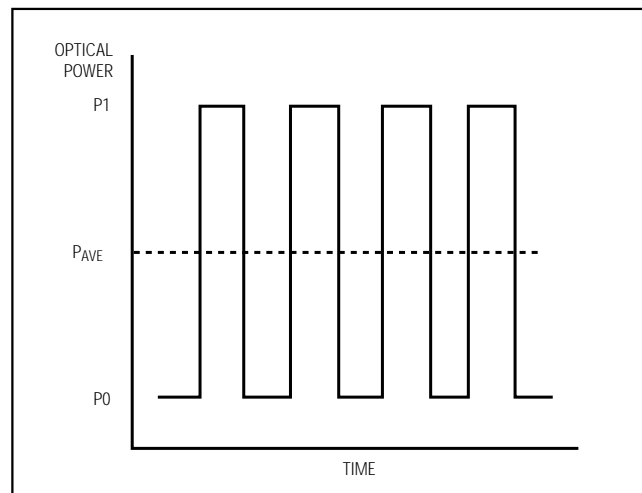


Figure 2. Optical Power Definitions

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Power Supply

The MAX3760 can operate from a power-supply voltage ($V_{CC} - GND$) between 4.5V and 5.5V. GND can be any stable voltage, including -5.0V, as found in many systems using ECL interface levels.

Layout Considerations

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and V_{CC} planes is recommended. Take care to bypass V_{CC} and to connect the GND pin to the ground plane with the shortest possible traces.

Designing a Low-Capacitance Input

Noise performance and bandwidth will be adversely affected by stray capacitance at IN. Make every effort to minimize capacitance on this node. Select a low-capacitance photodiode and use good high-frequency design and layout techniques. The MAX3760 is optimized for 0.75pF of capacitance on the input—approximately the capacitance of a low-cost photodetector packaged in a header.

When using the MAX3760 in the SO package, note that the package capacitance is about 0.3pF. The PC board between the MAX3760 input and the photodetector will add parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it.

For the best possible performance, assemble the MAX3760 in die form using chip-and-wire technology, or package the die in a TO header. These techniques minimize parasitic capacitance, resulting in the lowest noise.

Designing Filters

The MAX3760's noise performance is strongly affected by the circuit's bandwidth, which changes over temperature and varies from lot to lot. Receiver sensitivity can be improved by adding filters to limit this bandwidth. Filter designs range from a one-pole filter using a single capacitor to more complex filters using inductors. The simple filter provides a moderate rolloff with minimal components, while the complex filter provides a sharper rolloff and better transient response. A simple 530MHz filter can be created by placing a 6pF capacitor between the OUT+ and OUT- pins.

Supply-voltage noise at the photodiode cathode produces a current, $I = C_{PHOTO} \Delta V / \Delta t$, which reduces receiver sensitivity (C_{PHOTO} is the photodiode capacitance.) The MAX3760's FILTER resistor, combined with an external capacitor, can be used to reduce this noise (see *Typical Application Circuit*). Current generated by

supply-noise voltage is divided between C_{FILTER} and C_{PHOTO} . The input noise current due to supply noise is as follows (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILTER})(C_{FILTER})}$$

If the amount of tolerable noise is known, the filter capacitor is easy to select, as follows:

$$C_{FILTER} > \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILTER})(I_{NOISE})}$$

For example, with maximum noise voltage = 10mV_{RMS}, $C_{PHOTO} = 0.75\text{pF}$, $R_{FILTER} = 1\text{k}\Omega$, and I_{NOISE} selected to be 30nA (half the MAX3760's input noise):

$$C_{FILTER} = \frac{(10\text{mV})(0.75\text{pF})}{(1000)(30\text{E}-9)} = 250\text{pF}$$

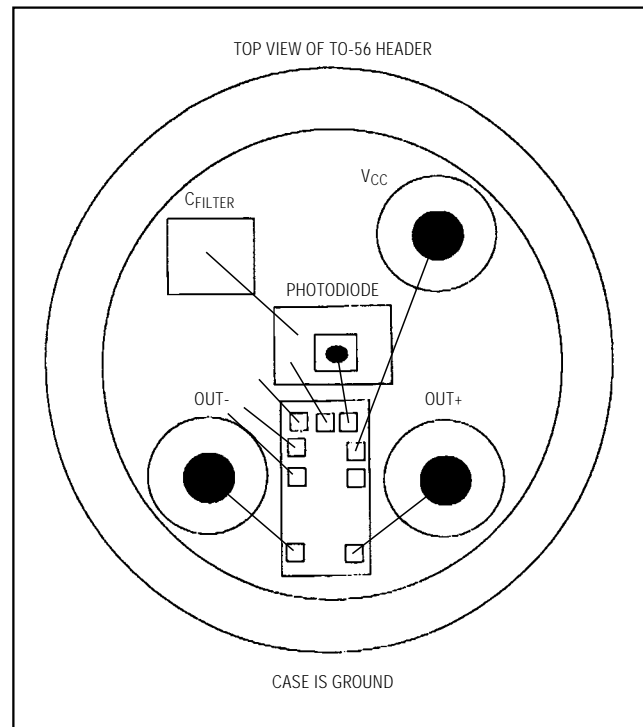


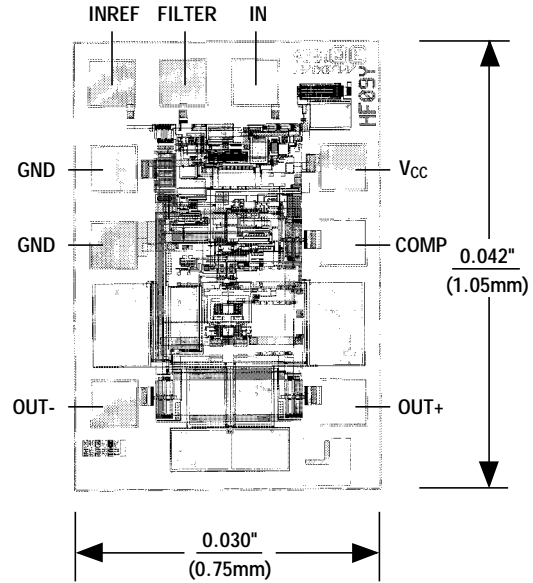
Figure 3. Suggested Layout for TO-56 Header

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Wire Bonding

For high current density and reliable operation, the MAX3760 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die-pad size is 4 mils square, with 6 mil pitch. Die thickness is 15 mils.

Chip Topography



TRANSISTOR COUNT: 131
SUBSTRATE CONNECTED TO GND

Package Information

INCHES		MILLIMETERS		
MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

INCHES		MILLIMETERS		N	MS012
MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8 A
D	0.337	0.344	8.55	8.75	14 B
D	0.386	0.394	9.80	10.00	16 C

NOTES:
 1. DBC DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
 4. CONTROLLING DIMENSION: MILLIMETER
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
 6. N = NUMBER OF PINS