19-0075; Rev. 5; 7/95

MAXIM

Microprocessor Supervisory Circuit

General Description

The MAX791 microprocessor (µP) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in µP systems. The 50µA supply current makes the MAX791 ideal for use in portable equipment, while the 6ns chip-enable propagation delay and 250mA output capability (25mA in battery-backup mode) make it suitable for larger, higher-performance equipment.

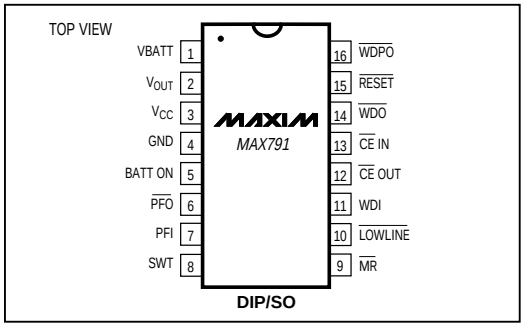
The MAX791 comes in 16-pin DIP and narrow SO packages and provides the following functions:

1) µP reset—$\overline{\text{RESET}}$ output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for V_{CC} down to 1V, even with no battery in the circuit.
2) Manual-reset input.
3) A 1.25V threshold detector provides for power-fail warning and low-battery detection, or monitors a power supply other than +5V.
4) Two-stage power-fail warning—a separate low-line comparator compares V_{CC} to a threshold 150mV above the reset threshold.
5) Backup-battery switchover for CMOS RAM, real-time clocks, µPs, or other low-power logic.
6) Software monitoring of backup-battery voltage.
7) A watchdog-fault output is asserted if the watchdog input has not been toggled within either a preset or an adjustable timeout period.
8) Write protection of CMOS RAM or EEPROM.
9) Pulsed watchdog output, to give advance warning of impending $\overline{\text{WDO}}$ assertion caused by watchdog timeout.

Applications

Computers — Critical µP Power Monitoring
Controllers — Intelligent Instruments
Portable/Battery-Powered Equipment

Pin Configuration



Features

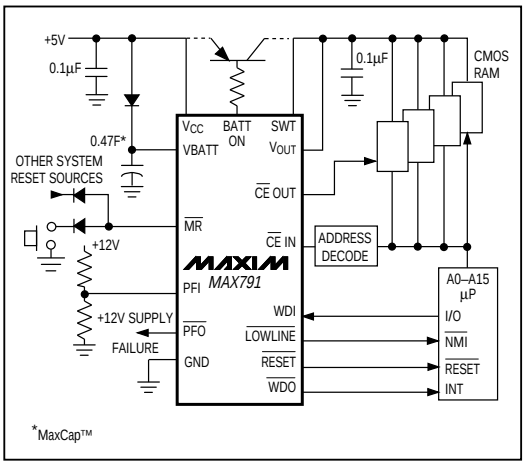
- **Precision 4.65V Voltage Monitoring**
- **200ms Power-OK/Reset Time Delay**
- **Independent Watchdog Timer—Preset or Adjustable**
- **1µA Standby Current**
- **Power Switching**
  - **250mA Output in V_{CC} Mode**
  - **25mA Output in Battery-Backup Mode**
- **On-Board Gating of Chip-Enable Signals**
  - **Memory Write-Cycle Completion**
  - **6ns CE Gate Propagation Delay**
- **MaxCap™ or SuperCap™ Compatible**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Backup-Battery Monitor**
- **Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX791CPE	0°C to +70°C	16 Plastic DIP
MAX791CSE	0°C to +70°C	16 Narrow SO
MAX791C/D	0°C to +70°C	Dice*
MAX791EPE	-40°C to +85°C	16 Plastic DIP
MAX791ESE	-40°C to +85°C	16 Narrow SO
MAX791EJE	-40°C to +85°C	16 CERDIP
MAX791MJE	-55°C to +125°C	16 CERDIP

** Dice are specified at T_A = +25°C.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to + 6V
- All Other Inputs ..... -0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous 25mA
- GND, BATT ON 100mA
- All Other Outputs 25mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above +70°C) 696mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges
- MAX791C_ _ ..... O°C to +70°C
- MAX791E_ _ ..... -40°C to +85°C
- MAX791MJE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, VBATT (Note 1)				0		5.5	V
V_{OUT} in Normal Operating Mode	V_{CC} = 4.5V	I_{OUT} = 25mA		V_{CC} - 0.05	V_{CC} - 0.02		V
		I_{OUT} = 250mA	MAX791C/E	V_{CC} - 0.3	V_{CC} - 0.2		
			MAX791M	V_{CC} - 0.40			
	V_{CC} = 3V, VBATT = 2.8V, I_{OUT} = 100mA			V_{CC} - 0.2	V_{CC} - 0.12		
V_{CC}-to-V_{OUT} On-Resistance	V_{CC} = 4.5V	MAX791C/E			0.8	1.2	Ω
		MAX791M			0.8	1.6	
	V_{CC} = 3V				1.2	2.0	
V_{OUT} in Battery-Backup Mode	VBATT = 4.5V, I_{OUT} = 20mA			VBATT - 0.3			V
	VBATT = 2.8V, I_{OUT} = 10mA			VBATT - 0.25			
	VBATT = 2.0V, I_{OUT} = 5mA			VBATT - 0.15			
VBATT-to-V_{OUT} On-Resistance	VBATT = 4.5V				8	15	Ω
	VBATT = 2.8V				13	25	
	VBATT = 2.0V				17	30	
Supply Current in Normal Operating Mode (Excludes I_{OUT})	V_{CC} > VBATT - 1V				50	150	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT}) (Note 2)	V_{CC} < VBATT - 1.2V, VBATT = 2.8V	T_A = +25°C			0.04	1	µA
		T_A = T_{MIN} to T_{MAX}				5	
VBATT Standby Current (Note 3)	VBATT + 0.2V ≤ V_{CC}	T_A = +25°C		-0.1		0.02	µA
		T_A = T_{MIN} to T_{MAX}		-1.0		0.02	
Battery-Switchover Threshold	Power up				VBATT + 0.03		V
	Power down				VBATT - 0.03		
Battery-Switchover Hysteresis					60		mV
Low-Battery Detector Threshold					2		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT ON Output Low Voltage	I_{SINK} = 3.2mA		0.1	0.4	V
	I_{SINK} = 25mA		0.7	1.5	
BATT ON Output Short-Circuit Current	Sink current		60		mA
	Source current	1	15	100	µA
RESET, LOW-LINE AND WATCHDOG TIMER					
$\overline{RESET}$ Threshold Voltage		4.50	4.65	4.75	V
$\overline{RESET}$ Threshold Hysteresis			15		mV
$\overline{LOWLINE}$-to-$\overline{RESET}$ Threshold Voltage			150		mV
V_{CC}-to-$\overline{RESET}$ Delay	Power down		100		µs
V_{CC}-to-$\overline{LOWLINE}$ Delay	Power down		80		µs
$\overline{RESET}$ Active Timeout Period	Power up	140	200	280	ms
Watchdog Timeout Period	SWT connected to V_{OUT}	1.0	1.6	2.25	sec
Minimum Watchdog Timeout Period	4.7nF capacitor connected from SWT to GND		10		ms
Minimum Watchdog Input Pulse Width	V_{IL} = 0.8V, V_{IH} = 0.75 x V_{CC}	100			ns
$\overline{WDPO}$ Pulse Width			1		ms
$\overline{WDPO}$-to-$\overline{WDO}$ Delay			70		ns
$\overline{RESET}$ Output Voltage	MAX791C, I_{SINK} = 50µA, V_{CC} = 1.0V, V_{CC} falling		0.004	0.3	V
	MAX791E/M, I_{SINK} = 50µA, V_{CC} = 1.2V, V_{CC} falling		0.004	0.3	
	I_{SINK} = 3.2mA, V_{CC} = 4.25V		0.1	0.4	
	I_{SOURCE} = 1.6mA, V_{CC} = 5V	3.5			
$\overline{RESET}$ Output Short-Circuit Current	Output source current		7	20	mA
$\overline{LOWLINE}$ Output Voltage	I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{LOWLINE}$ Output Short-Circuit Current	Output source current		15	100	µA
$\overline{WDO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 500µA, V_{CC} = 5V	3.5			
$\overline{WDO}$ Output Short-Circuit Current	Output source current		3	10	mA
$\overline{WDPO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1mA	3.5			
$\overline{WDPO}$ Output Short-Circuit Current	Output source current		7	20	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, VBATT = 2.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WDI Threshold Voltage (Note 4)	V_{IH}	0.75 x V_{CC}			V
	V_{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		µA
	WDI = V_{OUT}		20	50	
POWER-FAIL COMPARATOR					
PFI Input Threshold	V_{CC} = 5V	1.20	1.25	1.30	V
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{PFO}$ Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	µA
PFI-to-$\overline{PFO}$ Delay	V_{IN} = -20mV, V_{OD} = 15mV		15		µs
	V_{IN} = 20mV, V_{OD} = 15mV		55		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disabled mode		±0.005	±1	µA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Resistance (Note 5)	Enabled mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disabled mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Propagation Delay (Note 6)	50Ω source impedance driver, C_{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V_{CC} = 5V, I_{OUT} = -100µA	3.5			V
	V_{CC} = 0V, VBATT = 2.8V, I_{OUT} = 1µA	2.7			
$\overline{RESET}$-to-$\overline{CE}$ OUT Delay	Power down		15		µs
MANUAL RESET INPUT					
$\overline{MR}$ Minimum Pulse Width		25	15		µs
$\overline{MR}$-to -$\overline{RESET}$ Propagation Delay			7		µs
$\overline{MR}$ Threshold	V_{CC} = 5V		1.25		V
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V		23	250	µA

Note 1: Either V_{CC} or VBATT can go to 0V, if the other is greater than 2.0V.

Note 2: The supply current drawn by the MAX791 from the battery (excluding I_{OUT}) typically goes to 10µA when (VBATT - 1V) < V_{CC} < VBATT. In most applications, this is a brief period as V_{CC} falls through this region.

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

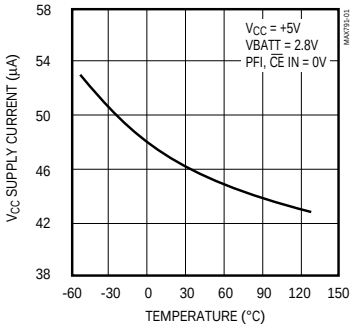
Note 5: The chip-enable resistance is tested with V_{CC} = 4.75V V $\overline{CE}$ IN = V $\overline{CE}$ OUT = V_{CC} / 2.

Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

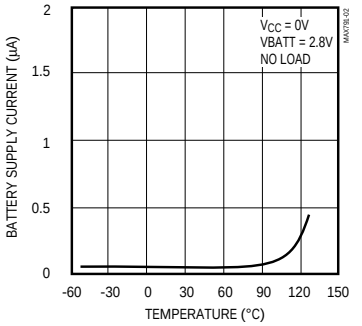
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

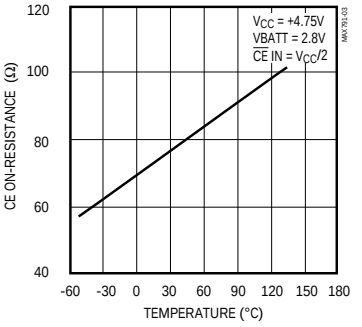
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



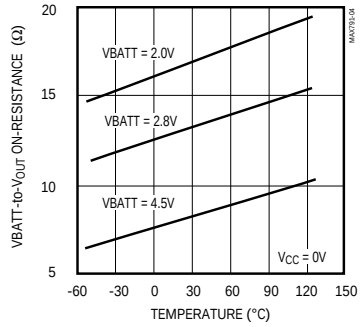
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



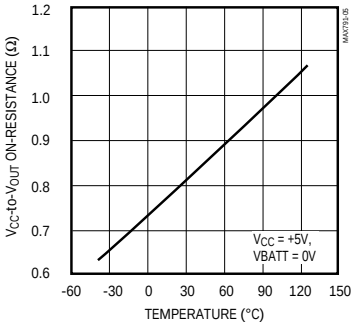
CHIP-ENABLE ON-RESISTANCE vs. TEMPERATURE



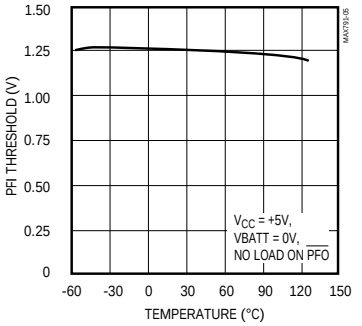
VBATT-to-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



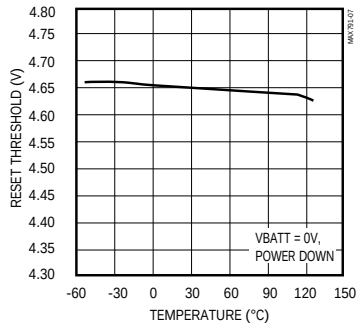
V_{CC}-to-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



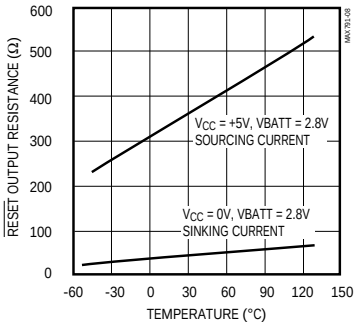
PFI THRESHOLD vs. TEMPERATURE



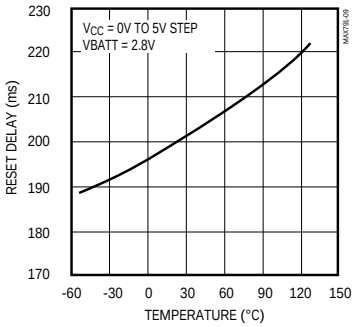
RESET THRESHOLD vs. TEMPERATURE



$\overline{RESET}$ OUTPUT RESISTANCE vs. TEMPERATURE



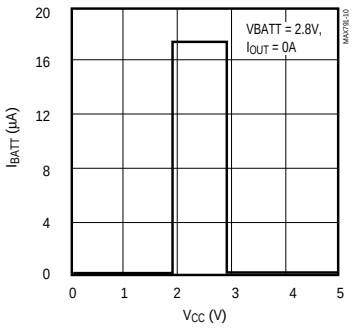
RESET DELAY vs. TEMPERATURE



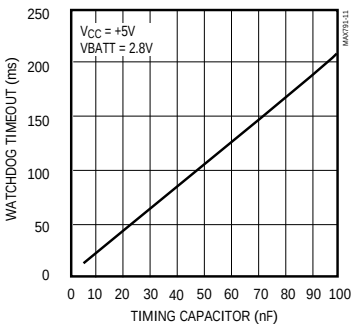
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

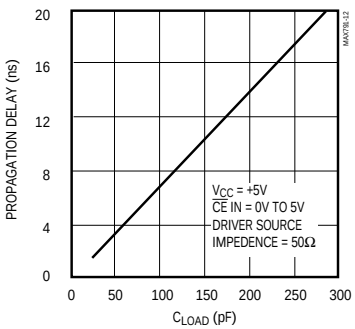
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



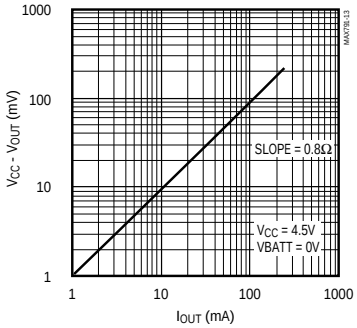
WATCHDOG TIMEOUT vs. TIMING CAPACITOR



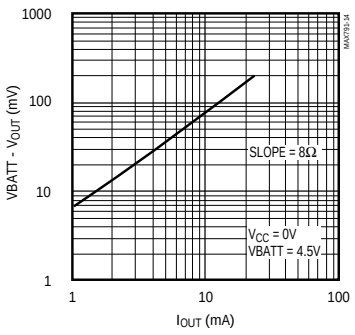
CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



V_{CC} to V_{OUT} vs. OUTPUT CURRENT



VBATT to V_{OUT} vs. OUTPUT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	VBATT	Backup-Battery Input. Connect to external battery or capacitor and charging circuit.
2	V_{OUT}	Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than VBATT and V_{CC} is above the reset threshold. When V_{CC} falls below VBATT and V_{CC} is below the reset threshold, V_{OUT} connects to VBATT. Connect a 0.1µF capacitor from V_{OUT} to GND.
3	V_{CC}	Input Supply Voltage—+5V input
4	GND	Ground. 0V reference for all signals
5	BATT ON	Battery On Output. Goes high when V_{OUT} switches to VBATT. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.
6	$\overline{PFO}$	Power-Fail Output. This is the output of the power-fail comparator. $\overline{PFO}$ goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.
7	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.
8	SWT	Set Watchdog-Timeout Input. Connect this input to V_{OUT} to select the default 1.6sec watchdog timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog-timeout period = 2.1 x (capacitor value in nF) ms.
9	$\overline{MR}$	Manual-Reset Input. This input can be tied to an external momentary pushbutton switch, or to a logic gate output. $\overline{RESET}$ remains low as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high.
10	$\overline{LOWLINE}$	$\overline{LOWLINE}$ Output goes low when V_{CC} falls to 150mV above the reset threshold. The output can be used to generate an NMI if the unregulated supply is inaccessible.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{WDO}$ goes low. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.
12	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 15µs or until $\overline{CE}$ IN goes high, whichever occurs first.
13	$\overline{CE}$ IN	Chip-Enable Input. The input to chip-enable gating circuit. Connect to GND or V_{OUT} if not used.
14	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transition at WDI. $\overline{WDO}$ remains high if WDI is unconnected. $\overline{WDO}$ is also high when $\overline{RESET}$ is asserted.
15	$\overline{RESET}$	$\overline{RESET}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{RESET}$ will remain low for typically 200ms after V_{CC} crosses the reset threshold on power-up.
16	$\overline{WDPO}$	Watchdog-Pulse Output. Upon the absence of a transition at WDI, $\overline{WDPO}$ will pulse low for a minimum of 1ms. $\overline{WDPO}$ precedes $\overline{WDO}$ by 70ns.

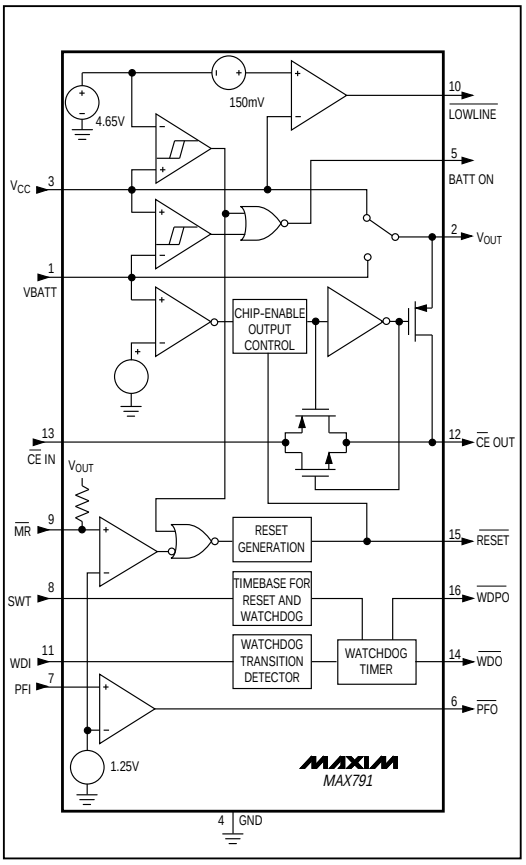


Figure 1. Block Diagram

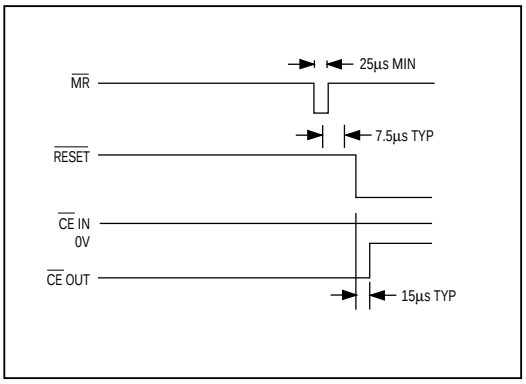


Figure 2. Manual-Reset Timing Diagram

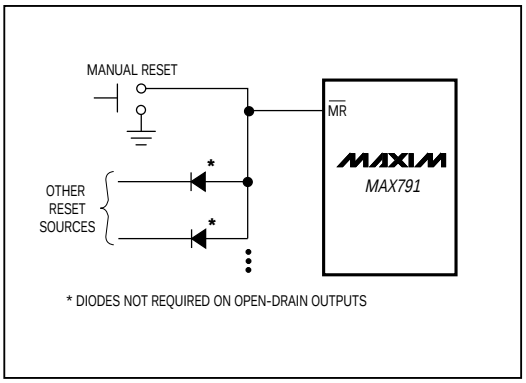


Figure 3. Diode "OR" connections allow multiple reset sources to connect to MR.

Detailed Description

Manual Reset Input

Many µP-based products require manual-reset capability, allowing the operator or test technician to initiate a reset. The Manual Reset Input (MR) can be connected directly to a switch, without an external pull-up resistor or debouncing network. It connects to a 1.25V comparator, and has a pull-up to V_{OUT} as shown in Figure 1. The propagation delay from asserting MR to RESET asserted is 4µs typical. Pulsing MR low for a minimum of 15µs resets all the internal counters, sets the Watchdog Output (WDO) and Watchdog-Pulse Output (WDPO) high, and sets the Set Watchdog-Timeout (SWT) input to V_{OUT} - 0.6V, if it is not already connected to V_{OUT} (for internal timeouts). It also disables the chip-enable function, setting the Chip-Enable Output (CE OUT) to a high state. The RESET output remains active as long as MR is held low, and the reset-timeout period begins after MR returns high (Figure 2).

Use this input as either a digital-logic input or a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes (Figure 3), and open-drain/collector outputs can be wire-ORed directly.

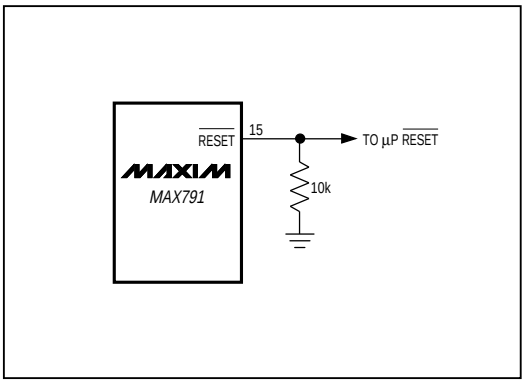


Figure 4. Adding an external pull-down resistor ensures RESET is valid with V_{CC} down to GND.

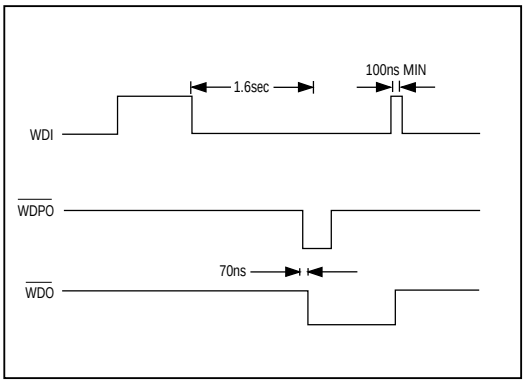


Figure 5. WDI, WDO and WDPO Timing Diagram (V_{CC} mode)

RESET Output

The MAX791's RESET output ensures that the µP powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The RESET output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, RESET sources 1.6mA at typically V_{OUT} - 0.5V. When no backup battery is used, RESET output is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on RESET ensures that RESET will be valid with V_{CC} down to GND (Figure 4). As V_{CC} goes below 1V, the gate drive to the RESET output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor ensures the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for the RESET output with V_{CC} = 4.75V is 4.5V typical. For battery voltages ≥ 2V connected to VBATT, RESET remains valid for V_{CC} from 0V to 5.5V.

RESET will be asserted during the following conditions:

1) V_{CC} < 4.65V (typ)
2) MR < 1.25V (typ)
3) RESET remains asserted for 200ms (typ) after V_{CC} rises above 4.65V or after MR has exceeded 1.25V.

The MAX791 battery-switchover comparator does not affect RESET assertion. However, RESET is asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, WDO and WDPO are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), WDPO and WDO are asserted, indicating a software fault condition (see *Watchdog Output* and *Watchdog-Pulse Output* sections).

Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at WDI during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6sec. Select alternative timeout periods by connecting an external capacitor from SWT to GND (see *Selecting an Alternative Watchdog Timeout* section).

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog-timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watch-

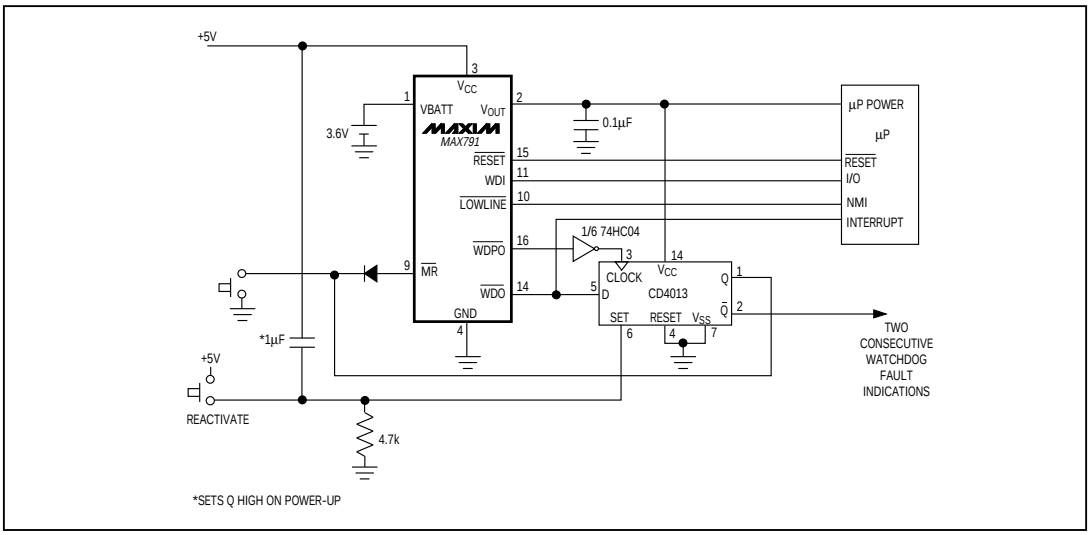


Figure 6. Two consecutive watchdog faults latch the system in reset.

dog-timeout period, $\overline{WDO}$ goes low 70ns after the falling edge of $\overline{WDPO}$ and remains low until the next transition at WDI (Figure 5). A flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults (Figure 6). $\overline{WDO}$ has a 2 x TTL output characteristic.

Watchdog-Pulse Output

As described in the preceding section, $\overline{WDPO}$ can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog-timeout period, $\overline{WDPO}$ will pulse low for 1ms. The falling edge of $\overline{WDPO}$ precedes $\overline{WDO}$ by 70ns. Since $\overline{WDO}$ is high when $\overline{WDPO}$ goes low, the flip-flop's Q output remains high as $\overline{WDO}$ goes low (Figure 5). If the watchdog timer is not reset by a transition at WDI, $\overline{WDO}$ remains low and $\overline{WDPO}$ clocks a logic low to the Q output, causing the MAX791 to latch in reset. If the watchdog timer is reset by a transition at WDI, $\overline{WDO}$ goes high and the flip-flop's Q output remains high. Thus, a system shutdown is only caused by two successive watchdog faults.

The internal pull-up resistors associated with $\overline{WDO}$ and $\overline{WDPO}$ connect to V_{OUT}. Therefore, do not connect these outputs directly to CMOS logic that is powered from V_{CC} since, in the absence of V_{CC} (i.e., battery mode), excessive current will flow from $\overline{WDO}$ or $\overline{WDPO}$ through the protection diode(s) of the CMOS-logic inputs to ground.

Selecting an Alternative Watchdog Timeout Period

SWT input controls the watchdog-timeout period. Connecting SWT to V_{OUT} selects the internal 1.6sec watchdog-timeout period. Select an alternative timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating, and do not connect it to ground. The following formula determines the watchdog-timeout period:

Watchdog Timeout Period = 2.1 x (capacitor value in nF) ms

This formula is valid for capacitance values between 4.7nF and 100nF (see the Watchdog Timeout vs. Timing Capacitor graph in the *Typical Operating Characteristics*). SWT is internally connected to a ±100nA (typ) current source, which charges and discharges the timing capacitor to create the oscillator frequency that sets the watchdog timeout period (see *Connecting a Timing Capacitor to SWT* in the *Applications Information* section).

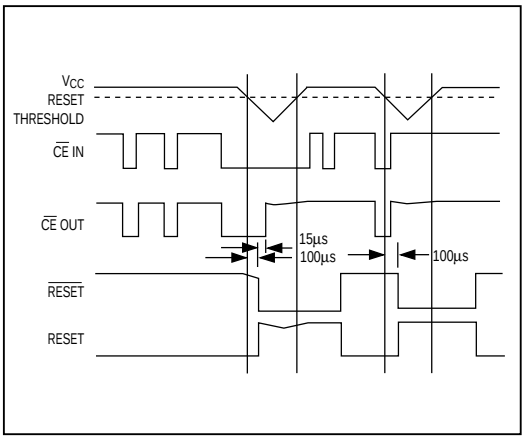


Figure 7. Reset and Chip-Enable Timing

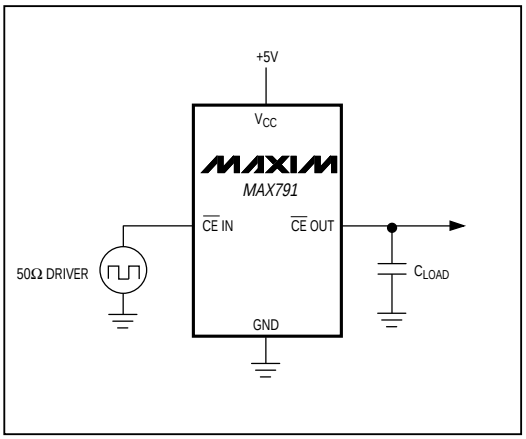


Figure 8. CE Propagation Delay Test Circuit

Chip-Enable Signal Gating

The MAX791 provides internal gating of chip-enable (CE) signals, to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX791 uses a series transmission gate from the Chip-Enable Input ($\overline{CE}$ IN) to $\overline{CE}$ OUT (Figure 1).

The 10ns max CE propagation from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX791 to be used with most µPs.

Chip-Enable Input

$\overline{CE}$ IN is high impedance (disabled mode) while $\overline{RESET}$ is asserted.

During a power-down sequence were V_{CC} passes 4.65V, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 7).

During a power-up sequence, $\overline{CE}$ IN remains high impedance, regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset-timeout period.

In the high-impedance mode, the leakage currents into this input are ±1µA max over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 8). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to V_{OUT}. This source turns off when the transmission gate is enabled.

$\overline{LOWLINE}$ Output

The low-line comparator monitors V_{CC} with a typical threshold voltage 150mV above the reset threshold, and has 15mV of hysteresis. $\overline{LOWLINE}$ typically sinks 3.2mA at 0.1V. For normal operation (V_{CC} above the $\overline{LOWLINE}$ threshold), $\overline{LOWLINE}$ is pulled to V_{OUT}. If access to the unregulated supply is unavailable, use $\overline{LOWLINE}$ to provide a nonmaskable interrupt (NMI) to the µP as V_{CC} begins to fall (Figure 9a).

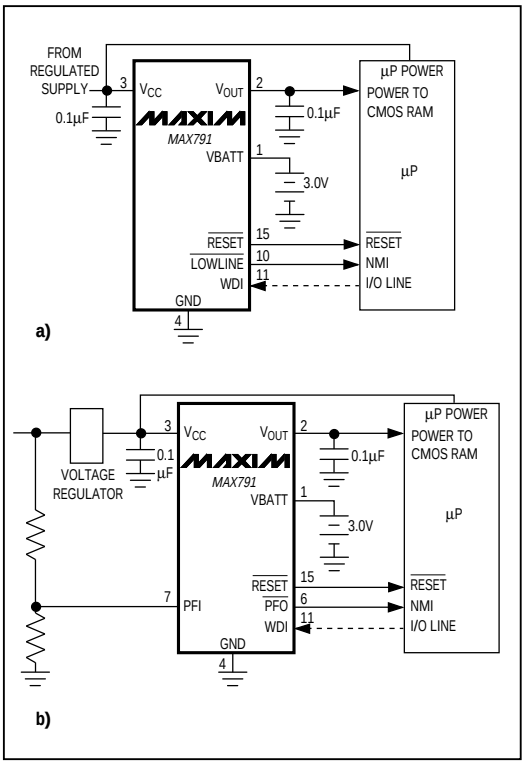


Figure 9. a) If the unregulated supply is inaccessible, LOWLINE generates the NMI for the µP. b) Use PFO to generate the µP NMI if the unregulated supply is inaccessible.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include monitoring supplies other than 5V (see the *Typical Operating Circuit* and the *Monitoring a Negative Voltage* section) and early power-fail detection when the unregulated power is easily accessible (Figure 9b).

Power-Fail Input

PFI is the input to the power-fail comparator. PFI has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 15µs from V_{IL} to V_{OL} (power failing), and 55µs from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

Table 1. Input and Output States in Battery-Backup Mode

PIN	NAME	STATUS
1	VBATT	Supply current is 1µA maximum.
2	V_{OUT}	V_{OUT} is connected to VBATT through an internal PMOS switch.
3	V_{CC}	Battery-switchover comparator monitors V_{CC} for active switchover.
4	GND	GND—0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V_{OUT}.
6	$\overline{PFO}$	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq$ VBATT - 1.2V typ. Below this voltage, $\overline{PFO}$ is forced low.
7	PFI	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq$ VBATT - 1.2V typ.
8	SWT	SWT is ignored.
9	$\overline{MR}$	$\overline{MR}$ is ignored.
10	$\overline{LOWLINE}$	Logic low*
11	WDI	WDI is ignored, and goes high impedance.
12	$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to V_{OUT}.
13	$\overline{CE}$ IN	High impedance
14	$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.
15	$\overline{RESET}$	Logic low*
16	$\overline{WDPO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.

* V_{CC} must be below the reset threshold to enter battery-backup mode.

Power-Fail Output

The Power-Fail Output ($\overline{PFO}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{PFO}$ is actively pulled to V_{OUT}. Connecting PFI through a voltage divider to an unregulated supply allows $\overline{PFO}$ to generate an NMI as the unregulated power begins to fall (Figure 9b). If the unregulated supply is inaccessible, use $\overline{LOWLINE}$ to generate the NMI. The $\overline{LOWLINE}$ threshold is typically 150mV above the reset threshold (see *LOWLINE Output* section).

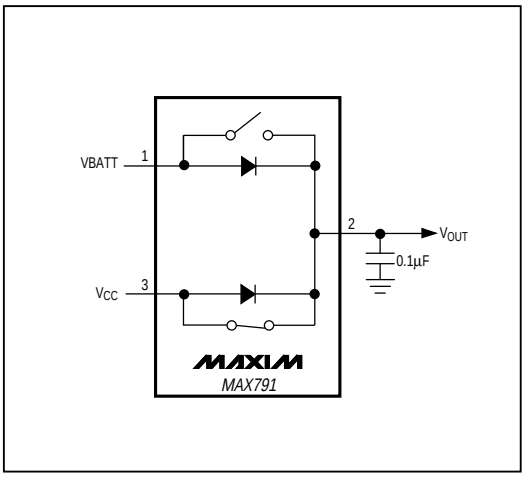


Figure 10. V_{CC} and VBATT-to-V_{OUT} Switch

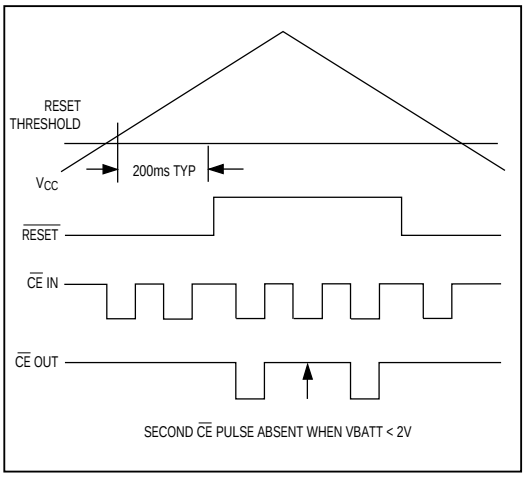


Figure 11. Backup-Battery Monitor Timing Diagram

Battery-Backup Mode

The MAX791 requires two conditions to switch to battery-backup mode: 1) V_{CC} must be below the reset threshold; 2) V_{CC} must be below VBATT. Table 1 lists the status of the inputs and outputs in battery-backup mode.

Battery On Output

The Battery On (BATT ON) output indicates the status of the internal V_{CC}/battery-switchover comparator, which controls the internal V_{CC} and VBATT switches. For V_{CC} greater that VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from V_{OUT}. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The Input Supply Voltage (V_{CC}) should be a regulated +5V. V_{CC} connects to V_{OUT} via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each (Figure 10). The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to V_{CC}, except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage.

Output Supply Voltage

The Output Supply Voltage (V_{OUT}) is internally connected to the substrate of the IC and supplies all the current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the V_{OUT} voltage in their high states rather than the V_{CC} voltage. At the maximum source current of 250mA, V_{OUT} will typically be 200mV below V_{CC}. Decouple this terminal with a 0.1µF capacitor.

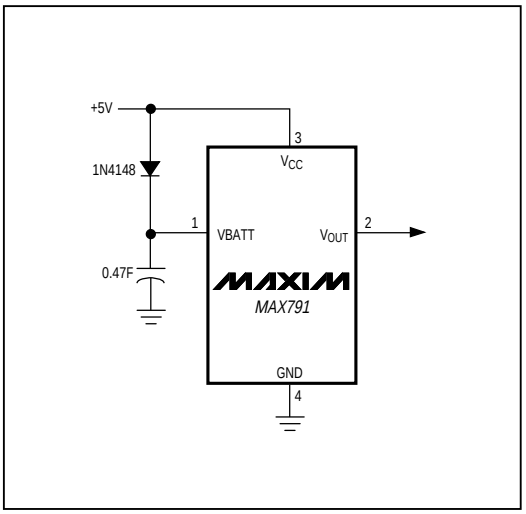


Figure 12. SuperCap or MaxCap on VBATT

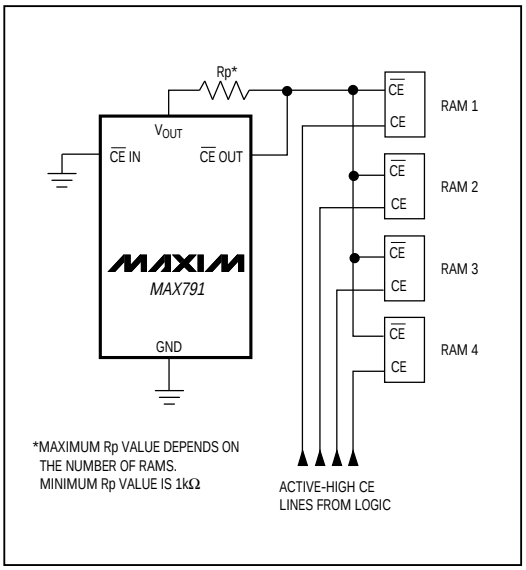


Figure 13. Alternate CE Gating

Low-Battery Monitor

The MAX791 low-battery voltage function monitors VBATT. Low-battery detection of 2.0V ±0.15V is monitored only during the reset-timeout period (200ms) that occurs either after a normal power-up sequence or after the $\overline{MR}$ reset input has been returned to its high state. If the battery voltage is below 2.0V, the second CE pulse is inhibited after reset timeout. If the battery voltage is above 2.0V, all CE pulses are allowed through the CE gate after the reset timeout period. To use this function, after the 200ms reset delay, write 00 (HEX) to a location using the first CE pulse, and write FF (HEX) to the same location using the second CE pulse following $\overline{RESET}$ going inactive on power-up. The contents of the memory then indicates a good battery (FF) or a low battery (00) (Figure 11).

Applications Information

The MAX791 is not short-circuit protected. Shorting V_{OUT} to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between V_{OUT} and GND rather than V_{CC} and GND.

If long leads connect to the chip inputs, ensure that these lines are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up. Typical supply current from V_{CC} is 60µA, while only leakage currents flow from the battery.
2) Battery-backup mode where V_{CC} is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60µA.
3) Battery-backup mode where V_{CC} is less than VBATT by at least 0.7V. VBATT supply current is than 1µA max.

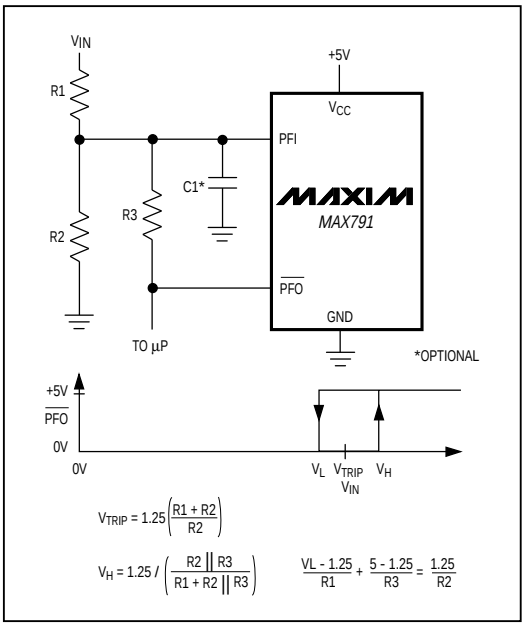


Figure 14. Adding Hysteresis to the Power-Fail Comparator

Using SuperCaps or MaxCaps with the MAX791

VBATT has the same operating voltage range as V_{CC}, and the battery-switchover threshold voltages are typically ±30mV centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 12).

If V_{CC} is above the reset threshold and VBATT is 0.5V above V_{CC}, current flows to V_{OUT} and V_{CC} from VBATT until the voltage at VBATT is less than 0.5V above V_{CC}. For example, with a SuperCap connected to VBATT and through a diode to V_{CC}, if V_{CC} quickly changes from 5.4V to 4.9V, the capacitor discharges through V_{OUT} and V_{CC} until VBATT reaches 5.3V typical. Leakage current through the SuperCap charging diode and MAX791 internal power diode eventually discharges the SuperCap to V_{CC}. Also, if V_{CC} and VBATT start from 0.5V above the reset threshold and power is lost at V_{CC}, the SuperCap on VBATT discharges through V_{CC} until VBATT reaches the reset threshold; the MAX791 then switches to battery-backup mode and the current through V_{CC} goes to zero (Figure 10).

Using Separate Power Supplies for VBATT and VCC

If using separate power supplies for V_{CC} and VBATT, VBATT must be less than 0.3V above V_{CC} when V_{CC} is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at V_{CC}, current flows continuously from VBATT to V_{CC} via the VBATT-to-V_{OUT} diode and the V_{OUT}-to-V_{CC} switch until the circuit is broken (Figure 10).

Alternative Chip-Enable Gating

Using memory devices with CE and $\overline{CE}$ inputs allows the MAX791 CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to V_{OUT}, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 13). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated by the MAX791.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when VIN is near the power-fail comparator trip point. Figure 14 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

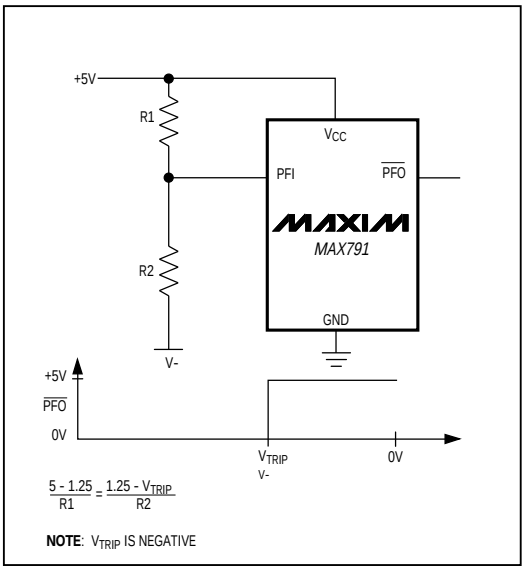


Figure 15. Monitoring a Negative Voltage

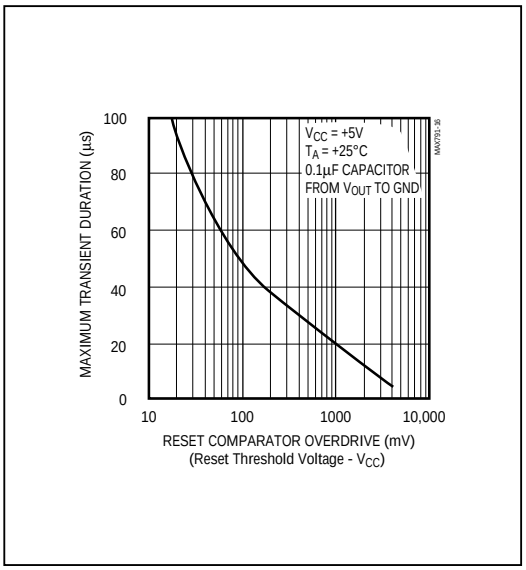


Figure 16. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 15's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

Backup-Battery Replacement

The backup battery may be disconnected while V_{CC} is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 16 shows maximum transient duration vs. reset comparator overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Connecting a Timing Capacitor to SWT

SWT is internally connected to a ±100nA current source. When a capacitor is connected from SWT to ground (to select an alternative watchdog timeout period), the current source charges and discharges the timing capacitor to create the oscillator that controls the watchdog timeout period. To prevent timing errors or oscillator start-up problems, minimize external current leakage sources at this pin, and locate the capacitor as close to SWT as possible. The sum of PC board leakage + SWT capacitor leakage must be small compared to ±100nA.

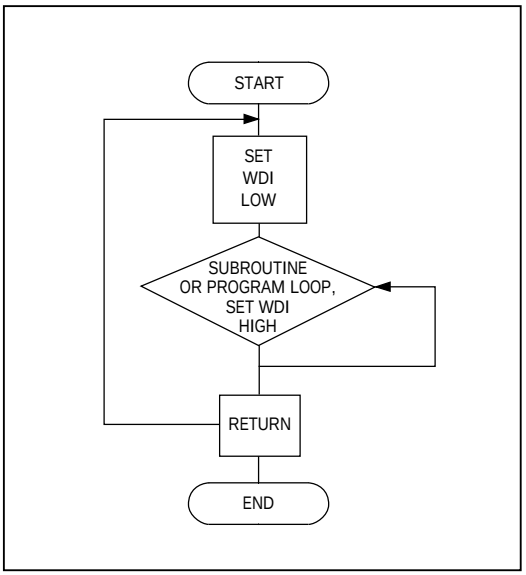


Figure 17. Watchdog Flow Diagram

Watchdog Software Considerations

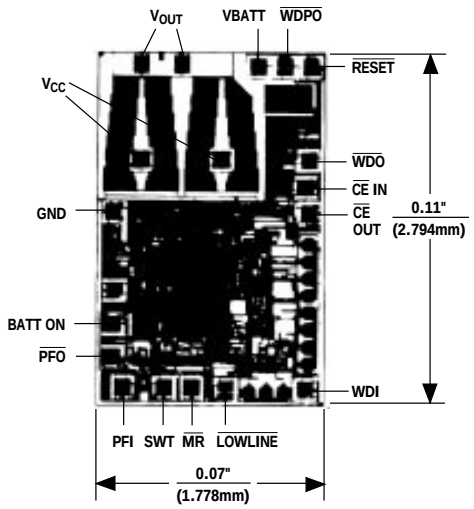
A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 17 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Maximum V_{CC} Fall Time

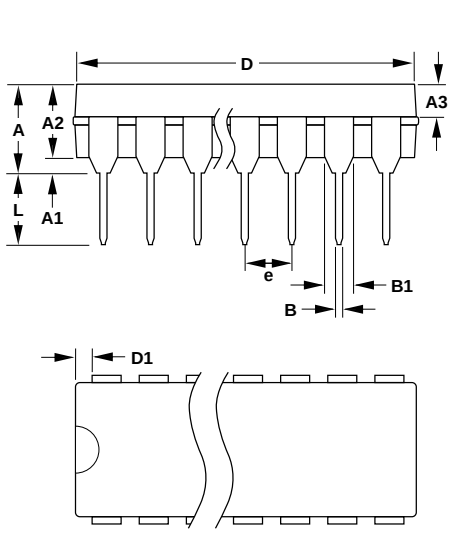
The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule of thumb for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse or 1A / 100µF = 0.01V/µs. The V_{CC} fall rate decreases with time as V_{CC} falls exponentially, which more than satisfies the maximum fall-time requirement.

Chip Topography



SUBSTRATE CONNECTED TO V_{OUT}
TRANSISTOR COUNT: 729

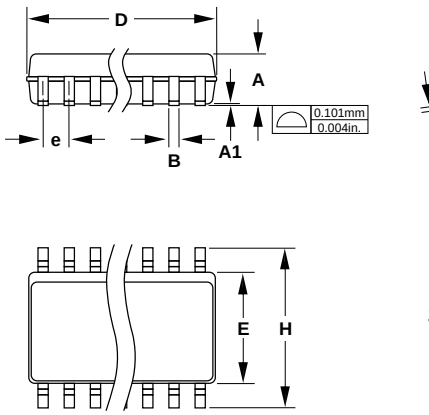
Package Information



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13



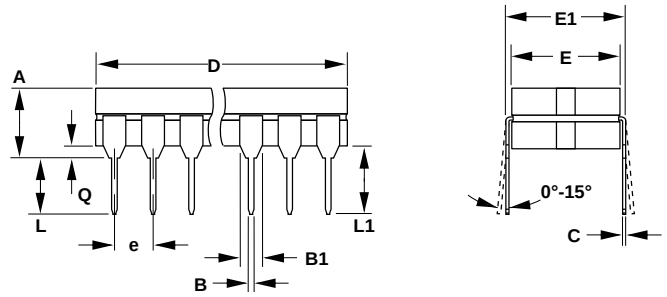
SO
SMALL OUTLINE
PACKAGE
(0.150 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

Package Information (continued)



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51