19-0366; Rev 1; 1/96

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

General Description

The MAX793/MAX794/MAX795 microprocessor (µP) supervisory circuits monitor and control the activities of +3.0V/+3.3V µPs by providing backup-battery switchover, among other features such as low-line indication, µP reset, write protection for CMOS RAM, and a watchdog (see the *Selector Guide* below). The backup-battery voltage can exceed V_{CC}, permitting the use of 3.6V lithium batteries in systems using 3.0V to 3.3V for V_{CC}.

The MAX793/MAX795 offer a choice of reset threshold voltage range (denoted by suffix letter): 3.00V to 3.15V (T), 2.85V to 3.00V (S), and 2.55V to 2.70V (R). The MAX794's reset threshold is set externally with a resistor divider. The MAX793/MAX794 are available in 16-pin DIP and narrow SO packages, and the MAX795 comes in 8-pin DIP and SO packages. For similar devices designed for 5V systems, see the *µP Supervisory Circuits* table at the back of this data sheet.

Selector Guide

FEATURE	MAX793	MAX794	MAX795
Active-Low Reset	✔	✔	✔
Active-High Reset	✔	✔	
Programmable Reset Threshold		✔	
Low-Line Early Warning Output	✔	✔	
Backup-Battery Switchover	✔	✔	✔
External Switch Driver	✔	✔	✔
Power-Fail Comparator	✔	✔	
Battery OK Output	✔		
Watchdog Input	✔	✔	
Battery Freshness Seal	✔	✔	
Manual Reset Input	✔	✔	
Chip-Enable Gating	✔	✔	✔
Pins-Package	16-DIP/SO	16-DIP/SO	8-DIP/SO

Applications

- Battery-Powered Computers and Controllers
- Embedded Controllers
- Intelligent Controllers
- Critical µP Power Monitoring
- Portable Equipment

Pin Configurations appear at end of data sheet.

Features

MAX793/MAX794/MAX795

- **Precision Supply-Voltage Monitor:**
  Fixed Reset Trip Voltage (MAX793/MAX795)
  Adjustable Reset Trip Voltage (MAX794)
- **Guaranteed Reset Assertion to V_{CC} = 1V**
- **Backup-Battery Power Switching—Battery Voltage Can Exceed V_{CC}**
- **On-Board Gating of Chip-Enable Signals—7ns Max Propagation Delay**

MAX793/MAX794 Only

- **Battery Freshness Seal**
- **Battery OK Output (MAX793)**
- **Uncommitted Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Independent Watchdog Timer (1.6sec timeout)**
- **Manual Reset Input**

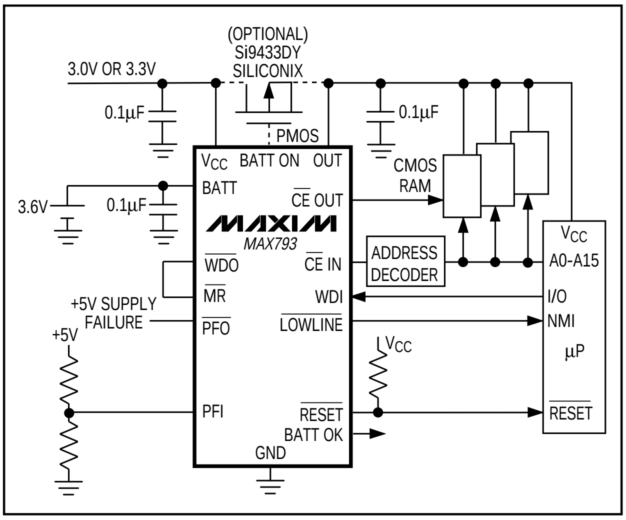
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX793_CPE	0°C to +70°C	16 Plastic DIP
MAX793_CSE	0°C to +70°C	16 Narrow SO
MAX793_EPE	-40°C to +85°C	16 Plastic DIP
MAX793_ESE	-40°C to +85°C	16 Narrow SO

Ordering Information continued on last page.

* The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range (T = 3.00V to 3.15V, S = 2.85V to 3.00V, R = 2.55V to 2.70V) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ....-0.3V to 6.0V
- V_{BATT} ....-0.3V to 6.0V
- All Other Inputs ....-0.3V to the higher of V_{CC} or V_{BATT}

Continuous Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} 200mA
- All Other Outputs 20mA

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C)..................471mW
- 16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .842mW
- 16-Pin Narrow SO (derate 9.52mW/°C above +70°C) ...696mW

Operating Temperature Ranges
- MAX793_C_ _/MAX794C_ _/MAX795_C_ _ .... 0°C to +70°C
- MAX793_E_ _/MAX794E_ _/MAX795_E_ _ ....-40°C to +85°C

Storage Temperature Range ....-65°C to +160°C

Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 1)		MAX79_C		1.0		5.5	V
		MAX79_E		1.1		5.5	
V_{CC} Supply Current (excluding I_{OUT}, $I_{\overline{CE}\,OUT}$)	I_{SUPPLY}	MAX793/MAX794, $\overline{MR}$ = V_{CC}	V_{CC} < 3.6V		46	60	µA
			V_{CC} < 5.5V		62	80	
		MAX795	V_{CC} < 3.6V		35	50	
			V_{CC} < 5.5V		49	70	
V_{CC} Supply Current in Battery-Backup Mode (excluding I_{OUT})	I_{SUPPLY}	V_{CC} = 2.1V, V_{BATT} = 2.3V	MAX793/MAX794		32	45	µA
			MAX795		24	35	
BATT Supply Current (excluding I_{OUT}) (Note 2)						1	µA
BATT Leakage Current, Freshness Seal Enabled		V_{CC} = 0V, V_{OUT} = 0V				1	µA
Battery Leakage Current (Note 3)						0.5	µA
OUT Output Voltage in Normal Mode	V_{OUT}	I_{OUT} = 75mA		V_{CC} - 0.3	V_{CC} - 0.125		V
		I_{OUT} = 30mA (Note 4)		V_{CC} - 0.12	V_{CC} - 0.050		
		I_{OUT} = 250µA (Note 4)		V_{CC} - 0.001	V_{CC} - 0.5mV		
OUT Output Voltage in Battery-Backup Mode	V_{OUT}	V_{BATT} = 2.3V	I_{OUT} = 250µA	V_{BATT} - 0.1	V_{BATT} - 0.034		V
			I_{OUT} = 1mA		V_{BATT} - 0.14		
Battery Switch Threshold (V_{CC} falling)	V_{CC} - V_{BATT}	V_{SW} > V_{CC} > 1.75V (Note 5)			20	65	mV
	V_{SW}	V_{BATT} > V_{CC} (Note 6)	MAX793T/MAX795T	2.69	2.82	2.95	V
			MAX793S/MAX795S	2.55	2.68	2.80	
			MAX793R/MAX795R/ MAX794	2.30	2.41	2.52	
Battery Switch Threshold (V_{CC} rising) (Note 7)	V_{CC} - V_{BATT}	This value is identical to the reset threshold, V_{CC} rising for V_{BATT} > V_{RST}					
		V_{BATT} < V_{RST}			25	65	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Threshold (Note 8)	V_{RST}	V_{CC} Falling	MAX793T/MAX795T	3.00	3.075	3.15	V
			MAX793S/MAX795S	2.85	2.925	3.00	
			MAX793R/MAX795R	2.55	2.625	2.70	
		V_{CC} Rising	MAX793T/MAX795T	3.00	3.085	3.17	
			MAX793S/MAX795S	2.85	2.935	3.02	
			MAX793R/MAX795R	2.55	2.635	2.72	
RESET IN Threshold (MAX794 only)	$V_{RST\ IN}$	V_{CC} Falling		1.212	1.240	1.262	V
		V_{CC} Rising		1.212	1.250	1.282	
RESET IN Leakage Current (MAX794 only)				-25	2	25	nA
Reset Timeout Period	t_{RP}	V_{CC} < 3.6V		140	200	280	ms
$\overline{\text{LOWLINE}}$-to-Reset Threshold, ($V_{\overline{LOWLINE}}$ - V_{RST}), V_{CC} Falling	V_{LR}	MAX793		30	45	60	mV
		MAX794		5	15	25	
Low-Line Comparator Hysteresis		MAX793			10		mV
		MAX794			10		mV
$\overline{\text{LOWLINE}}$ Threshold, V_{CC} Rising	V_{LL}	MAX793T/MAX795T				3.23	V
		MAX793S/MAX795S				3.08	
		MAX793R/MAX795R				2.78	
		MAX794				1.317	
PFI Input Threshold	V_{TH}	V_{PFI} falling		1.212	1.240	1.262	V
		V_{PFI} rising		1.212	1.250	1.287	
PFI Input Current				-25	2	25	nA
PFI Hysteresis, PFI Rising					10	20	mV
BATT OK Threshold (MAX793)	V_{BOK}			2.00	2.25	2.50	V
INPUT AND OUTPUT LEVELS							
RESET Output Voltage High	V_{OH}	I_{SOURCE} =300µA, V_{CC} = V_{RST} min		$0.8V_{CC}$	$0.86V_{CC}$		V
BATT OK, BATT ON, $\overline{\text{WDO}}$, $\overline{\text{LOWLINE}}$ Output Voltage High	V_{OH}	I_{SOURCE} = 300µA, V_{CC} = V_{RST} max		$0.8V_{CC}$	$0.86V_{CC}$		V
$\overline{\text{PFO}}$ Output Voltage High	V_{OH}	I_{SOURCE} = 65µA, V_{CC} = V_{RST} max		$0.8V_{CC}$			V
BATT ON Output Voltage High	V_{OH}	I_{SOURCE} = 100µA, V_{CC} = 2.3V, V_{BATT} = 3V		$0.8V_{BATT}$			V
$\overline{\text{RESET}}$ Output Leakage Current (Note 9)	I_{LEAK}	V_{CC} = V_{RST} max		-1		-1	µA
$\overline{\text{PFO}}$ Output Short to GND Current	I_{SC}	V_{CC} = 3.3V, $V_{\overline{PFO}}$ = 0V			180	500	µA
$\overline{\text{PFO}}$, $\overline{\text{RESET}}$, RESET, $\overline{\text{WDO}}$, $\overline{\text{LOWLINE}}$ Output Voltage Low	V_{OL}	I_{SINK} = 1.2mA; $\overline{\text{RESET}}$, $\overline{\text{LOWLINE}}$ tested with V_{CC} = V_{RST} min; RESET, BATTOK, $\overline{\text{WDO}}$ tested with V_{CC} = V_{RST} max			0.08	$0.2V_{CC}$	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{RESET}}$ Output Voltage Low	V_{OL}	MAX79_C, V_{BATT} = V_{CC} = 1.0V, I_{SINK} = 40µA		0.13	0.3	V
		MAX79_E, V_{BATT} = V_{CC} = 1.2V, I_{SINK} = 200µA		0.17	0.3	
BATT ON Output Voltage Low	V_{OL}	I_{SINK} = 3.2mA, V_{CC} = V_{RST} max			$0.2V_{CC}$	V
All Inputs Including $\overline{\text{PFO}}$ (Note 10)	V_{IH}	V_{RST} max < V_{CC} < 5.5V			$0.7V_{CC}$	V
	V_{IL}		$0.3V_{CC}$			
MANUAL RESET INPUT						
$\overline{\text{MR}}$ Pulse Width	t_{MR}	MAX793/MAX794 only	100	50		ns
$\overline{\text{MR}}$-to-Reset Delay	t_{MD}	MAX793/MAX794 only		75	250	ns
$\overline{\text{MR}}$ Pull-Up Current		MAX793/MAX794 only, $\overline{\text{MR}}$ = 0V	25	70	250	µA
CHIP-ENABLE GATING						
$\overline{\text{CE}}$ IN Leakage Current	I_{LEAK}	Disable mode		±10		nA
$\overline{\text{CE}}$ IN-to-$\overline{\text{CE}}$ OUT Resistance		Enable mode, V_{CC} = V_{RST} max		46		Ω
$\overline{\text{CE}}$ IN-to-$\overline{\text{CE}}$ OUT Propagation Delay		V_{CC} = V_{RST} max, Figure 9		2	7	ns
$\overline{\text{CE}}$ OUT Drive from $\overline{\text{CE}}$ IN	V_{OH}	V_{CC} = V_{RST} max, I_{OUT} = -1mA, $V_{\overline{CE}\,IN}$ = V_{CC}	$0.8V_{CC}$			V
	V_{OL}	V_{CC} = V_{RST} max, I_{OUT} = 1.6mA, $V_{\overline{CE}\,IN}$ = 0V			$0.2V_{CC}$	
Reset to $\overline{\text{CE}}$ OUT High Delay				10		µs
$\overline{\text{CE}}$ OUT Output Voltage High (reset active)	V_{OH}	I_{OH} = 500µA, V_{CC} < 2.3V	$0.8V_{BATT}$			V
WATCHDOG (MAX793/MAX794 only)						
WDI Input Current		0V < V_{CC} < 5.5V	-1	0.01	1	µA
Watchdog Timeout Period	t_{WD}		1.00	1.60	2.25	sec
WDI Pulse Width			1.00			ns

Note 1: V_{CC} supply current, logic input leakage, watchdog functionality (MAX793/MAX794), $\overline{\text{MR}}$ functionality (MAX793/MAX794), PFI functionality (MAX793/MAX794), state of $\overline{\text{RESET}}$ and RESET (MAX793/MAX794) tested at V_{BATT} = 3.6V and V_{CC} = 5.5V. The state of $\overline{\text{RESET}}$ is tested at V_{CC} = V_{CC} min.

Note 2: Tested at V_{BATT} = 3.6V, V_{CC} = 3.5V and 0V. The battery current will rise to 10µA over a narrow transition window around V_{CC} = 1.9V.

Note 3: Leakage current into the battery is tested under the worst-case conditions at V_{CC} = 5.5V, V_{BATT} = 1.8V and V_{CC} = 1.5V, V_{BATT} = 1.0V.

Note 4: Guaranteed by design.

Note 5: When V_{SW} > V_{CC} > V_{BATT}, OUT remains connected to V_{CC} until V_{CC} drops below V_{BATT}. The V_{CC}-to-V_{BATT} comparator has a small 15mV typical hysteresis to prevent oscillation. For V_{CC} < 1.75V (typical), OUT switches to BATT regardless of V_{BATT}.

Note 6: When V_{BATT} > V_{CC} > V_{SW}, OUT remains connected to V_{CC} until V_{CC} drops below the battery switch threshold (V_{SW}).

Note 7: OUT switches from BATT to V_{CC} when V_{CC} rises above the reset threshold, if V_{BATT} > V_{RST}. In this case, switchover back to V_{CC} occurs at the exact voltage that causes reset to be asserted, however switchover occurs 200ms prior to reset. If V_{BATT} < V_{RST}, OUT switches from BATT to V_{CC} when V_{CC} exceeds V_{BATT}.

Note 8: The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

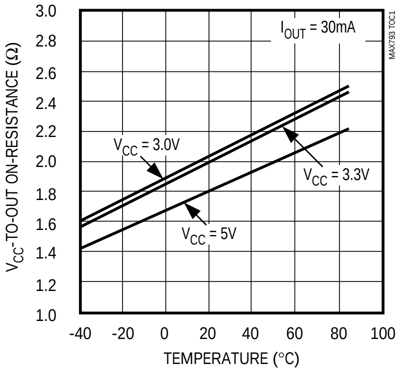
Note 9: The leakage current into or out of the $\overline{\text{RESET}}$ pin is tested with $\overline{\text{RESET}}$ not asserted ($\overline{\text{RESET}}$ output high impedance).

Note 10: $\overline{\text{PFO}}$ is normally an output, but is used as an input when activating the battery freshness seal.

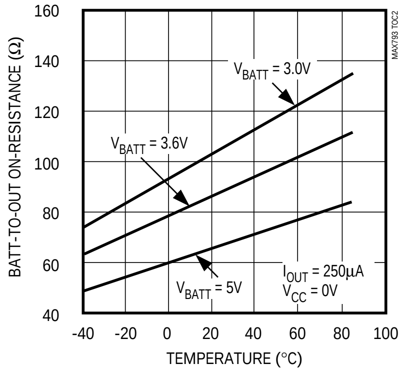
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

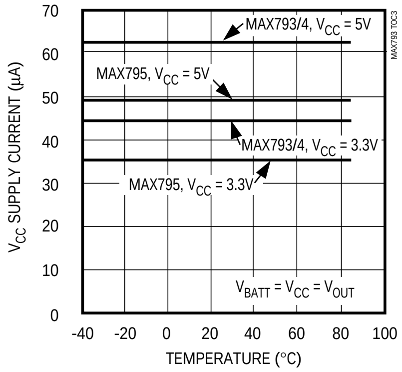
V_{CC}-TO-OUT ON-RESISTANCE vs. TEMPERATURE



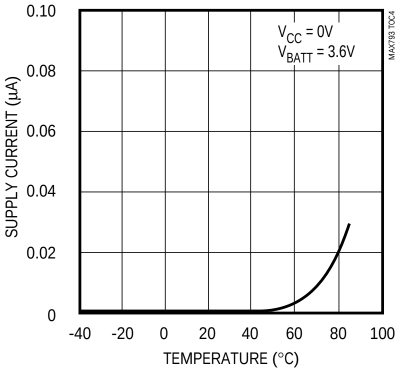
BATT-TO-OUT ON-RESISTANCE vs. TEMPERATURE



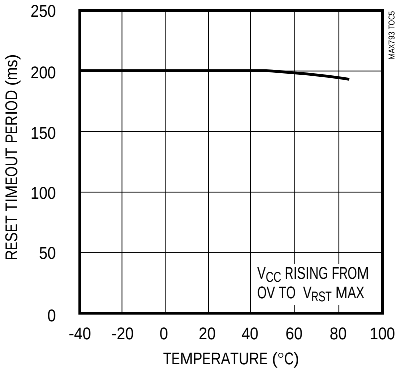
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



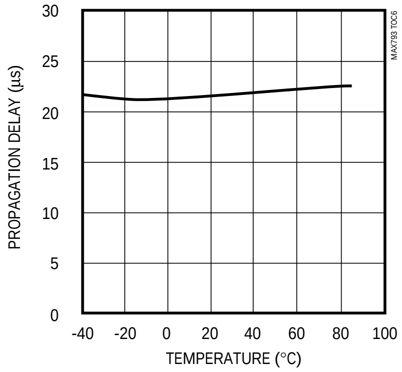
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



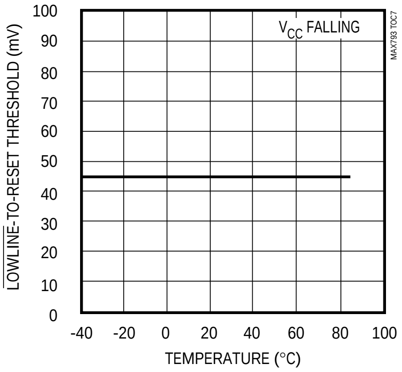
RESET TIMEOUT PERIOD vs. TEMPERATURE



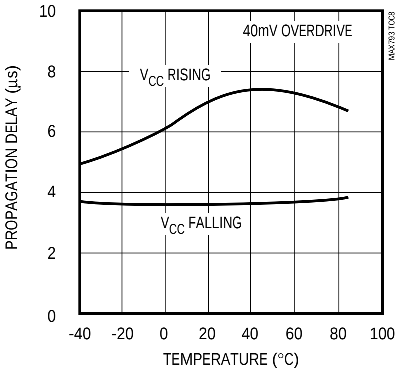
RESET COMPARATOR PROPAGATION DELAY vs. TEMPERATURE (V_{CC} FALLING)



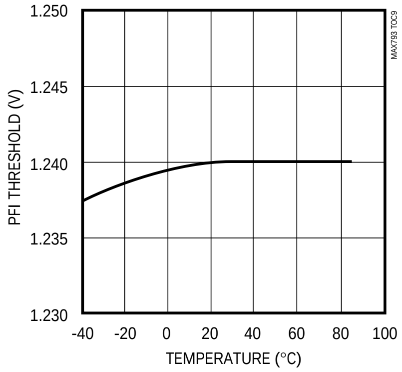
MAX793 $\overline{\text{LOWLINE}}$-TO-RESET THRESHOLD vs. TEMPERATURE



MAX793/MAX794 $\overline{\text{LOWLINE}}$ COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



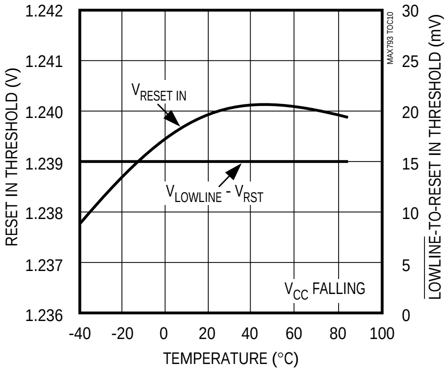
MAX793/MAX794 PFI THRESHOLD vs. TEMPERATURE



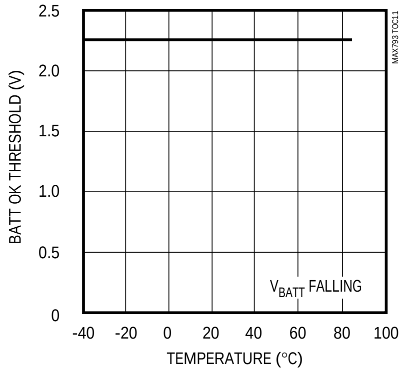
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

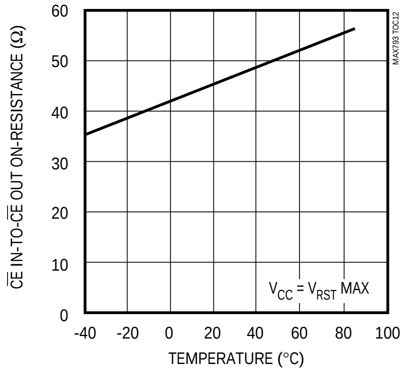
MAX794
RESET IN THRESHOLD AND $\overline{\text{LOWLINE}}$-TO-RESET IN THRESHOLD vs. TEMPERATURE



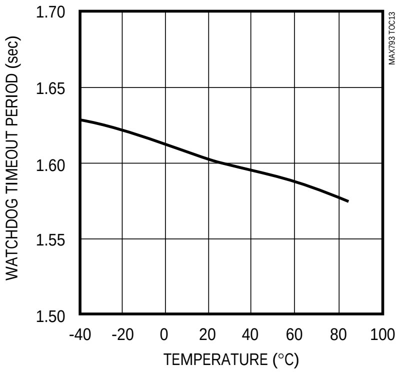
MAX793
BATT OK THRESHOLD vs. TEMPERATURE



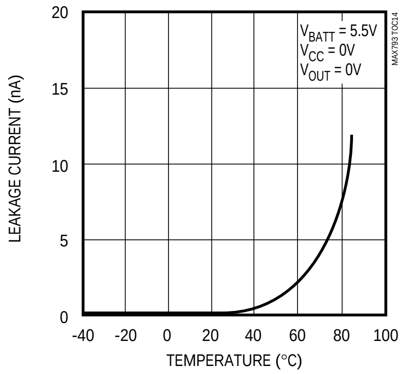
$\overline{\text{CE}}$ IN-TO-$\overline{\text{CE}}$ OUT ON-RESISTANCE vs. TEMPERATURE



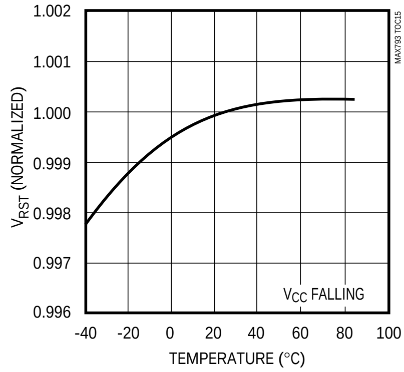
MAX793/MAX794
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



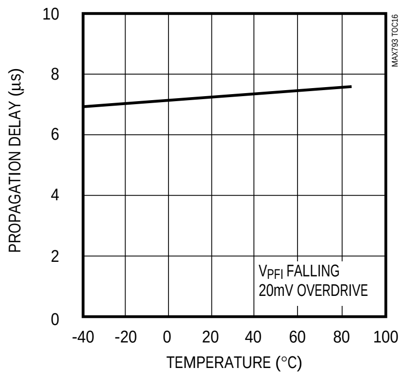
MAX793/MAX794
BATTERY FRESHNESS SEAL LEAKAGE CURRENT vs. TEMPERATURE



RESET THRESHOLD vs. TEMPERATURE (NORMALIZED)



MAX793/MAX794
PFI TO $\overline{\text{PFO}}$ PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX793/ MAX794	MAX795		
1	1	OUT	Supply Output for CMOS RAM. When V_{CC} rises above the reset threshold or above V_{BATT}, OUT is connected to V_{CC} through an internal P-channel MOSFET switch. When V_{CC} falls below V_{SW} and V_{BATT}, BATT connects to OUT.
2	2	V_{CC}	Main Supply Input
3	—	BATT OK (MAX793)	Battery Status Output. High in normal operating mode when V_{BATT} exceeds V_{BOK}, otherwise low. V_{BATT} is checked continuously. Disabled and logic low while V_{CC} is below V_{SW}.
		RESET IN (MAX794)	Reset Input. Connect to an external resistor divider to select the reset threshold. The reset threshold can be programmed anywhere in the V_{SW} to 5.5V range.
4	—	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} or when V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high (see *Power-Fail Comparator* section). Connect to V_{CC} if unused.
5	3	BATT ON	Logic Output/External Bypass Switch-Driver Output. High when OUT switches to BATT. Low when OUT switches to V_{CC}. Connect the base/gate of PNP/PMOS transistor to BATT ON for I_{OUT} requirements exceeding 75mA.
6	4	GND	Ground
7	—	$\overline{PFO}$	Power-Fail Comparator Output. When PFI is less than V_{PFT} or when V_{CC} falls below V_{SW}, PFO goes low; otherwise, $\overline{PFO}$ remains high. $\overline{PFO}$ is also used to enable the battery freshness seal (see B*attery Freshness Seal*, and *Power-Fail Comparator* sections).
8	—	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low and for 200ms after $\overline{MR}$ returns high. The active-low input has an internal 70µA pull-up current. In can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open if unused.
9	—	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transition of WDI. $\overline{WDO}$ is a logic high for $V_{SW} < V_{CC} < V_{RST}$, and low when V_{CC} is below V_{SW}.
10	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and $\overline{WDO}$ goes low. $\overline{WDO}$ returns high on the next transition of WDI. Connect $\overline{WDO}$ to $\overline{MR}$ to generate a reset due to a watchdog fault.
11	5	$\overline{CE}$ IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to GND if unused
12	6	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will remain low for 10µs or until $\overline{CE}$ IN goes high, whichever occurs first. $\overline{CE}$ OUT is pulled up to OUT.
13	—	RESET	Active-High Reset Output. Sources and sinks current. RESET is the inverse of $\overline{RESET}$.
14	—	$\overline{LOWLINE}$	Early Power-Fail Warning Output. Low when V_{CC} falls to V_{LR}. This output can be used to generate an NMI to provide early warning of imminent power-failure.
15	7	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after either V_{CC} rises above the reset threshold, the watchdog triggers a reset (WDO connected to $\overline{MR}$), or $\overline{MR}$ goes low to high.
16	8	BATT	Backup-Battery Input. When V_{CC} falls below V_{SW} and V_{BATT}, OUT switches from V_{CC} to BATT. When V_{CC} rises above the reset threshold or above V_{BATT}, OUT reconnects to V_{CC}. V_{BATT} may exceed V_{CC}. Connect V_{CC}, OUT, and BATT together if no battery is used.

Detailed Description

General Timing Characteristics

The MAX793/MAX794/MAX795 are designed for 3.3V and 3V systems, and provide a number of supervisory functions (see the *Selector Guide* on the front page). Figures 1 and 2 show the typical timing relationships of the various outputs during power-up and power-down with typical V_{CC} rise and fall times.

Manual Reset Input (MAX793/MAX794)

Many microprocessor-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX793/MAX794, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (200ms) after it returns high. During the first half of the reset timeout period (t_{RP}), the state of $\overline{MR}$ is ignored if $\overline{PFO}$ is externally forced low, to facilitate enabling the battery freshness seal. $\overline{MR}$ has an internal 70µA pull-up current, so it can be left open if it is not used. This input can be driven with TTL- or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to ground to provide additional noise immunity.

Reset Outputs

A microprocessor's (µP's) reset input starts the µP in a known state. These MAX793/MAX794/MAX795 µP supervisory circuits assert a reset to prevent code execution errors during power-up, power-down, and

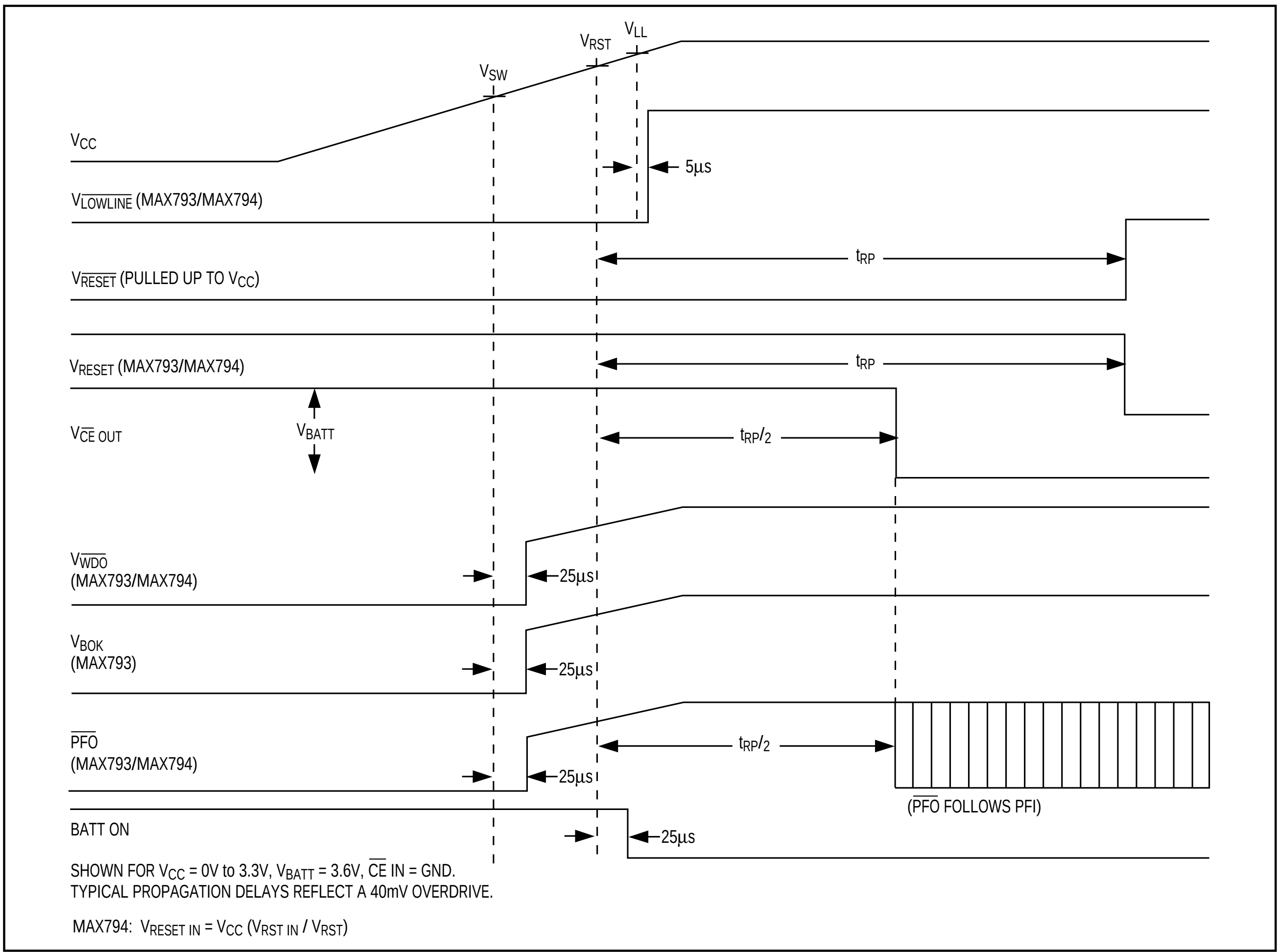


Figure 1. Timing Diagram, V_{CC} Rising

brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for 0V < V_{CC} < V_{RST}, provided V_{BATT} is greater than 1V. Without a backup battery (V_{BATT} = V_{CC} = V_{OUT}), $\overline{RESET}$ is guaranteed valid for $V_{CC} \geq$ 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period (t_{RP}); after this interval, $\overline{RESET}$ becomes high impedance (Figure 2). $\overline{RESET}$ is an open-drain output, and requires a pull-up resistor to V_{CC} (Figure 3). Use a 4.7kΩ to 1MΩ pull-up resistor that will provide sufficient current to assure the proper logic levels to the µP.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts.

The watchdog output ($\overline{WDO}$) can also be used to initiate a reset. See the *Watchdog Output* section.

The RESET output is the inverse of the $\overline{RESET}$ output, and it can both source and sink current.

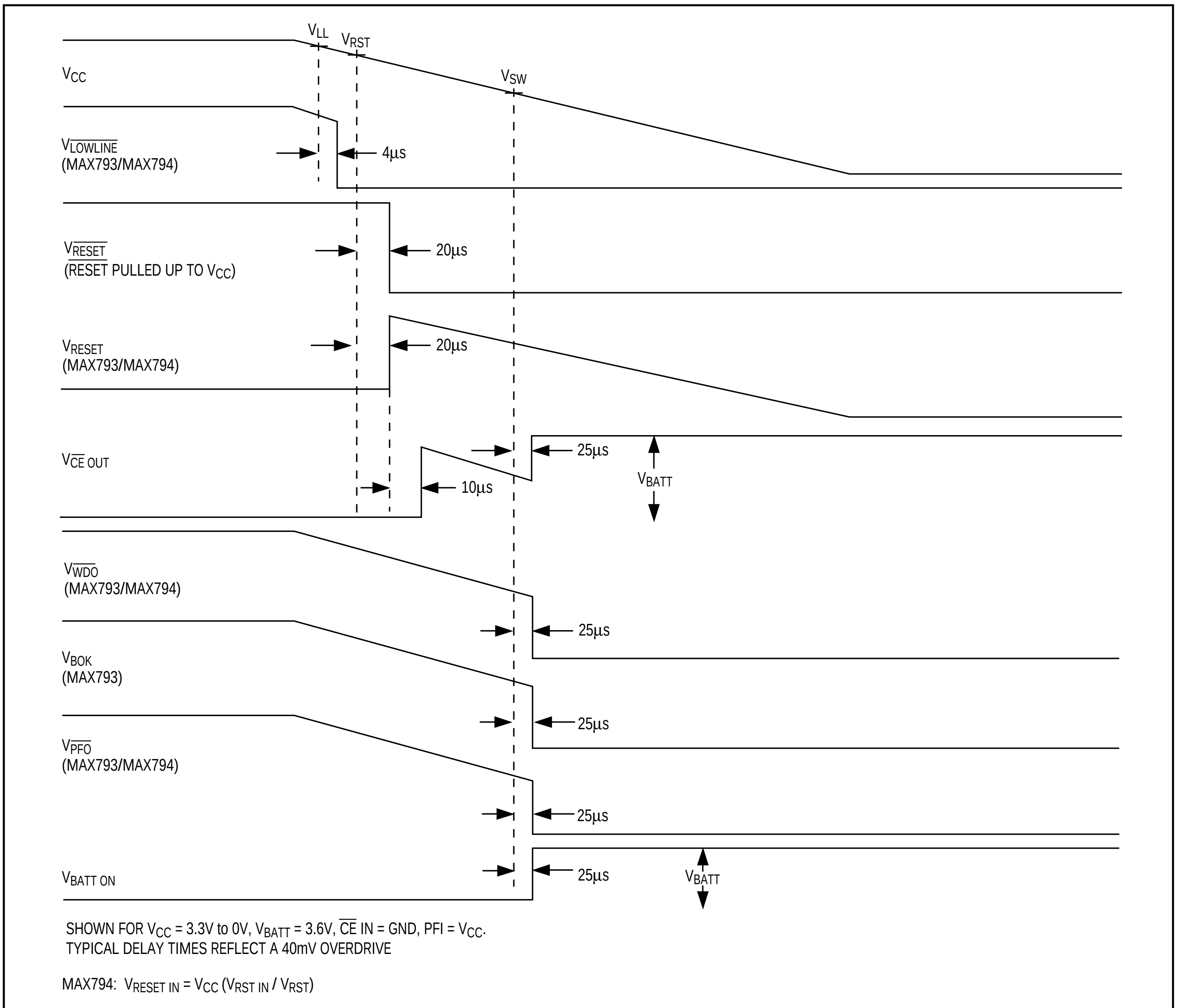


Figure 2. Timing Diagram, V_{CC} Falling

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

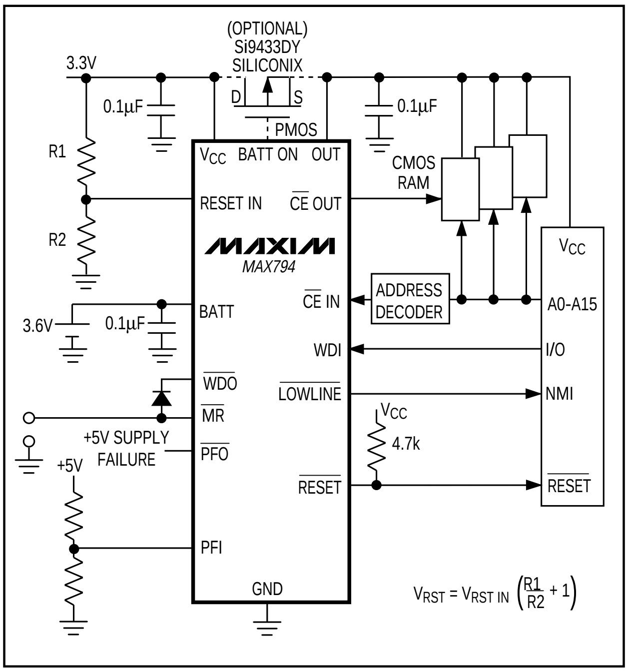


Figure 3. MAX794 Standard Application Circuit

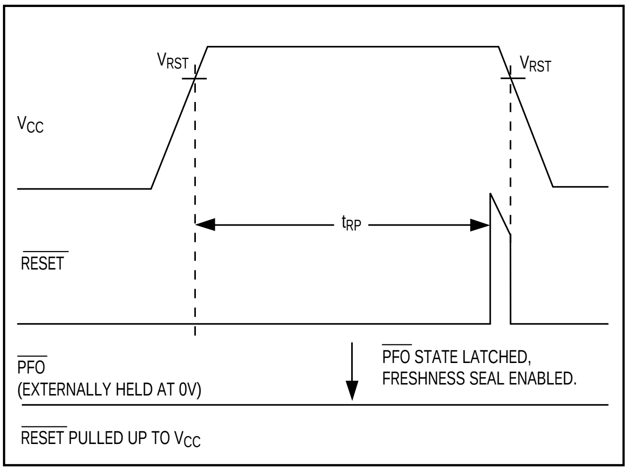


Figure 4. Battery Freshness Seal Enable Timing

Reset Threshold

The MAX793T/MAX795T are intended for 3.3V systems with a ±5% power-supply tolerance and a 10% systems tolerance. Except when $\overline{MR}$ is asserted, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V (3.3V - 10%).

The MAX793S/MAX795S are designed for 3.3V ±10% power supplies. Except when $\overline{MR}$ is asserted, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.0V is just above 3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (3.3V - 14%).

The MAX793R/MAX795R are optimized to monitor 3.0V ±10% power supplies. Reset will not occur until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.55V (3.0V - 15%).

Program the MAX794's reset threshold with an external voltage divider to RESET IN. The reset-threshold tolerance will be a combination of the RESET IN tolerance and the tolerance of the resistors used to make the external voltage divider. Calculate the reset threshold as follows:

$$V_{RST} = V_{RST\ IN}\ (R1 / R2 + 1)$$

Using the standard application circuit (Figure 3), the reset threshold may be programmed anywhere in the range of V_{SW} (the battery switch threshold) to 5.5V. Reset is asserted when V_{CC} falls below V_{SW}.

Battery Freshness Seal

The MAX793/MAX794's battery freshness seal disconnects the backup battery from internal circuitry until it is needed. This allows an OEM to ensure that the backup battery connected to BATT will be fresh when the final product is put to use. To enable the freshness seal, connect a battery to BATT, ground $\overline{PFO}$, bring V_{CC} above the reset threshold and hold it there until reset is deasserted following the reset timeout period, then bring V_{CC} back down again (Figure 4). Once the battery freshness seal is enabled (disconnecting the backup battery from the internal circuitry and anything connected to OUT), it remains enabled until V_{CC} is brought above V_{RST}. Note that connecting $\overline{PFO}$ to $\overline{MR}$ will not interfere with battery freshness seal operation.

BATT OK Output (MAX793)

BATT OK indicates the status of the backup battery. When reset is not asserted, the MAX793 checks the battery voltage continuously. If V_{BATT} is below V_{BOK} (2.0V min), BATT OK goes low; otherwise, it remains pulled up to V_{CC}. BATT OK also goes low when V_{CC} goes below V_{SW}.

Watchdog Input (MAX793/MAX794)

In the MAX793/MAX794, the watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, $\overline{WDO}$ goes low. The internal 1.6sec timer is cleared and $\overline{WDO}$ returns high

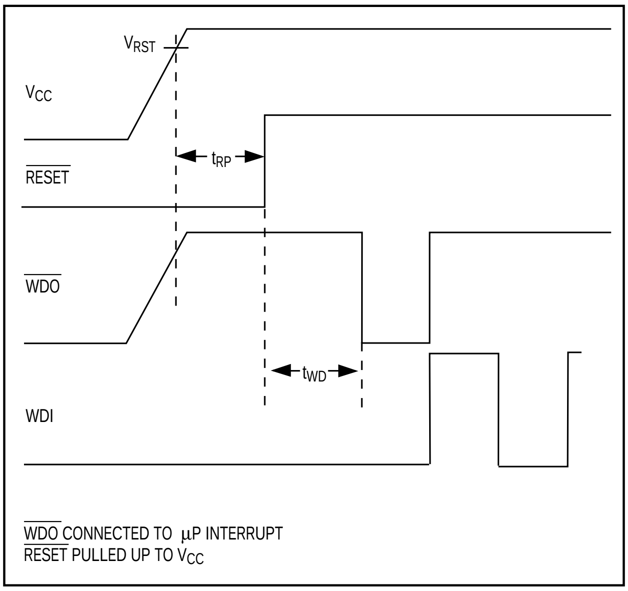


Figure 5. Watchdog Timing Relationship

either when a reset occurs or when a transition (low-to-high or high-to-low) takes place at WDI. As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is released or WDI changes state, the timer starts counting (Figure 5). WDI can detect pulses as short as 100ns. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

Watchdog Output (MAX793/MAX794)

In the MAX793/MAX794, $\overline{WDO}$ remains high ($\overline{WDO}$ is pulled up to V_{CC}) if there is a transition or pulse at WDI during the watchdog timeout period. $\overline{WDO}$ goes low if no transition occurs at WDI during the watchdog timeout period. The watchdog function is disabled and $\overline{WDO}$ is a logic high when reset is asserted if V_{CC} is above V_{SW}. $\overline{WDO}$ is a logic low when V_{CC} is below V_{SW}.

If a system reset is desired on every watchdog fault, simply diode-OR connect $\overline{WDO}$ to $\overline{MR}$ (Figure 6). When a watchdog fault occurs in this mode, $\overline{WDO}$ goes low, pulling $\overline{MR}$ low, which causes a reset pulse to be issued. Ten microseconds after reset is asserted, the watchdog timer clears and $\overline{WDO}$ returns high. This delay results in a 10µs pulse at $\overline{WDO}$, allowing external circuitry to “capture” a watchdog fault indication. A continuous high or low on WDI will cause 200ms reset pulses to be issued every 1.6sec.

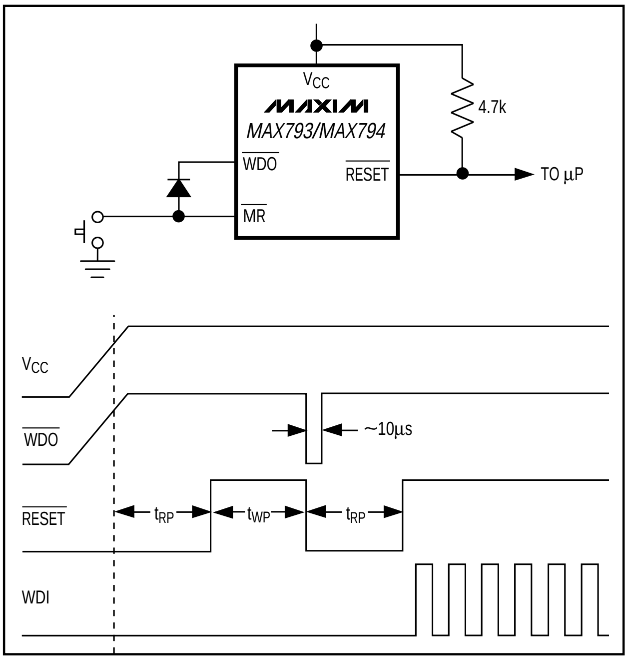


Figure 6. Generating a Reset on Each Watchdog Fault

Chip-Enable Signal Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX793/MAX794/MAX795 use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 7). During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables these µP supervisors to be used with most µPs. If $\overline{CE}$ IN is low when reset asserts, $\overline{CE}$ OUT remains low for typically 10µs to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE}$ IN immediately becomes high impedance if the voltage at $\overline{CE}$ IN is high. If $\overline{CE}$ IN is low when reset asserts, the CE transmission gate will disable at the moment $\overline{CE}$ IN goes high, or 10µs after reset asserts, whichever occurs first (Figure 8). This permits the current write cycle to complete during power-down.

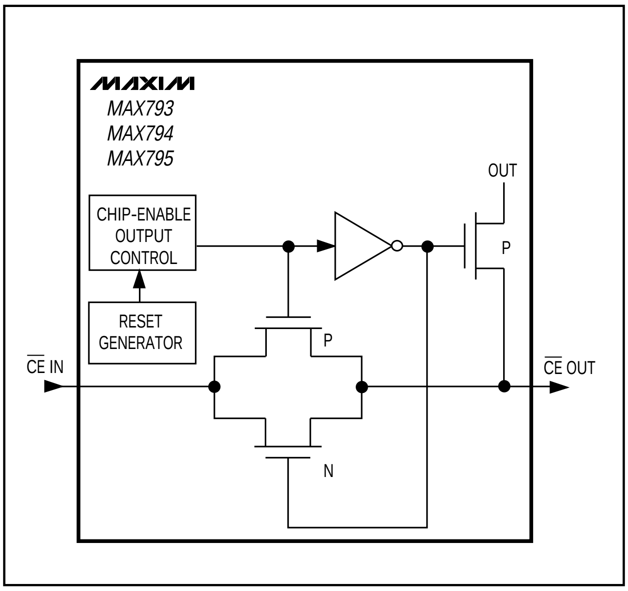


Figure 7. Chip-Enable Transmission Gate

The CE transmission gate remains disabled and $\overline{CE}$ IN remains high impedance (regardless of $\overline{CE}$ IN activity) for the first half of the reset timeout period (t_{RP} / 2), any time a reset is generated. While disabled, $\overline{CE}$ IN is high impedance. When the CE transmission gate is enabled, the impedance of $\overline{CE}$ IN appears as a 46Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{CE}$ IN, and the loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 9). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low-output-impedance driver.

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of $\overline{CE}$ OUT is equivalent to a 46Ω resistor in series with the source driving $\overline{CE}$ IN. In the disabled mode, the transmission gate is off and an active pull-up connects $\overline{CE}$ OUT to OUT (Figure 8). This pull-up turns off when the transmission gate is enabled.

Early Power-Fail Warning (MAX793/MAX794)

Critical systems often require an early warning indicating that power is failing. This warning provides time for the µP to store vital data and take care of any additional "housekeeping" functions, before the power supply gets too far out of tolerance for the µP to operate reliably. The MAX793/MAX794 offer two methods of achieving this early warning. If access to the unregulated supply is feasible, the power-fail comparator input (PFI) can be connected to the unregulated supply

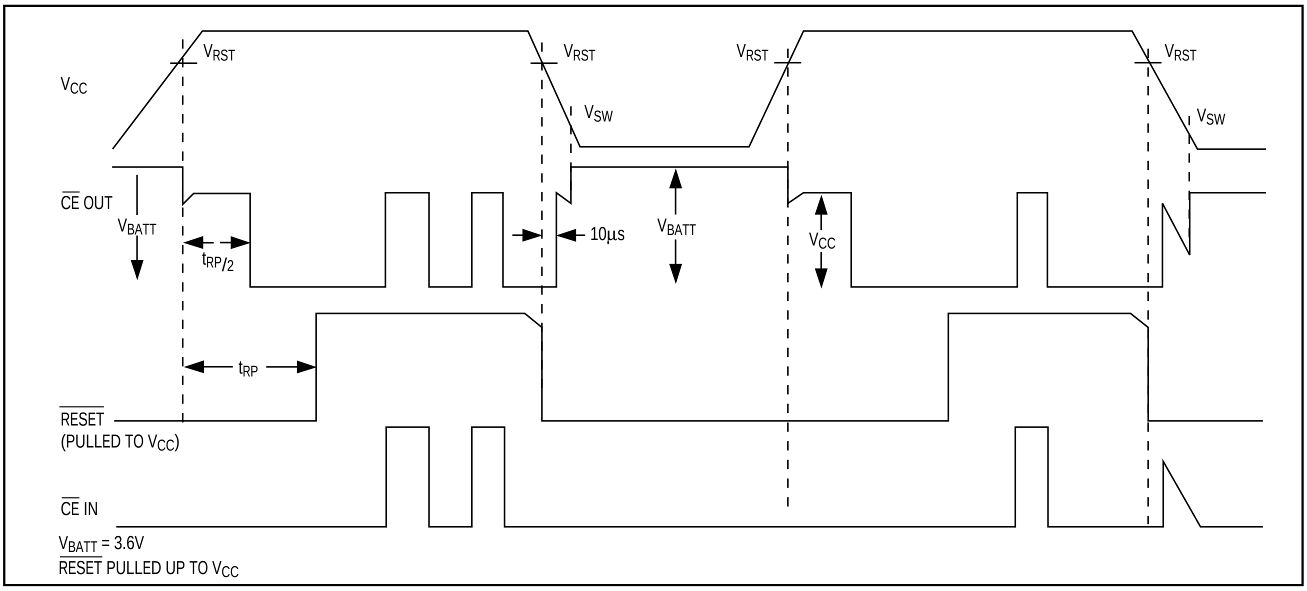


Figure 8. Chip-Enable Timing

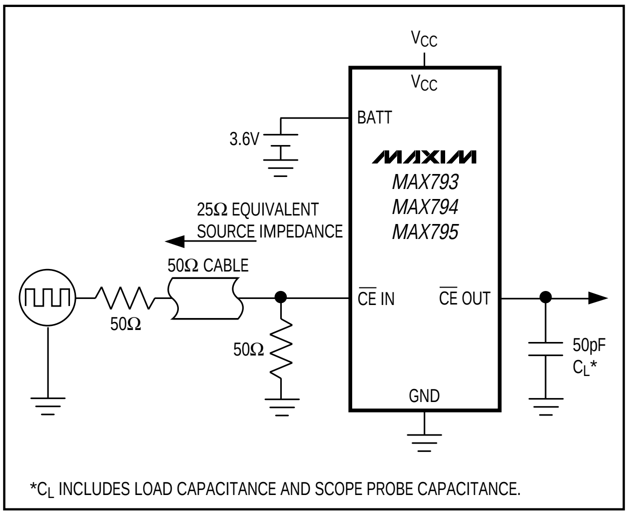


Figure 9. CE Propagation Delay Test Circuit

through a voltage divider, with the power-fail comparator output ($\overline{PFO}$) providing the NMI to the µP (Figure 10). If there is no easy access to the unregulated supply, the $\overline{LOWLINE}$ output can be used to generate an NMI to the µP (see *$\overline{LOWLINE}$ Output* section).

$\overline{LOWLINE}$ Output (MAX793/MAX794)

The low-line comparator monitors V_{CC} with a threshold voltage typically 45mV above the reset threshold (10mV of hysteresis) for the MAX793, and 15mV above RESET IN (4mV of hysteresis) for the MAX794. For normal operation (V_{CC} above the reset threshold), $\overline{LOWLINE}$ is pulled to V_{CC}. Use $\overline{LOWLINE}$ to provide an NMI to the µP when power begins to fall.

In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must also contend with a more rapid V_{CC} fall time, such as when the main battery is disconnected or a high-side switch is opened during normal operation, use capacitance on the V_{CC} line to provide time to execute the shutdown routine (Figure 11).

First, calculate the worst-case time required for the system to perform its shutdown routine. Then, with the worst-case shutdown time, the worst-case load current, and the minimum low-line to reset threshold (V_{LR} min), calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} > I_{LOAD} \times t_{SHDN} / V_{LR}$$

where I_{LOAD} is the current being drained from the capacitor, V_{LR} is the low-line to reset threshold difference (V_{LL} - V_{RST}), and t_{SHDN} is the time required for the system to complete an orderly shutdown routine.

Power-Fail Comparator (MAX793/MAX794)

The MAX793/MAX794's PFI input is compared to an internal reference. If PFI is less than the power-fail threshold (V_{PFT}), $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 12). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

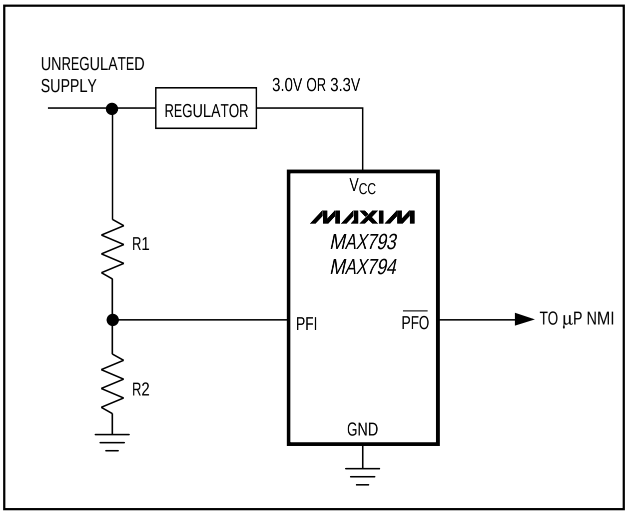


Figure 10. Using the Power-Fail Comparator to Generate Power-Fail Warning

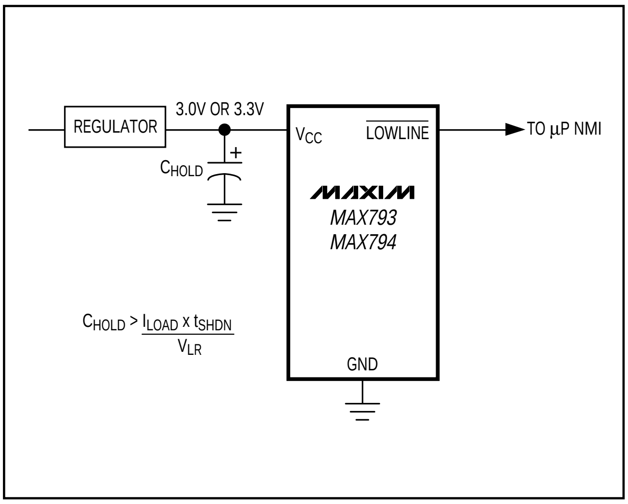


Figure 11. Using $\overline{LOWLINE}$ to Provide Power-Fail Warning to the µP

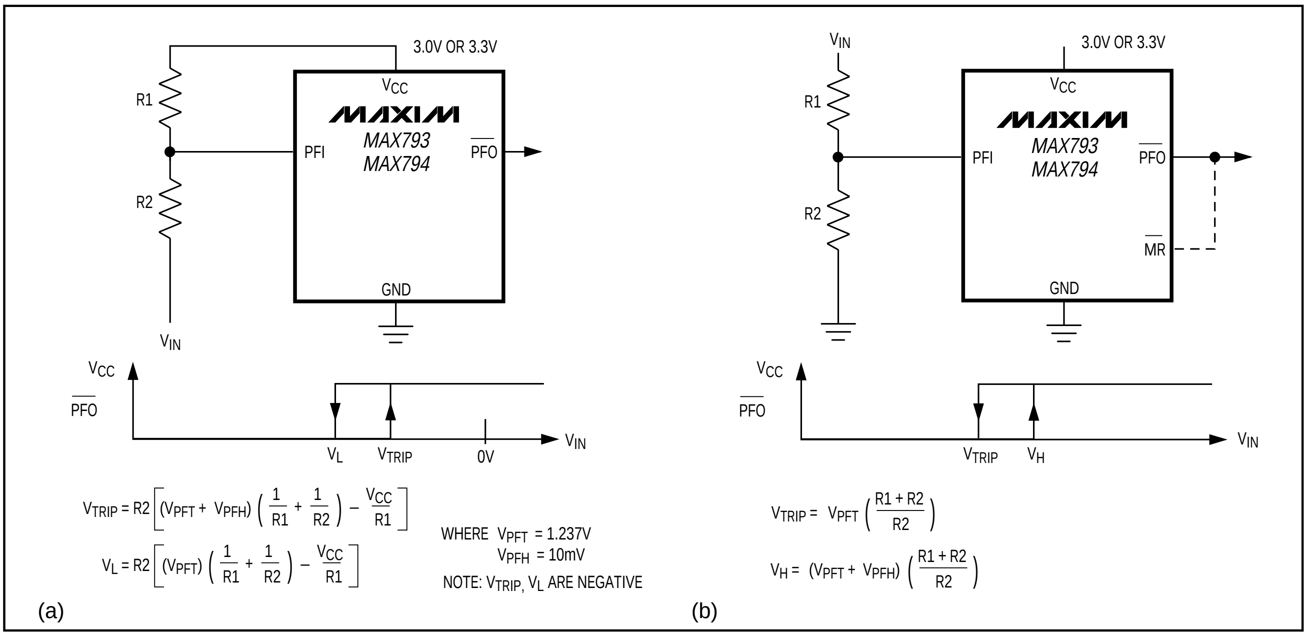


Figure 12. Using the Power-Fail Comparator to Monitor an Additional Power Supply: (a) V_{IN} Is Negative, (b) V_{IN} Is Positive

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{SW} on power-down. During the first half of the reset timeout period (t_{RP}), $\overline{PFO}$ is forced high, irrespective of V_{PFI}. At the beginning of the second half of t_{RP}, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, connect PFI to V_{CC} and leave PFO unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ so that a low voltage on PFI will generate a reset (Figure 12b). In this configuration, when the monitored voltage causes PFI to fall below V_{PFT}, $\overline{PFO}$ pulls $\overline{MR}$ low, causing a reset to be asserted. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for 200ms after $\overline{PFO}$ pulls $\overline{MR}$ high when the monitored supply is above the programmed threshold.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the devices automatically switch RAM to backup power when V_{CC} falls. In order to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC}, this family of µP supervisors (designed for 3.3V and 3V systems) does not always connect BATT to OUT when V_{BATT} is greater than V_{CC}. BATT connects to OUT (through a 140Ω switch) either when V_{CC} falls below V_{SW} **and** V_{BATT} is greater than V_{CC}, **or** when V_{CC} falls below 1.75V (typ) regardless of the BATT voltage.

Switchover at V_{SW} ensures that battery-backup mode is entered before V_{OUT} gets too close to the 2.0V minimum required to reliably retain data in most CMOS RAM, (switchover at higher V_{CC} voltages would decrease backup-battery life). When V_{CC} recovers, switchover is deferred either until V_{CC} crosses V_{BATT} if V_{BATT} is below V_{RST}, or when V_{CC} rises above the reset threshold (V_{RST}) if V_{BATT} is above V_{RST}. This power-up switchover technique prevents V_{CC} from charging the backup battery through OUT when using an external transistor driven by BATT ON. OUT connects to V_{CC} through a 4Ω (max) PMOS power switch when V_{CC} crosses the reset threshold (Figure 13).

BATT ON (MAX793/MAX794)

BATT ON is high when OUT is connected to BATT. Although BATT ON can be used as a logic output to indicate the battery switchover status, it is most often used as a gate or base drive for an external pass transistor for high-current applications (see *Driving an External Switch with BATT ON* in the *Applications Information* section). When V_{CC} exceeds V_{RST} on power-up, BATT ON sinks 3.2mA at 0.4V. In battery-backup mode, this terminal sources 100µA from BATT.

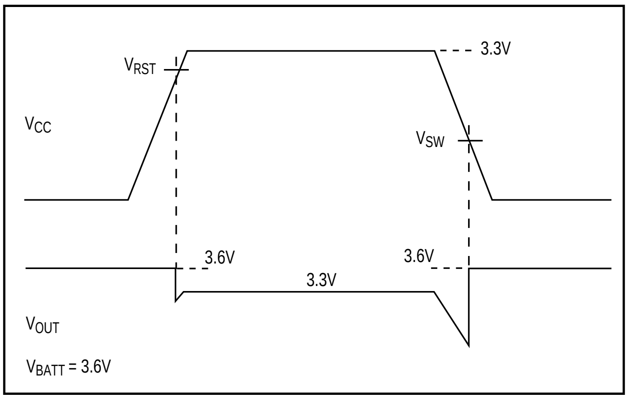


Figure 13. Battery Switchover Timing

Table 1. Input and Output Status in Battery-Backup Mode

PIN NAME	STATUS
OUT	Connected to BATT through an internal 140Ω switch
V_{CC}	Disconnected from OUT
BATT ON	Pulled up to BATT
BATT OK	Logic low
PFI	Disabled
$\overline{\text{PFO}}$	Logic low
$\overline{\text{MR}}$	Disabled, but still pulled up to V_{CC}
$\overline{\text{WDO}}$	Logic low
WDI	Disabled
$\overline{\text{RESET}}$	Logic low
RESET	Pulled up to V_{CC}
BATT	Connected to OUT
$\overline{\text{LOWLINE}}$	Logic low
$\overline{\text{CE}}$ IN	High impedance
$\overline{\text{CE}}$ OUT	Pulled to BATT

Applications Information

These µP supervisory circuits are not short-circuit protected. Shorting V_{OUT} to ground, excluding power-up transients such as charging a decoupling capacitor, destroys the device. Decouple both V_{CC} and BATT pins to ground by placing 0.1µF ceramic capacitors as close to the device as possible.

Driving an External Switch with BATT ON

BATT ON can be directly connected to the base of a PNP transistor or the gate of a PMOS transistor. The PNP connection is straightforward: connect the emitter to V_{CC}, the collector to OUT, and the base to BATT ON (Figure 14a). No current-limiting resistor is required, but a resistor connecting the base of the PNP to BATT ON can be used to limit the current drawn from V_{CC}, prolonging battery life in portable equipment.

If you are using a PMOS transistor, however, it must be connected backwards from the traditional method. Connect the gate to BATT ON, the drain to V_{CC}, and the source to OUT (Figure 14b). This method orients the body diode from V_{CC} to OUT and prevents the backup battery from discharging through the FET when its gate is high. Two PMOS transistors in the Siliconix LITTLE FOOT™ series are specified with V_{GS} down to -2.7V. The Si9433DY has a maximum 100mΩ drain-source on-resistance with 2.7V of gate drive and a 2A drain-source current. The Si9434DY specifies a 60mΩ drain-source on-resistance with 2.7V of gate drive and a 5.1A drain-source current.

Using a SuperCap™ as a Backup Power Source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 15 shows two ways to use a SuperCap as a backup power source. The SuperCap can be connected through a diode to the 3V input (Figure 15a); or, if a 5V supply is also available, the SuperCap can be charged up to the 5V supply (Figure 15b), allowing a longer backup period. Since V_{BATT} can exceed V_{CC} while V_{CC} is above the reset threshold, there are no special precautions when using these µP supervisors with a SuperCap.

Operation without a Backup Power Source

These µP supervisors were designed for battery-backed applications. If a backup battery is not used, connect BATT, OUT, and V_{CC} together, or use a different µP supervisor. See the *µP Supervisory Circuits* table at the end of this data sheet.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, without danger of triggering a reset pulse, provided that BATT is decoupled with a 0.1µF capacitor to ground. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

™ LITTLE FOOT is a trademark of Siliconix Inc.
SuperCap is a trademark of Baknor Industries.

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

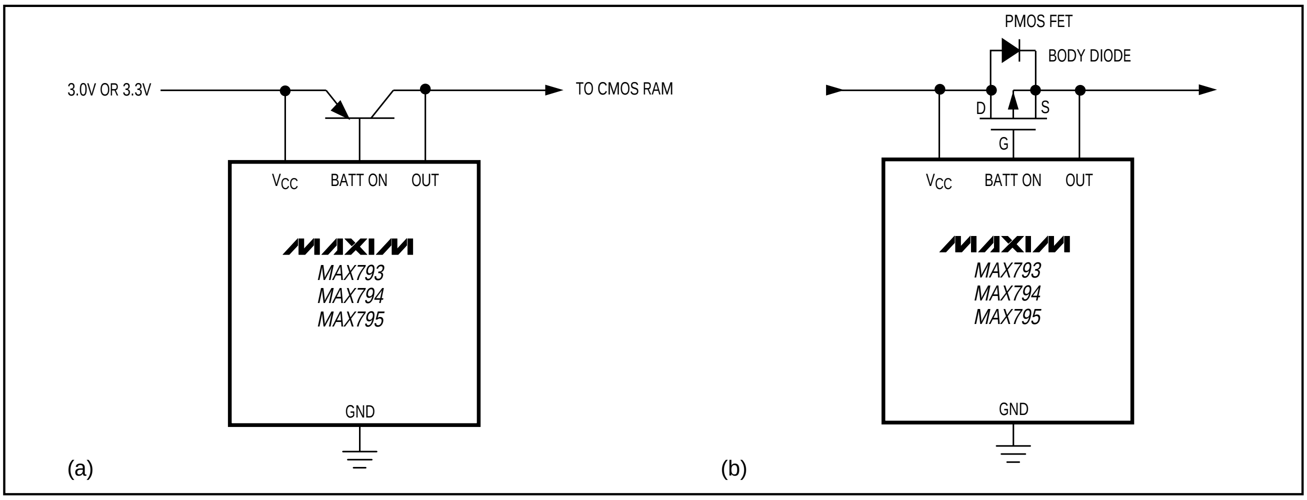


Figure 14. Driving an External Transistor with BATT ON

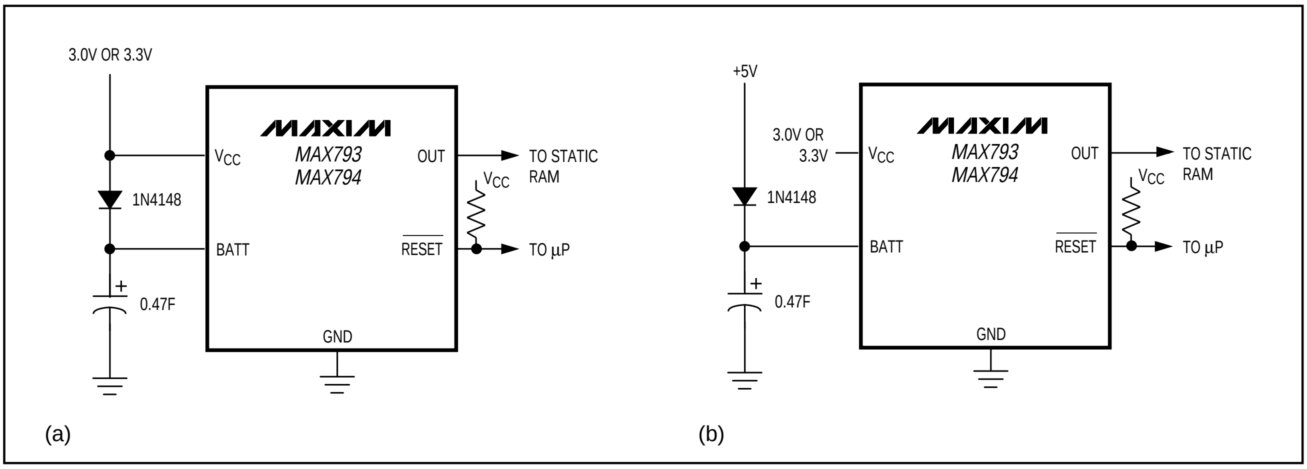


Figure 15. Using a SuperCap™ as a Backup Source

Erratum

Initial versions of the MAX793 and MAX794 have a logic design error that can cause the loss of output voltage (OUT) when V_{CC} is absent even though a backup battery is connected to the BATT input. Applications that do not use the $\overline{\text{MR}}$ input (including all MAX795 applications) are unaffected by this phenomenon. Also, applications that do not use $\overline{\text{PFO}}$ are unaffected if PFI is tied to V_{CC}.

The loss of output voltage is caused by the IC incorrectly entering the battery "freshness seal" mode. Normally, freshness seal mode is activated by grounding $\overline{\text{PFO}}$ during a power-up reset timeout period. Then, the removal of V_{CC} powers the IC down without connecting the backup battery to OUT.

The IC decides whether or not to enter freshness seal mode during all reset timeout periods. During a power-up reset timeout period (which occurs when V_{CC} is raised above the MAX793's reset threshold or the voltage on the MAX794's RESET IN pin is raised above the RESET IN threshold), the IC momentarily disconnects the $\overline{\text{PFO}}$ pin from the comparator output and lightly pulls $\overline{\text{PFO}}$ up to V_{CC}. The voltage level on the $\overline{\text{PFO}}$ pin is then tested and, if it is low, freshness seal mode is chosen. ($\overline{\text{PFO}}$ is reconnected to the comparator output before the end of the reset timeout period.)

However, when a reset is initiated by $\overline{\text{MR}}$, the $\overline{\text{PFO}}$ pin incorrectly remains connected to the comparator output during the entire timeout period and is not pulled up. If the comparator is driving $\overline{\text{PFO}}$ low during an $\overline{\text{MR}}$ reset

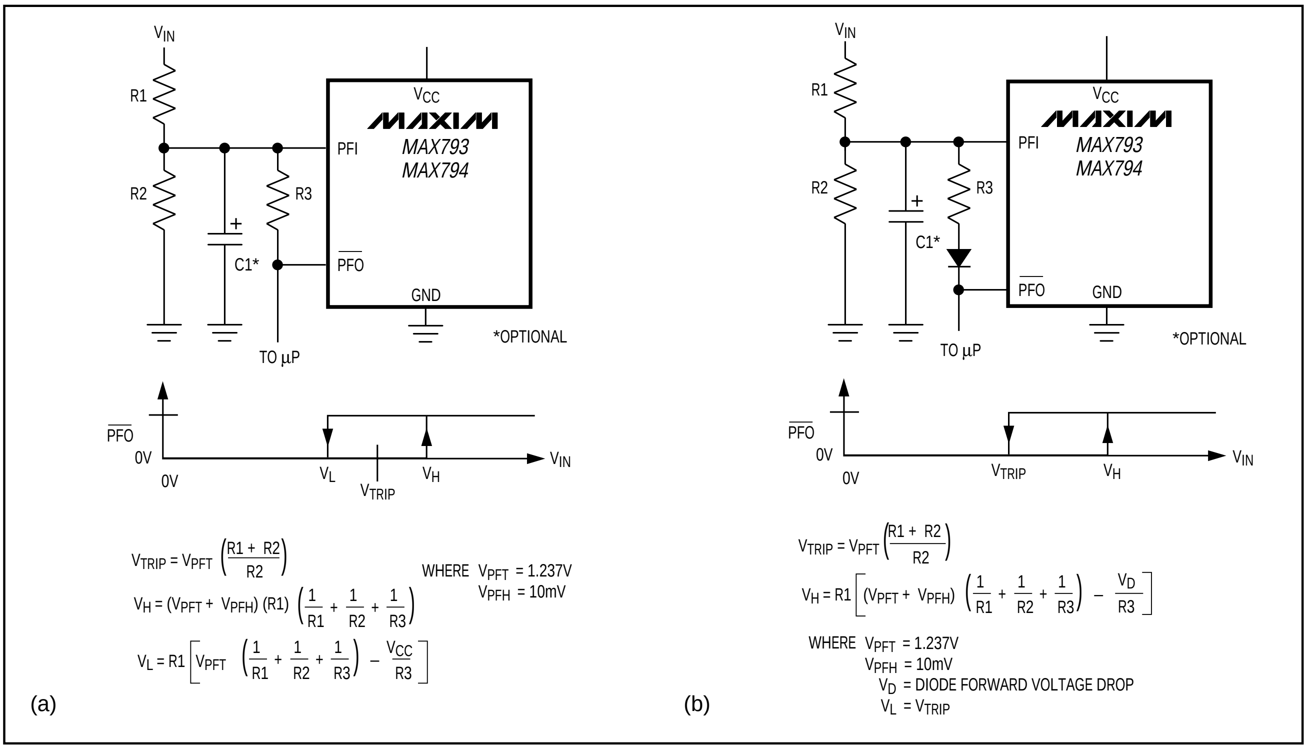


Figure 16. Adding Hysteresis to the Power-Fail Comparator: (a) Symmetrical Hysteresis, (b) Hysteresis Only on Rising V_{IN}

timeout period (because PFI is below the PFI threshold), the IC will test the voltage level on $\overline{PFO}$, find that it is low, and incorrectly decide to enter freshness seal mode. If V_{CC} is later removed, the backup battery will not be connected to OUT and any devices powered by OUT will lose power.

Applications that do not use the $\overline{PFO}$ comparator need not be affected by this problem. Simply connect PFI to V_{CC} and $\overline{PFO}$ will be driven high during all reset timeout periods. Freshness seal mode can be entered only when $\overline{PFO}$ is low.

The IC is under revision to correct this problem. The revised IC will disable $\overline{PFO}$ during all reset timeout periods including $\overline{MR}$-initiated ones. This revision will not affect applications that either do not use $\overline{MR}$ or do not use $\overline{PFO}$, but could affect applications that require the use of the $\overline{PFO}$ output during $\overline{MR}$-initiated reset timeout periods. The revised ICs are expected to be available in late 1996. For technical assistance, please contact Maxim Applications at 1-800-998-8800 or at http:// www. maxim-ic.com.

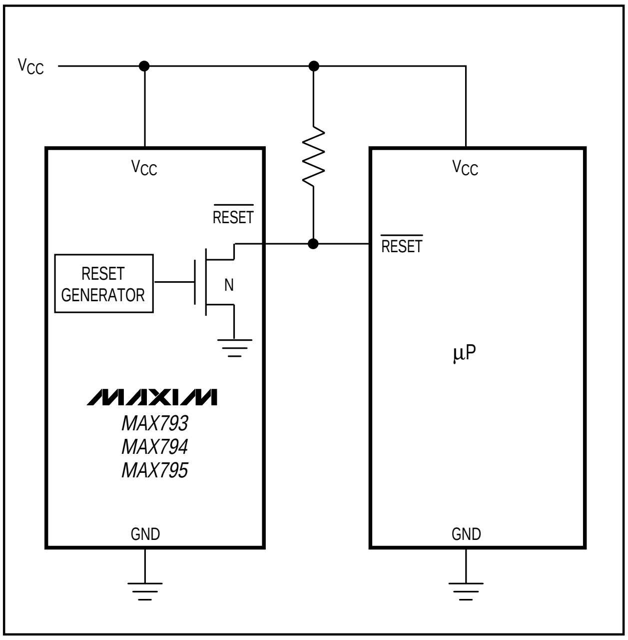


Figure 17. Interfacing to µPs with Bidirectional Reset I/O

Adding Hysteresis to the Power-Fail Comparator (MAX793/MAX794)

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the section *Monitoring an Additional Power Supply*).

If additional noise margin is desired, connect a resistor between PFO and PFI as shown in Figure 16a. Select the ratio of R1 and R2 such that PFI sees V_{PFT} when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the additional hysteresis and should typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

Connecting an ordinary signal diode in series with R3, as shown in Figure 16b, causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}), so the entire hysteresis window occurs above V_{TRIP}. This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max over temperature) PFI input current does not shift the trip point. R3 should be larger than 82kΩ so it does not load down the PFO pin. Capacitor C1 is optional, and adds noise rejection.

Monitoring an Additional Power Supply

These µP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. PFO can be used to generate an interrupt to the µP or to cause reset to assert (Figure 12).

Interfacing to µPs with Bidirectional Reset Pins

Since the RESET output is open drain, the MAX793/MAX794/MAX795 interface easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the RESET output of the µP supervisor directly to the RESET input of the microcontroller with a single pull-up resistor allows either device to assert reset (Figure 17).

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches) while issuing resets to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not recommended.

Figure 18 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient can typically

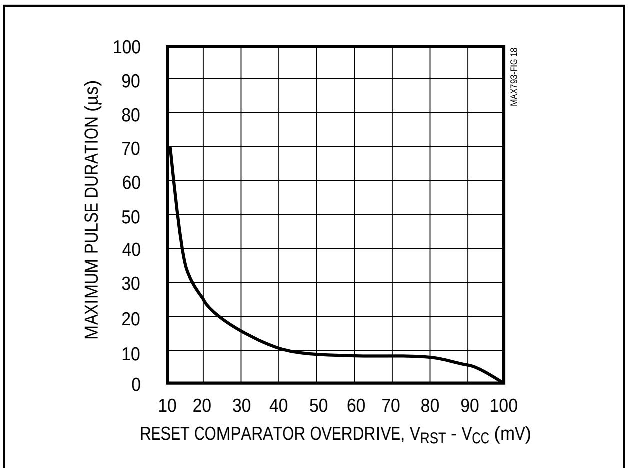


Figure 18. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

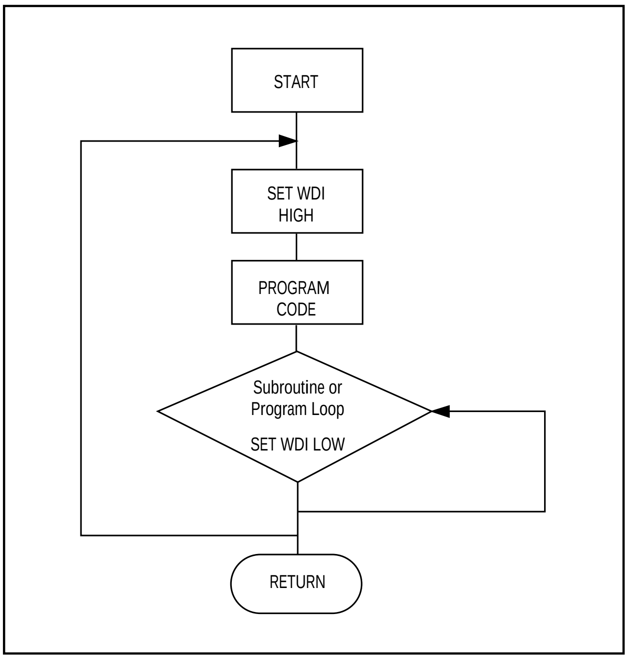


Figure 19. Watchdog Flow Diagram

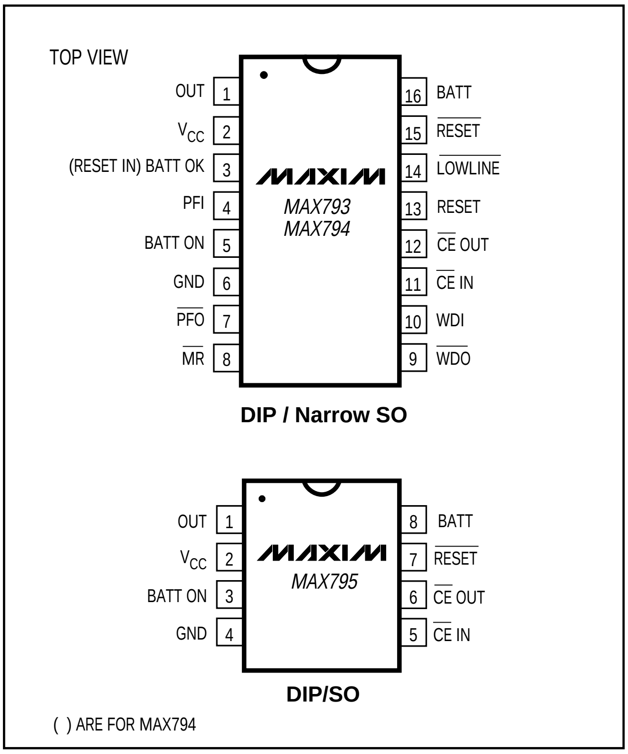
have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 40mV below the reset threshold and lasts for 10µs or less will not cause a reset pulse to be issued.

A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Watchdog Software Considerations

There is a way to help the watchdog timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 19 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Pin Configurations



Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX794CPE	0°C to +70°C	16 Plastic DIP
MAX794CSE	0°C to +70°C	16 Narrow SO
MAX794EPE	-40°C to +85°C	16 Plastic DIP
MAX794ESE	-40°C to +85°C	16 Narrow SO
MAX795_CPA	0°C to +70°C	8 Plastic DIP
MAX795_CSA	0°C to +70°C	8 SO
MAX795_EPA	-40°C to +85°C	8 Plastic DIP
MAX795_ESA	-40°C to +85°C	8 SO

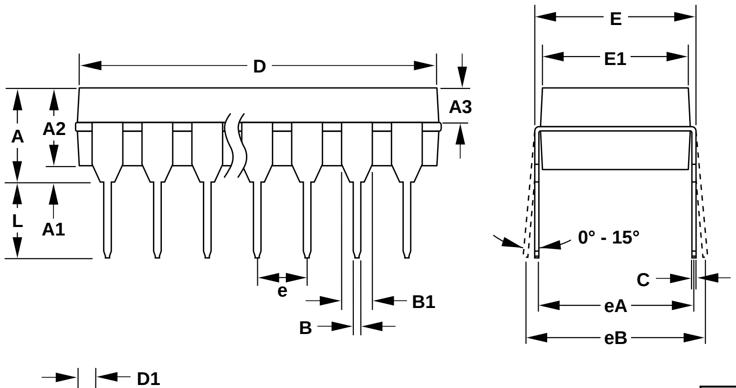
* The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range (T = 3.00V to 3.15V, S = 2.85V to 3.00V, R = 2.55V to 2.70V) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

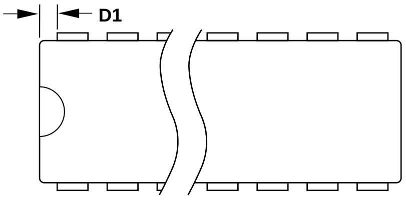
Chip Information

TRANSISTOR COUNT: 1271

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Package Information



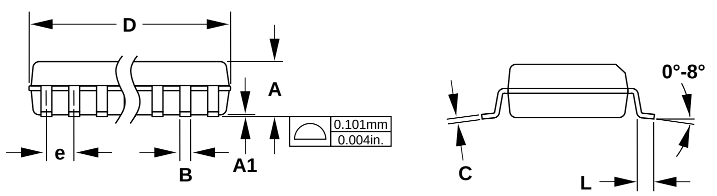


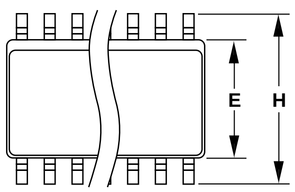
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A