19-0315; Rev 0; 10/94

MAXIM

950MHz FET-Input Buffer with 75Ω Output

General Description

The MAX4005 is a ±5V, single-ended unity-gain buffer with a high-impedance JFET input, intended to drive a 75Ω load. A 75Ω thin-film output resistor is included on-board to minimize reflections when driving a 75Ω load through a transmission line of arbitrary length. Gain in this configuration is 0.5.

Features

- **950MHz Bandwidth**
- **350ps Rise/Fall Times**
- **0.11%/0.03° Differential Gain/Phase Error**
- **1000V/µs Slew Rate**
- **10pA Input Bias Current**
- **75Ω Output Impedance**

Applications

Video Buffer / Line Driver

Isolation Between High-Impedance Node and Low-Impedance Instrument

Remote Signal Sensing

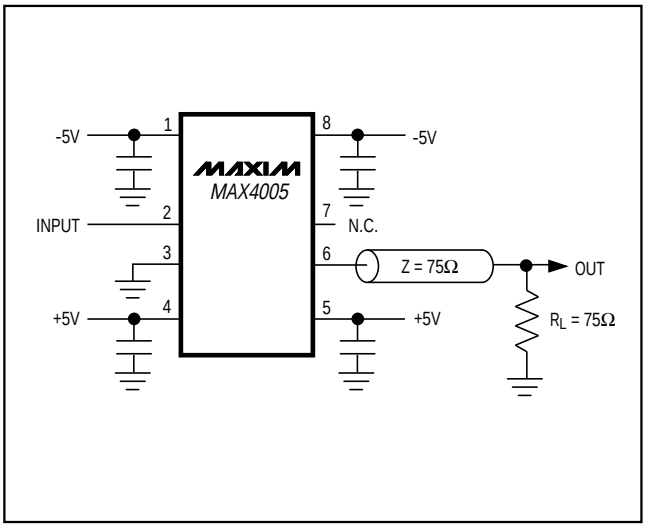
Impedance Transformation

Fanout Multiplier for 75Ω Distribution Systems

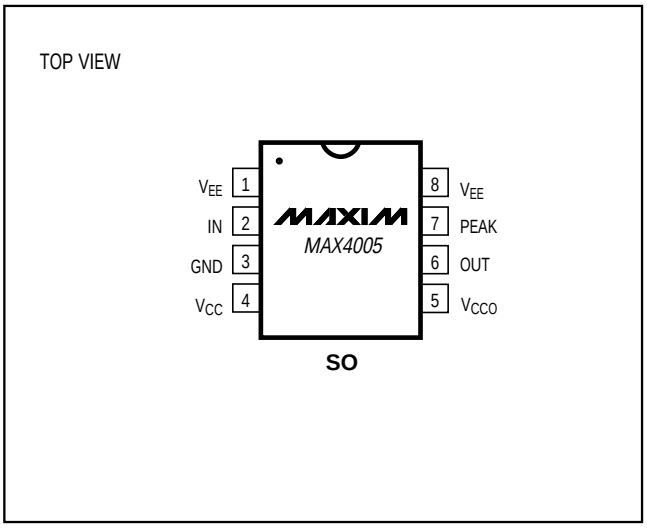
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4005CSA	0°C to +70°C	8 SO

Typical Operating Circuit



Pin Configuration



950MHz FET-Input Buffer with 75Ω Output

ABSOLUTE MAXIMUM RATINGS

Input Voltage.....±2.5V
V_{CC} Supply Voltage.....+5.5V
Output-Stage Supply .....+5.5V
V_{EE} Supply Voltage.....-5.5V
Peaking Pad Voltage.....0.0V
Ground Voltage.....0.0V
Continuous Power Dissipation (T_A = +70°C).....471mW
Operating Temperature Range.....0°C to +70°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

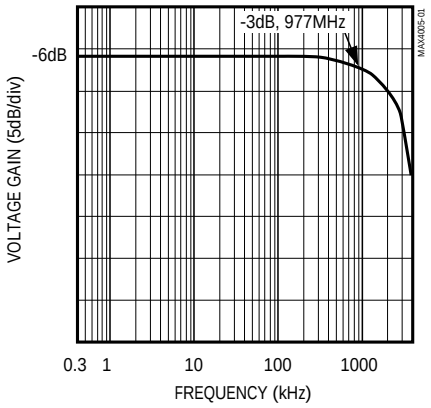
(V_{CC} = 4.75V to 5.25V, V_{EE} = -4.75V to -5.25V, T_A = +25°C, stated performance characterized for T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+5V V_{CC} Current	I_{VCC1}	V_{IN} = 0V, R_L = 75Ω	9	14	19	mA
+5V Output Stage Quiescent Current	I_{VCC2}	V_{IN} = 0V, R_L = 75Ω	9	11	14	mA
-5V V_{EE} Current	I_{VEE}	V_{IN} = 0V, R_L = 75Ω	17	24	31	mA
Output Offset Voltage		R_L = 75Ω, gain = 0.5	-3		3	mV
Output Resistance	R_{OUT}		74.0	75.0	76.5	Ω
Input Current	I_B	V_{IN} = 0V	-1	0.01	1	nA
Gain		R_L = 75Ω	0.49	0.50	0.51	
Linearity		R_L = 75Ω, measured over input dynamic range		0.50	1	%
Input Dynamic Range		R_L = 75Ω, gain = 0.5	-1.3		1.6	V
+5V V_{CC} Power-Supply Rejection Ratio		V_{IN} = 0V, R_L = 75Ω	40	55		dB
+5V Output Stage Power-Supply Rejection Ratio		V_{IN} = 0V, R_L = 75Ω	50	75		dB
-5V V_{EE} Power-Supply Rejection Ratio		V_{IN} = 0V, R_L = 75Ω	40	60		dB
TYPICAL OPERATING PERFORMANCE (V_{CC} = 5.0V, V_{EE} = -5.0V, R_L = 75Ω, T_A = +25°C, unless otherwise noted.)						
Bandwidth	BW	-3dB		950		MHz
		-6dB		2000		
Input Capacitance	C_{IN}			2.2		pF
Settling Time to 0.1%	t_{SET}	V_{IN} = 0.25V step, V_{OUT} = 0.125V step		2		ns
Rise/Fall Times	t_{RISE}/t_{FALL}	V_{IN} = 0.25V step with < 30ps rise time		350		ps
Gain Flatness	GF	At 30MHz		±0.01		dB
Gain Flatness ±0.1dB	GF1			60		MHz
Gain Flatness ±0.2dB	GF2			80		MHz
Slew Rate	SR	V_{IN} = 2.5V step with 200ps rise time		1000		V/µs
Overdrive Recovery Time	t_{OD}	V_{IN} = 2.5V step		5		ns
2nd Harmonic Distortion	2HD	At 50MHz		-50		dBc
3rd Harmonic Distortion	3HD	At 50MHz		< -60		dBc
3rd-Order Intercept	TOI	At 100MHz		28		dBm
Differential Gain Error	DG	At 3.58MHz		0.11		%
Differential Phase Error	DP	At 3.58MHz		0.03		degrees

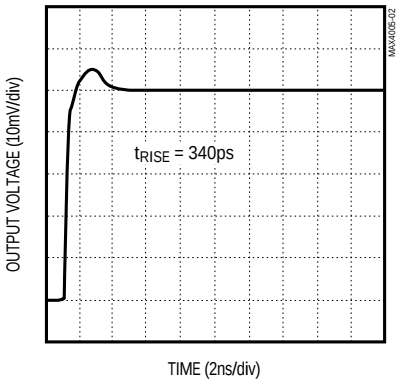
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

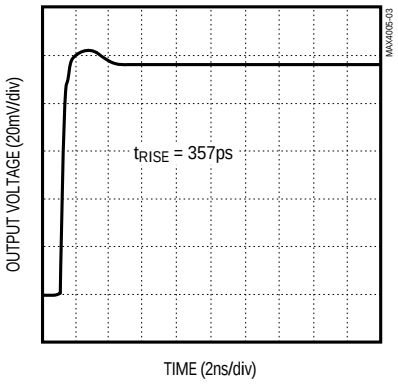
GAIN vs. FREQUENCY



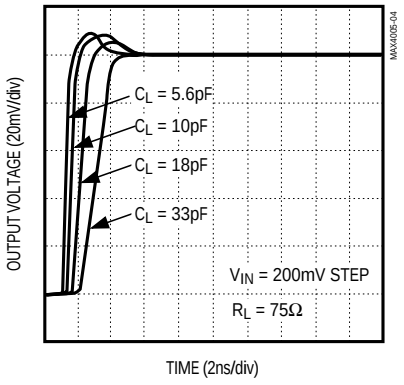
SMALL-SIGNAL STEP RESPONSE



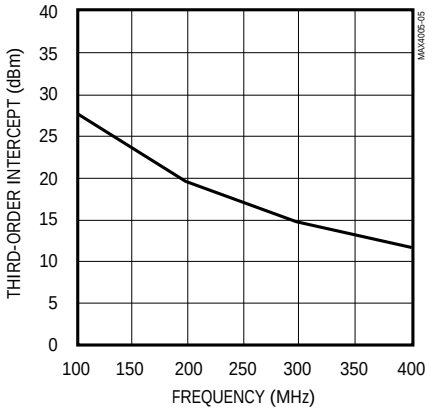
SMALL-SIGNAL STEP RESPONSE



SMALL-SIGNAL STEP RESPONSE vs. CAPACITIVE LOAD



THIRD-ORDER INTERCEPT vs. FREQUENCY



950MHz FET-Input Buffer with 75Ω Output

Pin Description

PIN	NAME	FUNCTION
1, 8	V_{EE}	-5V Negative Supplies
2	IN	High-Impedance Input
3	GND	Ground
4	V_{CC}	+5V Positive Supply
5	V_{CCO}	Output Stage +5V Positive Supply
6	OUT	Output (Z_{OUT} = 75Ω)
7	PEAK	Normally no connection. Capacitor to ground will peak frequency response.

Applications Information

Power Supply

The MAX4005 allows for two separate +5V supplies for the output stage and the rest of the MAX4005 circuit. The supplies are bonded out separately to give the option of using a different +5V supply. The output stage is a Class A type, with the output transistor fed by a current source in the emitter, so its current will vary with output signal. For best bandwidth and pulse response, solder bypass chip capacitors directly from the supply pins on the four corners of the package to a ground plane.

Input Impedance

The MAX4005 has a JFET input with an input capacitance of only 2pF. As a result, the leakage current is typically less than 10pA. This exceptionally high input impedance is important in applications that require isolation between a high source impedance and a low-impedance transmission cable. An attenuator may be used in front of the MAX4005 to increase the dynamic range and reduce input capacitance.

Output Impedance

A 75Ω precision thin-film output resistor is included on-board to provide more precise reverse termination than standard discrete resistors. This minimizes reflections caused by impedance mismatching when driving transmission cable. The MAX4005 can also drive a 50Ω load with only a slight loss in amplitude (gain drops from 0.5 to 0.4). The typical operating performance specifications shown in the *Electrical Characteristics* have been verified with a 50Ω load, as well as a 75Ω load.

Frequency Response Peaking

To peak the response to compensate for losses when driving long transmission lines, connect a chip capacitor of about 10pF to 50pF between the PEAK pin and ground. This peaking occurs in the 200MHz to 500MHz range. The PEAK pin will normally be left open for flattest response.