19-0982; Rev 1; 7/96

MAXIM

Fault-Protected Analog Multiplexer with Latch

General Description

Maxim's MAX368/369 are 8 channel single-ended (1 of 8) and 4 channel differential (2 of 8) fault-protected multiplexers with on-chip data latches. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly improved fault protection over previous devices. If power to the multiplexers is removed while input voltages are still applied, all channels turn off, allowing only a few nanoamperes of leakage current to flow in the inputs. This not only protects the multiplexer and the circuitry connected to the output, but also protects the sensors or signal sources which drive the multiplexer inputs.

When an overvoltage signal of up to ±35V is applied to an analog input of a Maxim fault-protected multiplexer, that input channel turns off. If the overvoltage is applied to an on channel, the multiplexer output is clamped to less than its power supply voltage, thereby protecting sensitive circuitry that may be connected to the multiplexer output.

All channel selection and control inputs are fully compatible with both TTL and CMOS logic levels. In addition, break-before-make switch operation is guaranteed and typical power dissipation is less than 7 milliwatts, which makes the MAX 368/369 ideally suited for portable equipment usage.

Applications

Data Acquisition Systems

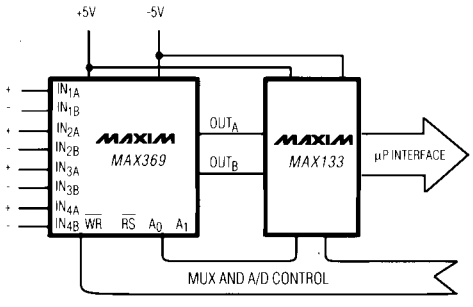
Industrial Process Control Systems

Avionics Test Equipment

Signal Routing Between Systems

Computer Controlled Analog Data Logging

Typical Operating Circuit



Input Protected Differential Input Data Acquisition System

Features

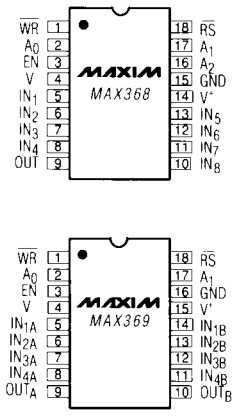
- ♦ All Switches Off with Power Supplies Off
- ♦ Overvoltage Protection up to ±35V
- ♦ Only Nanoamperes of Input Current under All Fault Conditions
- ♦ Latch-Up Proof Construction
- ♦ Operates from ±4.5 to ±18V Supplies
- ♦ All Digital Inputs are TTL and CMOS Compatible
- ♦ Internal Data Latches for Channel Selection

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX368C/D	0°C to +70°C	Dice
MAX368CPN	0°C to +70°C	18 Lead Plastic DIP
MAX368CJN	0°C to +70°C	18 Lead CERDIP
MAX368CWN	0°C to +70°C	18 Lead Wide SO
MAX368EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX368EJN	-40°C to +85°C	18 Lead CERDIP
MAX368EWN	-40°C to +85°C	18 Lead Wide SO
MAX368MJN	-55°C to +125°C	18 Lead CERDIP
MAX369C/D	0°C to +70°C	Dice
MAX369CPN	0°C to +70°C	18 Lead Plastic DIP
MAX369CJN	0°C to +70°C	18 Lead CERDIP
MAX369CWN	0°C to +70°C	18 Lead Wide SO
MAX369EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX369EJN	-40°C to +85°C	18 Lead CERDIP
MAX369EWN	-40°C to +85°C	18 Lead Wide SO
MAX369MJN	-55°C to +125°C	18 Lead CERDIP

Pin Configurations

Top View



Fault-Protected Analog Multiplexer with Latch

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins ..... +44V
V+ ..... +22V
V- ..... -22V
Digital Input Overvoltage:
V_{IN}, V_A { $V_{Supply}(+)$ ..... +4V; $V_{Supply}(-)$ ..... -4V
Analog Input Overvoltage with Multiplexer Power On:
V_S { $V_{Supply}(+)$ ..... +20V; $V_{Supply}(-)$ ..... -20V
Analog Input Overvoltage with Multiplexer Power Off:
V_S { $V_{Supply}(+)$ ..... +35V; $V_{Supply}(-)$ ..... -35V

Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (Note 1) (CERDIP) 1.28W
Operating Temperature Range
MAX368/369C ..... 0°C to +70°C
MAX368/369E ..... -40°C to +85°C
MAX368/369M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +70°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V, GND = 0, WR = 0, RS = 2.4V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP *	TYP	M SUFFIX MIN	M SUFFIX MAX	E, C SUFFIX MIN	E, C SUFFIX MAX	UNITS
ANALOG SWITCH									
Analog Signal Range	V_{ANALOG}	(Note 2)	1		-15	15	15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V_D = ±10V, V_{A_0} = 0.8V, I_S = 100µA, $V_{A_{0-2}}$ = 2.4V	1, 3 2			1500 1800		1800 2000	Ω
Greatest Change in $r_{DS(ON)}$ Between Channels	$\Delta r_{DS(ON)}$	-10V < V_S < 10V	1	10					%
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V	1 2	-0.005	-1 -50	1 50	-5 -50	-5 50	nA
Drain OFF Leakage Current, MAX368	$I_{D(OFF)}$	V_{IN} = 0.8V, V_S = ±10V, V_D = ∓10V	1 2	-0.015	-2 -200	2 200	-5 -200	5 200	nA
Drain OFF Leakage Current, MAX369	$I_{D(OFF)}$	V_{IN} = 0.8V, V_S = ±10V, V_D = ∓10V	1 2	-0.008	-1 -100	1 100	5 100	5 100	nA
Drain ON Leakage Current, MAX368	$I_{D(ON)}$	V_S = V_D = ±10V, V_{IN} = 2.4V, V_{A_0} = 0.8V, $V_{A_{1-2}}$ = 2.4V	1 2	-0.03	-2 200	2 200	5 -200	5 200	nA
Drain ON Leakage Current, MAX369	$I_{D(ON)}$	V_S = V_D = ±10V, V_{IN} = 2.4V, V_{A_0} = 0.8V, $V_{A_{1-2}}$ = 2.4V	1 2	-0.015	-1 -100	1 100	-5 -100	5 100	nA
LOGIC INPUT									
Logic Input Current (Input Voltage High)	I_{AH}	V_A = 2.4V	1, 2, 3	-0.002	-1	1	-1	1	µA
		V_A = 14V	1, 2, 3	0.006	-1	1	-1	1	µA
Logic Input Current (Input Voltage Low)	I_{AL}	V_{IN} = 0 or 2.4V, V_A = 0V, RS = 0V, WR = 0V	1, 2, 3	-0.002	-1	1	1	1	µA
FAULT									
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	V_D = 0V (Note 3), Analog Overvoltage = ±33V	1 2		-10 -2000	10 2000	20 -2000	20 2000	nA
Input Leakage Current (with Overvoltage)	$I_{S(OFF)}$	V_{IN} = ±25V, V_D = +10V (Note 3)	1		-5	5	-10	10	µA
Input Leakage Current (with Power Supplies Off)	$I_{D(OFF)}$	V_{IN} = ±25V, V_{IN} - V_D = 0V, A_0 = A_1 = A_2 = 0V or 5V	1		-2	2	-5	5	µA

*1 = 25°C, 2 = 125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, GND = 0, WR = 0, $\overline{RS}$ = 2.4V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP *	TYP	M SUFFIX MIN	M SUFFIX MAX	E,C SUFFIX MIN	E,C SUFFIX MAX	UNITS
DYNAMIC									
Switching Time of Multiplexer	t_{TRANS}	See Figure 2	1	0.6		1		1	µs
Break-Before-Make Interval	t_{OPEN}	See Figure 4	1	0.2					
Enable and Write Turn ON Time	$t_{ON(EN,WR)}$	See Figures 3 and 5	1	1		1.5		1.5	
Enable and Reset Turn OFF Time	$t_{OFF(EN,RS)}$	See Figures 3 and 6	1	0.4		1		1	
Charge Injection	Q	See Figure 7 and Tables 1A and 1B	1	55					pC
OFF Isolation	OIRR	V_{EN} = 0, R = 1kΩ, C_L = 15pF, V_{EN} = 7V_{RMS}, f = 100kHz	1	68					dB
Logic Input Capacitance with Switch OFF	C_{IN}	f = 1MHz	1	5					pF
Input Capacitance with Switch OFF	$C_{S(OFF)}$	V_{EN} = 0, V_S = 0, f = 140kHz	1	5					pF
Output Capacitance with Switch OFF — MAX368	$C_{D(OFF)}$	V_{EN} = 0, V_{OUT} = 0, f = 140kHz	1	25					pF
Output Capacitance with Switch OFF — MAX369	$C_{D(OFF)}$	V_{EN} = 0, V_{OUT} = 0, f = 140kHz	1	12					pF
WR Pulse Width	t_{WW}	See Figure 1	1, 2, 3		300		300		ns
A_X, EN Data Valid to WR	t_{DW}	Set-up Time See Figure 1	1, 2, 3		180		180		ns
A_X, EN Data Valid after WR	t_{WD}	Hold Time See Figure 1	1, 2, 3	0	10		30		ns
RS Pulse Width	t_{RS}	V_{EN} = 5V See Figure 1	1, 2, 3		300		500		ns
SUPPLY									
Positive Supply Current	I^+	V_{EN} = 2.4V, V_A = 0V/5V	1, 2, 3			1.25 1.5		1.5 2.0	mA
Negative Supply Current	I^-		1, 2, 3		-0.1 -0.2		-0.1 -0.2		mA

*1 = 25°C, 2 = -125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

Note 2: When the analog signal exceeds +13.5V or -12V, the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
Note 3: The value shown is the steady state value. The transient leakage is typically 10µA. See detailed description.
Note 4: Electrical Characteristics, such as ON Resistance will change when power supplies other than ±15V are used.
Note 5: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Fault-Protected Analog Multiplexer with Latch

TRUTH TABLE — MAX368

A_2	A_1	A_0	EN	WR	RS	ON SWITCH
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (Latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE — MAX369

A_1	A_0	EN	WR	RS	ON SWITCH
Latching					
X	X	X	↑	1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (Latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

NOTE: Logic "1" $V_{A+1} \geq 2.4V$, Logic "0" $V_A \leq 0.8V$

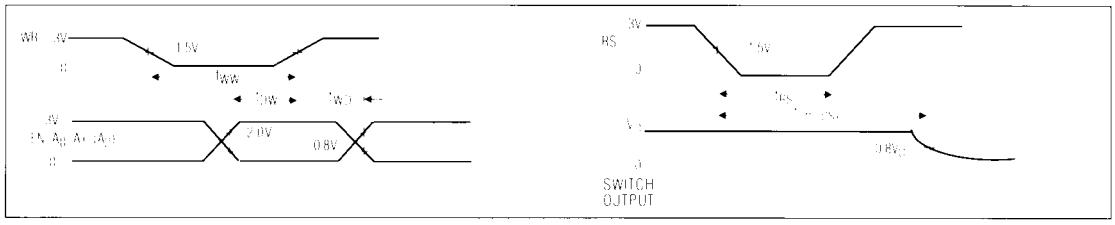


Figure 1. Typical Timing Diagrams for MAX368/369

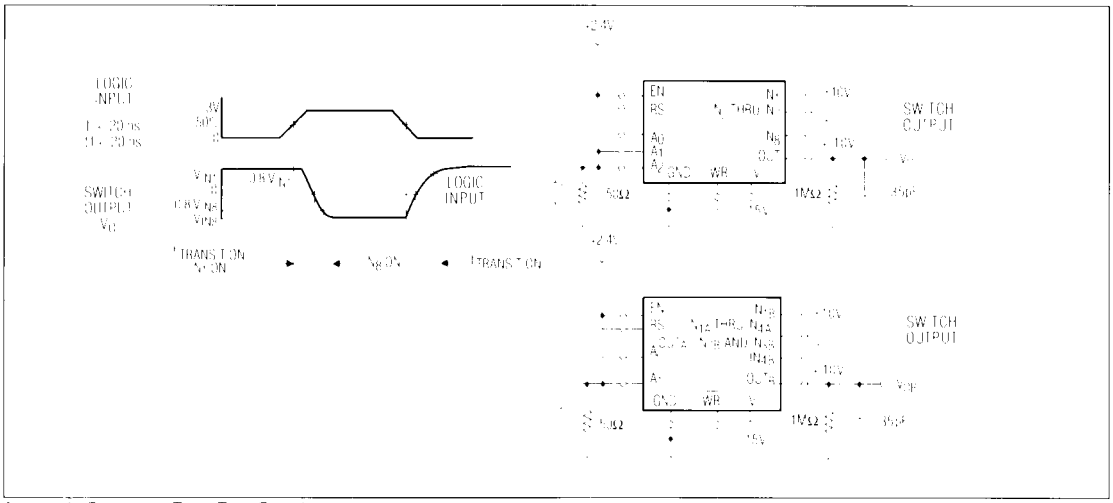


Figure 2. Transition Time Test Circuits

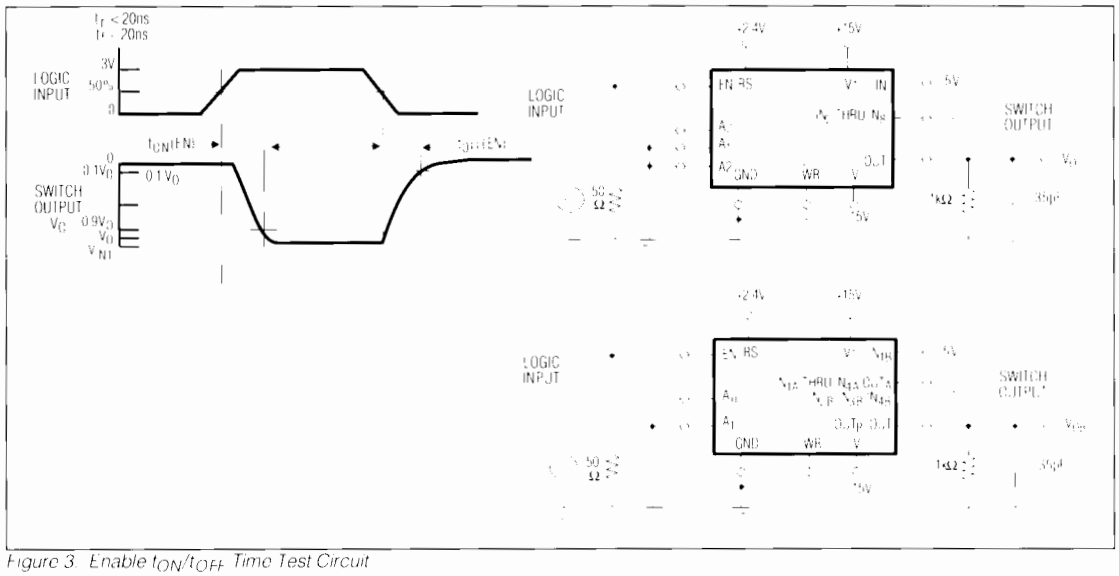


Figure 3. Enable t_{ON}/t_{OFF} Time Test Circuit

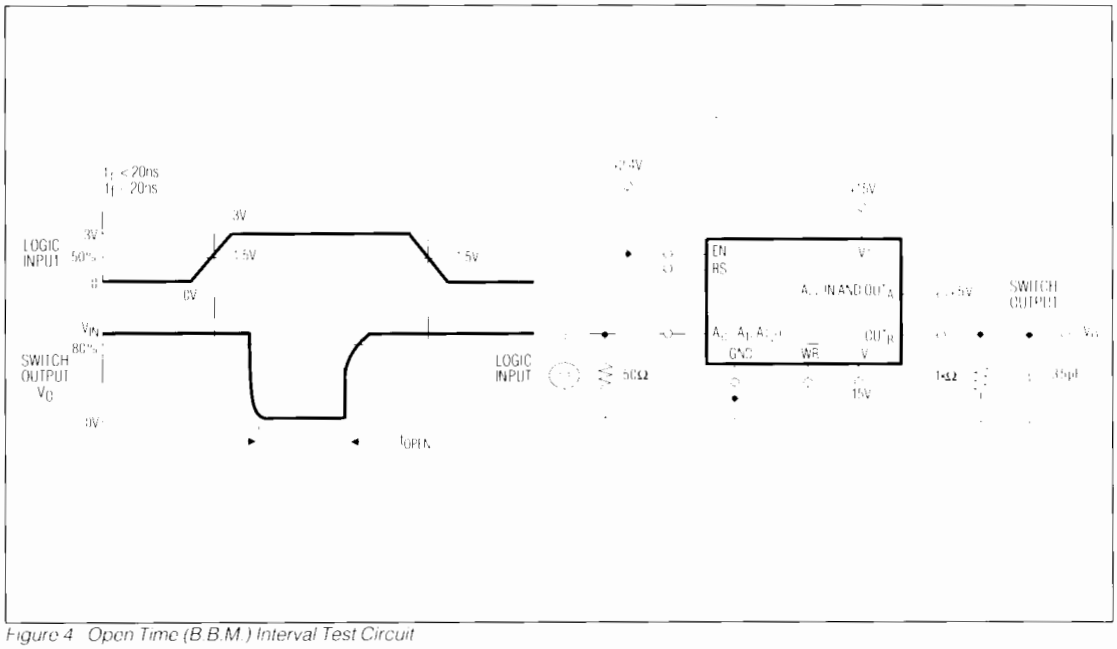


Figure 4. Open Time (B.B.M.) Interval Test Circuit

Fault-Protected Analog Multiplexer with Latch

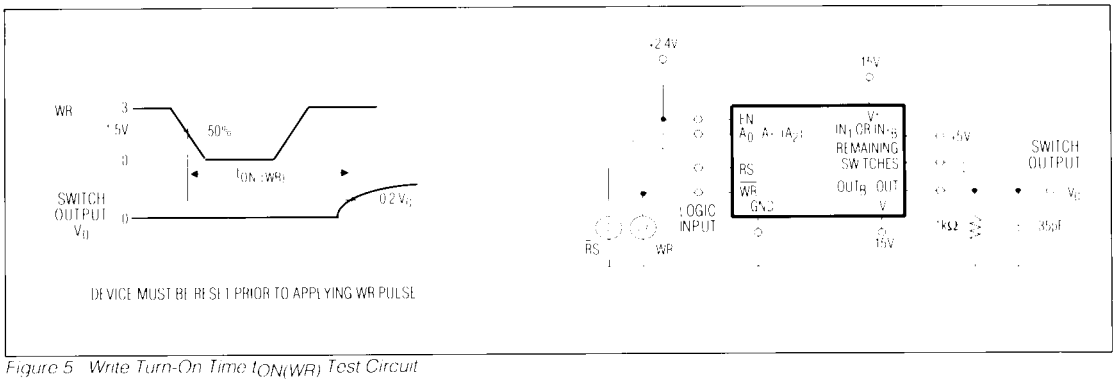


Figure 5. Write Turn-On Time $t_{ON(WR)}$ Test Circuit

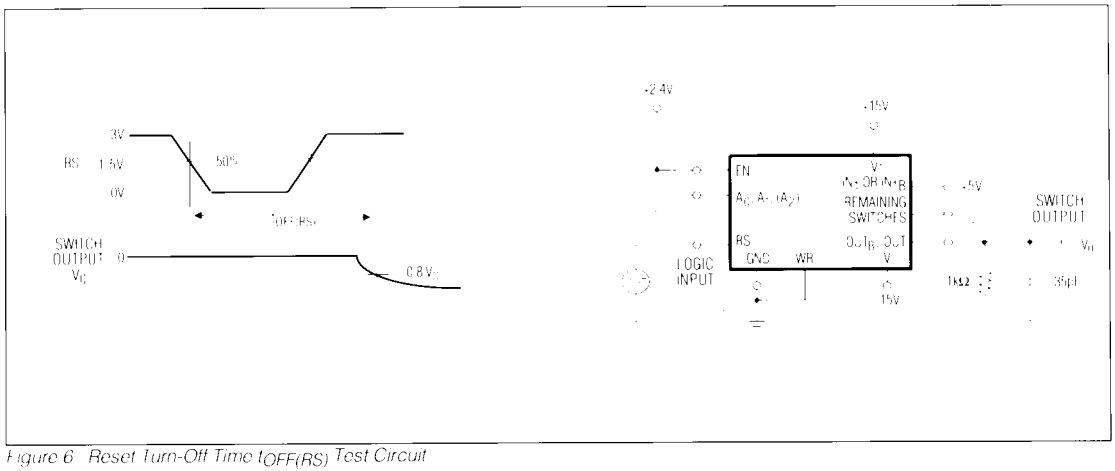


Figure 6. Reset Turn-Off Time $t_{OFF(RS)}$ Test Circuit

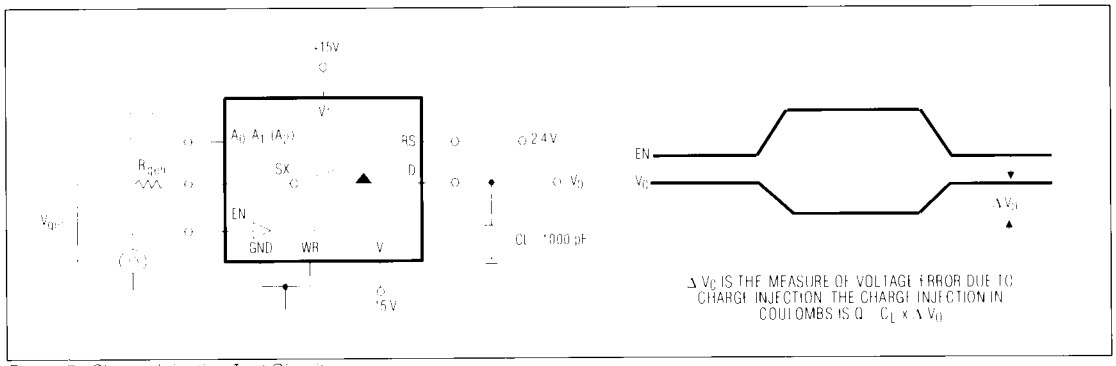


Figure 7. Charge Injection Test Circuit

Detailed Description

Fault Protection Circuitry

Maxim's MAX368/369 are fully fault-protected for continuous input voltages up to ±35V, whether or not the $+V_{SUP}$ and $-V_{SUP}$ power supplies are present. These devices use a "series FET" protection scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all the FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any over voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an OFF channel with $+V_{SUP}$ and $-V_{SUP}$ present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from -35V to +35V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages the fault current will initially be 10 or 20µA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 11 shows the condition of the ON channel with $+V_{SUP}$ and $-V_{SUP}$ present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds $+V_{SUP}$ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than $-V_{SUP}$ minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies.

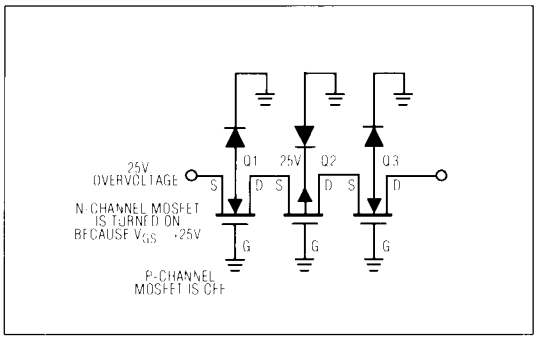


Figure 8. -25V Overvoltage with Multiplexer Power OFF

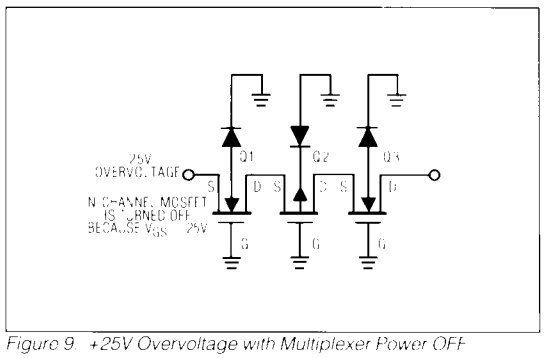


Figure 9. +25V Overvoltage with Multiplexer Power OFF

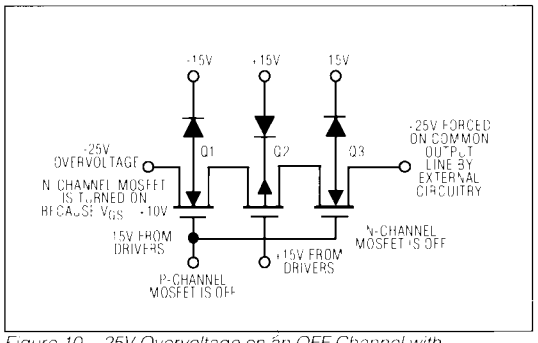


Figure 10. -25V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

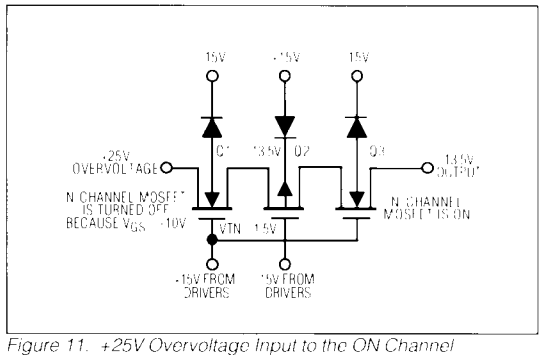


Figure 11. +25V Overvoltage Input to the ON Channel

Fault-Protected Analog Multiplexer with Latch

The Typical Operating Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated overvoltage of these devices is ±35V, the MAX368/369 typically has excellent performance up to ±40V, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX368/369 provides superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Digital Control Circuitry

The internal structure of the MAX368/369 includes translators for the A_0, A_1, A_2, EN, RS, and WR digital inputs, latches, a decode section for channel selection (see Truth Tables on the fourth page of this data sheet). The gate structure consists of series N-channel/ P-channel/ N-channel MOSFETs (see Figure 12). This combination produces a very rugged, fault tolerant multiplexer with address latch capability, and does so with extremely low power dissipation.

Write ($\overline{WR}$), and Reset ($\overline{RS}$) strobes are provided for interfacing with microprocessor bus lines (Figure 13), alleviating the need for the microprocessor to provide constant address inputs to the MUX in order to hold on to a particular channel.

When the write strobe is in the low state (less than 0.8V), and the reset strobe is in the high state (greater than 2.4V), the MUXs are in the transparent mode; this means that the MUXs act similar to non-latching MUXs such as the MAX358/359 or the HI-508A/509A.

When the write input goes to the high state (>2.4V), the previous BCD address input will be latched and held in that state indefinitely. To pull the MUX out of this state, either the write input (WR) must be taken low (0.8V), back to the transparent state, or the Reset ($\overline{RS}$) input taken low, turning off all channels.

The function of the Reset input is to allow for turning off all channels when the $\overline{RS}$ input is low (<0.8V); this has the dual function of resetting channel selection back to the channel 1 mode.

The MAX368/369 is designed to work with single as well as dual supplies, and good performance can be expected in the 9V to 22V single supply range. For example, with a single +15V power supply, analog signals in the range of +3.3V to +12V can be switched normally, and overvoltages up to ±35V can still be tolerated. If negative signals, around 0V are expected, a negative supply is needed. However, only -5V is needed to normally switch signals in the -2V to +12V range (-5V, +15V supplies). No current is drawn from the negative supply, so Maxim's MAX635 D/C to D/C converter does the job very nicely.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more MAX368s are cascaded to build 16-line and larger analog signal input multiplexers.

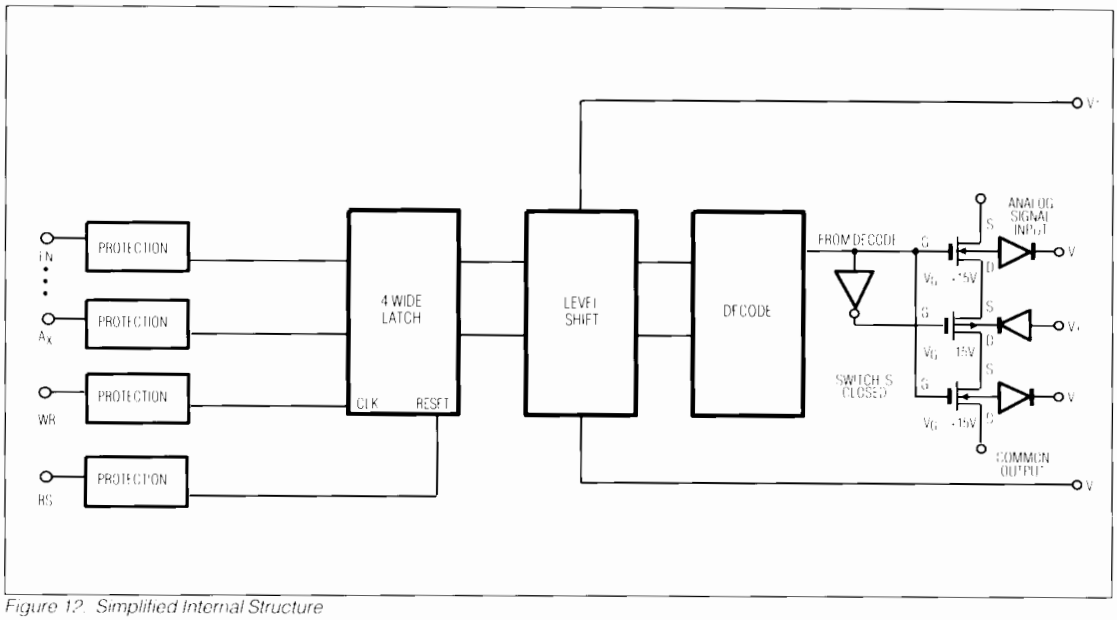
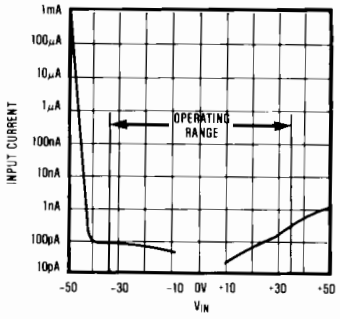


Figure 12. Simplified Internal Structure

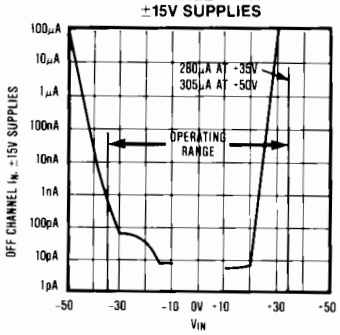
Fault-Protected Analog Multiplexer with Latch

Typical Operating Characteristics

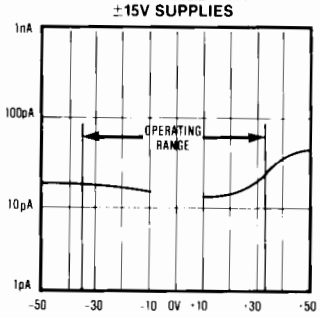
INPUT LEAKAGE VS. INPUT VOLTAGE WITH $V^+ = V^- = 0V$



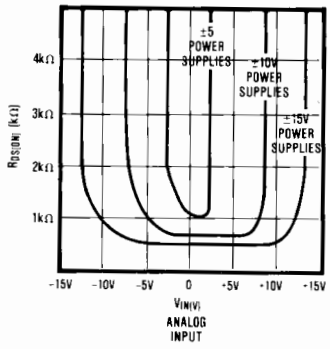
OFF CHANNEL LEAKAGE CURRENT VS. INPUT VOLTAGE WITH ±15V SUPPLIES



OUTPUT LEAKAGE VS. OFF CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$R_{DS(ON)}$ VS. INPUT VOLTAGE



Applications

Operation with Supply Voltages Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX368/369 limits the output voltage to about 1.5V below $+V_{SUP}$ and about 3V above V_{SUP}. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The Typical Operating Characteristics graphs show typical $R_{DS(ON)}$ for ±15V, ±10V, and ±5V power supplies. Maxim guarantees the MAX368/369 for operation from ±4.5V to ±18V supplies. The switching delays increase by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX368/369 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold will remain approximately 1.6V above the GROUND pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between $+V_{SUP}$ and $-V_{SUP}$. Connect $-V_{SUP}$ to 0V when operating with a +9V to +22V single supply.

The MAX368/369 digital threshold is relatively independent of the power supply voltages, going from a typical 1.6V when $+V_{SUP}$ is 15V to 1.5V typical with a 5V $+V_{SUP}$. This means that Maxim's MAX368/369 will operate with standard TTL logic levels, even with ±5V power supplies. In all cases, the threshold of the Enable pin is the same as the other logic inputs.

Operation as a Demultiplexer

The MAX368/369 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX368/369 provide both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Fault-Protected Analog Multiplexer with Latch

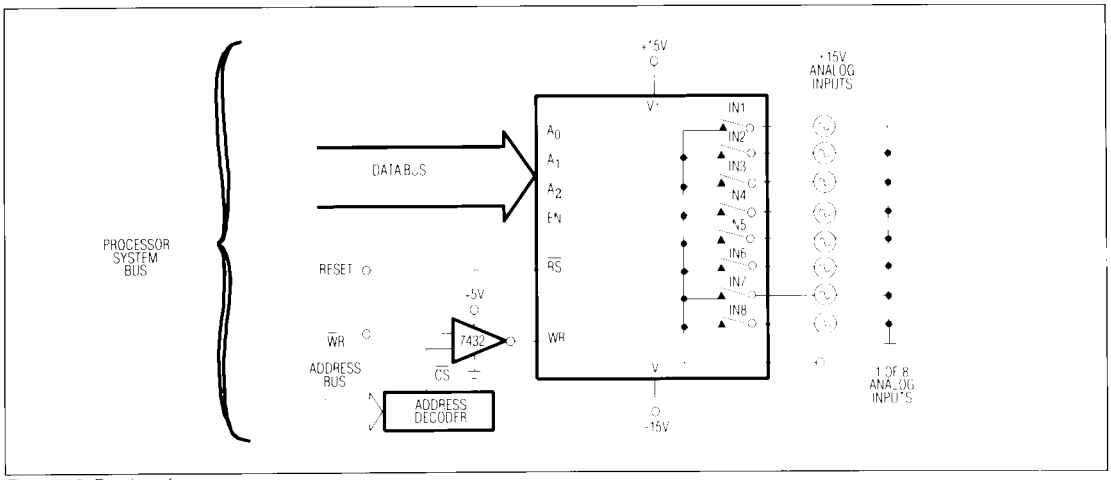


Figure 13. Bus Interface

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage for the MAX368 and MAX369. Note that since the channels are well matched, the differential charge injection for the MAX368/369 is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break-before-make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as that shown in Figure 13, the dominant delay is not the switching time of the MAX368/MAX369 multiplexer but is the settling time of the following amplifier and sample/hold. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output approximately doubles the settling time for 0.01% accuracy settling.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of approximately -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the GROUND pin.

Table 1A. MAX368 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge
±5V	+1.7V	+100pC
	0V	+70pC
	-1.7V	+45pC
±10V	+5V	+200pC
	0V	+130pC
	-5V	+60pC
±15V	+10V	+300pC
	0V	+180pC
	-10V	+50pC

Test Conditions: C_L = 1000pF on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2 = 0V$, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX369 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A - B
±5V	+1.7V	+105pC	+107pC	-2pC
	0V	+73pC	+48pC	-1pC
	-1.7V	+48pC	+50pC	-2pC
±10V	+5V	+215pC	+220pC	-5pC
	0V	+135pC	+139pC	-4pC
	-5V	+62pC	+63pC	-1pC
±15V	+10V	+325pC	+330pC	-5pC
	0V	+180pC	+185pC	-5pC
	-10V	+55pC	+55pC	0pC

Test Conditions: C_L = 1000pF on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, $A_1 = 0V$, A_0 is toggled from 0V to 3V at a 2kHz rate.

The digital inputs can also be driven with CMOS logic levels swinging from either $+V_{SUP}$ to $-V_{SUP}$ or from $+V_{SUP}$ to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1µA. The digital inputs are protected from ESD by a 30V zener diode between the input and $+V_{SUP}$, and can be driven ±6V beyond the supplies without drawing excessive current.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies, the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX368/369 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX368/369 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases, since the load driven by the MAX368/369 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled.

When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GROUND and $-V_{SUP}$ pins. The groundplane formed by these lines is continued onto the MAX368/369 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. TYPICAL OFF ISOLATION REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: $V_{IN} = 20V_{PK-PK}$ at the tabulated frequency, R_L = 1.5k between OUT and ground, EN = 0V.

$$OIRR = 20 \text{ Log } \frac{20\ V_{PK-PK}}{V_{OUT\ (PK-PK)}}$$

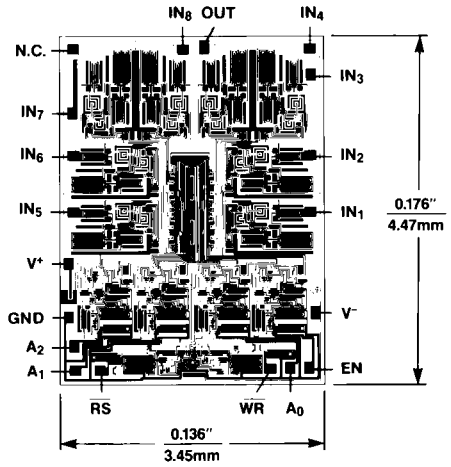
Table 2B. TYPICAL CROSSTALK REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
R_L = 1.5k	70dB	68dB	64dB
R_L = 10k	62dB	46dB	42dB

Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, $A_0 = A_1 = A_2 = 0V$ (Channel 1 selected). $20V_{PK-PK}$ at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Chip Topographies

MAX368



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