DS2784

1-Cell Stand-Alone Fuel Gauge IC with Li+ Protector and SHA-1 Authentication

www.maxim-ic.com

GENERAL DESCRIPTION

The DS2784 operates from 2.5V to 4.6V for integration in battery packs using a single lithium-ion (Li+) or Li+ polymer cell. Available capacity is reported in mAh and as a percentage. Safe operation is ensured with the included Li+ protection function and SHA-1-based challenge-response authentication.

Precision measurements of voltage, temperature, and current, along with cell characteristics and application parameters are used to estimate capacity. The available capacity registers report a conservative estimate of the amount of charge that can be removed given the current temperature and discharge rate.

In addition to the nonvolatile (NV) storage for cell compensation and application parameters, 16 bytes of EEPROM memory is made available for the exclusive use of the host system and/or pack manufacturer. This facilitates battery lot and date tracking or NV storage of system or battery usage statistics.

A 1-Wire® interface provides serial communication at 16kbps or 143kbps to access data registers, control registers, and user memory. Additionally, 1-Wire communication enables challenge-response pack authentication using SHA-1 as the hash algorithm in a hash-based message authentication code (HMAC) authentication protocol.

APPLICATIONS

Smartphones/PDAs
Digital Still and Video Cameras
Cordless VOIP Phones
Portable GPS Navigation

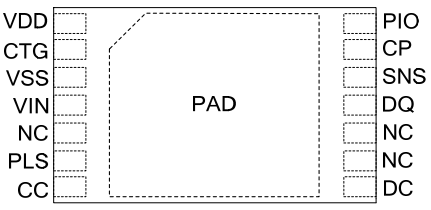
Modes and commands are capitalized for clarity.

1-Wire is a registered trademark of Dallas Semiconductor, a wholly owned subsidiary of Maxim Integrated Products, Inc.

FEATURES

- **Precision Voltage, Temperature, and Current Measurement System**
- **Available Capacity Estimated from Coulomb Count, Discharge Rate, Temperature, and Cell Characteristics**
- **Estimates Cell Aging Using Learn Cycles**
- **Uses Low-Cost Sense Resistor**
- **Allows for Calibration of Gain and Temperature Coefficient**
- **Li+ Safety Circuitry—Overvoltage, Undervoltage, Overcurrent, Short-Circuit Protection**
- **Programmable Safety Thresholds for Overvoltage and Overcurrent**
- **Authentication Using SHA-1 Algorithm and 64-Bit Secret**
- **32-Byte Parameter EEPROM**
- **16-Byte User EEPROM**
- **Dallas 1-Wire Interface with 64-Bit Unique ID**
- **Tiny, Pb-Free, 14-Pin TDFN Package Embeds Easily in Battery Packs Using Thin Prismatic Cells**

PIN CONFIGURATION



3mm x 5mm TDFN - 14
Top View

ORDERING INFORMATION

PART	TEMP RANGE	TOP MARK	PIN PACKAGE
DS2784G+	-40°C to +85°C	DS2784	14 TDFN (3mm x 5mm)
DS2784G+T&R	-40°C to +85°C	DS2784	14 TDFN (3mm x 5mm)

+ Denotes a lead-free package.
T&R = tape and reel

REV: 092507

ABSOLUTE MAXIMUM RATINGS

Voltage Range on PLS Pin Relative to V_{SS}	-0.3V to +18V
Voltage Range on CP Pin Relative to V_{SS}	-0.3V to +12V
Voltage Range on DC Pin Relative to V_{SS}	-0.3V to (CP + 0.3V)
Voltage Range on CC Pin Relative to V_{SS}	V_{DD} - 0.3V to CP + 0.3V
Voltage Range on All Other Pins Relative to V_{SS}	-0.3V to +6.0V
Maximum Voltage Range on V_{IN} Pin Relative to V_{DD}	V_{DD} + 0.3V
Continuous Sink Current, PIO, DQ	20mA
Continuous Sink Current, CC, DC	10mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature (10s)	See IPC/JEDEC J-STD-020

**This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 4.6V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	2.5		4.6	V
Supply Current	I_{DD0}	Sleep mode		1	4	µA
	I_{DD1}	Sleep mode, V_{DD} = 2.5V 0°C to +50°C		0.4	1.5	
	I_{DD2}	Active mode		85	125	
	I_{DD3}	Active mode during SHA computation		300	500	µA
Temperature Accuracy			-3		+3	°C
Temperature Resolution				0.125		
Temperature Range			-128.000		+127.875	
Voltage Accuracy, V_{IN}		4.0 ≤ V_{IN} ≤ 4.6, V_{IN} ≤ V_{DD} + 0.3V	-30		30	mV
		2.5 ≤ V_{IN} ≤ 4.6V, V_{IN} ≤ V_{DD} + 0.3V	-50		+50	
Voltage Resolution, V_{IN}				4.88		mV
Voltage Range, V_{IN}			0		4.99	V
Input Resistance, V_{IN}			15			MΩ
Current Resolution				1.56		µV
Current Full Scale			-51.2		+51.2	mV
Current Gain Error			-1		+1	% full scale
Current Offset		(Notes 2, 3, 4)	-15		+25	µV
Accumulated Current Offset		(Notes 2, 3, 4)	-360		0	µVh/day
Time Base Error		0ºC ≤ T_A ≤ +50ºC	-2		+2	%
			-3		+3	
CP Output Voltage	V_{CP}	I_{CC} + I_{DC} = 0.9µA	8.50	9.25	10.00	V
CP Startup Time	t_{SCP}	CE = 0, DE = 0, C_{CP} = 0.1µF, Active mode			200	ms
Output High: CC, DC	V_{OHCC} V_{OHDC}	I_{OH} = -100µA (Note 5)	V_{CP} - 0.4			V
Output Low: CC	V_{OLCC}	I_{OL} = 100µA			V_{DD} + 0.1	V
Output Low: DC	V_{OLDC}	I_{OL} = 100µA			0.1	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DQ, PIO Voltage Range			-0.3		+5.5	V
DQ, PIO Input-Logic High	V_{IH}		1.5			V
DQ, PIO Input-Logic Low	V_{IL}				0.6	V
DQ, PIO Output-Logic Low	V_{OL}	IOL = 4mA			0.4	V
DQ, PIO Pullup Current	I_{PU}	Sleep mode, $V_{PIN} = V_{DD}$ - 0.4V		0.2		µA
DQ, PIO Pulldown Current	I_{PD}	Active mode, V_{PIN} = 0.4V		0.2		µA
DQ Input Capacitance	C_{DQ}			50		pF
DQ Sleep Timeout	t_{SLEEP}	DQ < V_{IL}	2		9	s
PIO, DQ Wake Debounce	t_{WDB}	Sleep mode		100		ms
SHA-1 COMPUTATION TIMING						
Computation Time	t_{SHA}				30	ms

ELECTRICAL CHARACTERISTICS: Protection Circuit

(V_{DD} = 2.5V to 4.6V, T_A = 0°C to +50°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detect	V_{OV}	V_{OV} = 11000b	4.457	4.482	4.507	V
		V_{OV} = 00011b	4.252	4.277	4.302	
Charge-Enable Voltage	V_{CE}	Relative to V_{OV}	-75	-100	-125	mV
Undervoltage Detect	V_{UV}		2.40	2.45	2.50	V
Overcurrent Detect: Charge	V_{COC}	OC = 11b	-57	-72	-87	mV
		OC = 00b	-15.5	-23.5	-31.5	
Overcurrent Detect: Discharge	V_{DOC}	OC = 11b	76	96	116	mV
		OC = 00b	23.5	35.5	47.5	
Short-Circuit Current Detect	V_{SC}	SC = 1b	240	300	360	mV
		SC = 0b	120	150	180	mV
Overvoltage Delay	t_{OVD}	(Note 6)	425		1150	ms
Undervoltage Delay	t_{UVD}	(Notes 6, 7)	84		680	ms
Overcurrent Delay	t_{OCD}		8	10	12	ms
Short-Circuit Delay	t_{SCD}		80	120	160	µs
Test Threshold	V_{TP}	COC, DOC conditions	0.3	0.8	1.5	V
Test Current	I_{TST}	SC, COC, DOC condition	10	20	40	µA
PLS Pulldown Current	I_{PPD}	Sleep mode	30	200	600	µA
Recovery Current	I_{RC}	VUV condition, max: V_{PLS} = 15V, V_{DD} = 1V min: V_{PLS} = 4.2V, V_{DD} = 2V	2.5	5.0	10.00	mA

EEPROM RELIABILITY SPECIFICATION

(V_{DD} = 2.5V to 5.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Copy Time	t_{EEC}				10	ms
EEPROM Copy Endurance	N_{EEC}	T_A = +50°C	50,000			cycles

ELECTRICAL CHARACTERISTICS: 1-Wire Interface, Standard

(V_{DD} = 2.5V to 5.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		60		120	µs
Write-1 Low Time	t_{LOW1}		1		15	µs
Read-Data Valid	t_{RDV}				15	µs
Reset-Time High	t_{RSTH}		480			µs
Reset-Time Low	t_{RSTL}		480		960	µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs

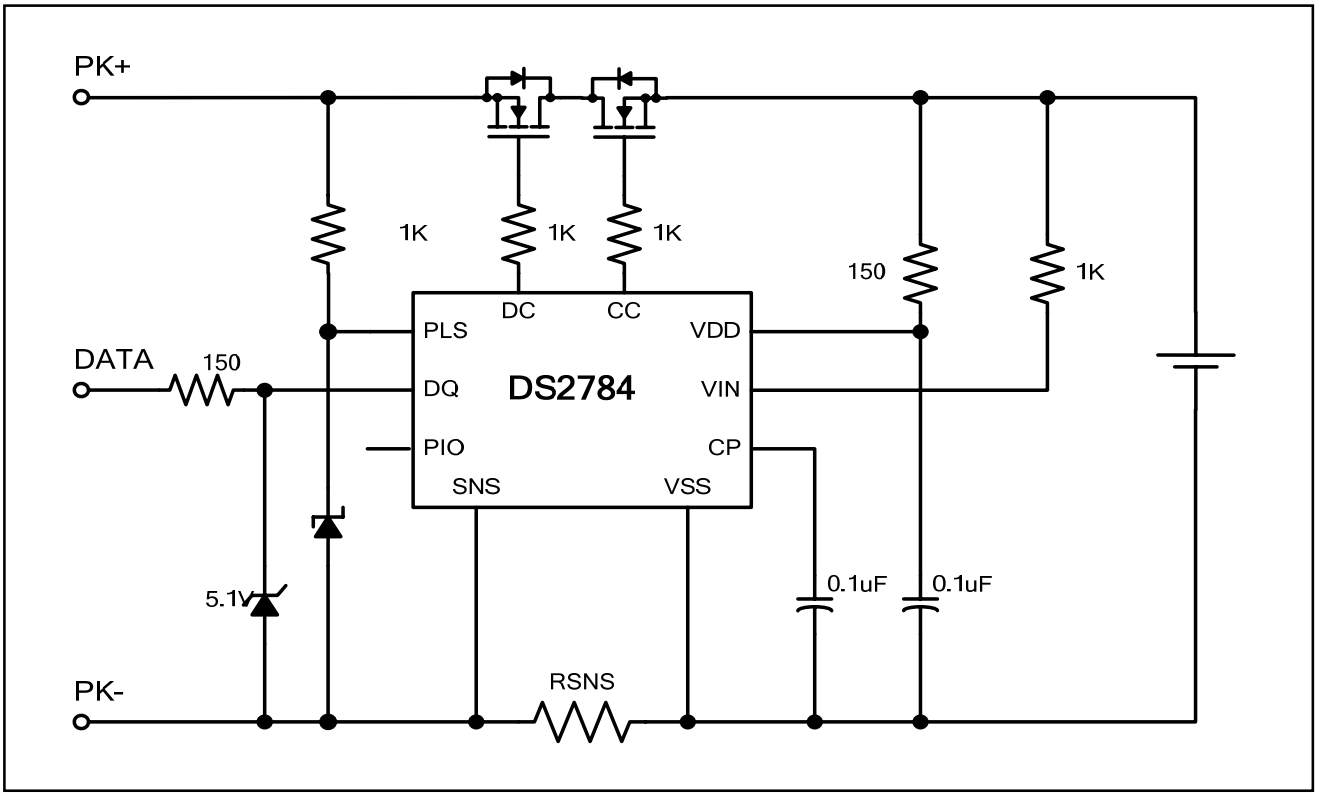
ELECTRICAL CHARACTERISTICS: 1-Wire Interface, Overdrive

(V_{DD} = 2.5V to 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		6		16	µs
Write-1 Low Time	t_{LOW1}		1		2	µs
Read-Data Valid	t_{RDV}				2	µs
Reset-Time High	t_{RSTH}		48			µs
Reset-Time Low	t_{RSTL}		48		80	µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs

Note 1: All voltages are referenced to V_{SS}.
Note 2: Factory-calibrated accuracy. Higher accuracy can be achieved by in-system calibration by the user.
Note 3: Accumulation bias and offset bias registers set to 00h. NBEN bit set to 0.
Note 4: Parameters guaranteed by design.
Note 5: CP pin externally driven to 10V.
Note 6: Overvoltage and undervoltage delays (t_{OVD}, t_{UVD}) are reduced to 0s if the OV or UV condition is detected within 100ms of entering Active mode.
Note 7: t_{UVD} MIN determined by stepping the voltage on V_{IN} from V_{UV} + 250mV to V_{UV} - 250mV.

TYPICAL OPERATING CIRCUIT



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input. Chip supply input. Bypass with 0.1µF to V_{SS}.
2	CTG	Connect to Ground
3	V_{SS}	Device Ground. Chip ground and battery-side sense resistor input.
4	V_{IN}	Battery Voltage-Sense Input. Connect to positive cell terminal through decoupling network.
5, 9, 10	N.C.	No Connection
6	PLS	Pack Plus Terminal-Sense Input. Used to detect the removal of short-circuit, discharge overcurrent, and charge overcurrent conditions.
7	CC	Charge Control. Charge FET control output.
8	DC	Discharge Control. Discharge FET control output.
11	DQ	Data Input/Output. Serial data I/O, includes weak pulldown to detect battery disconnect and can be configured as wake input.
12	SNS	Sense Resistor Connection. Pack minus terminal and pack-side sense resistor sense input.
13	CP	Charge Pump Output. Bypass with 0.1µF to V_{SS}.
14	PIO	Programmable I/O Pin. Can be configured as wake input.
PAD	PAD	Exposed Pad. Connect to V_{SS} or float.

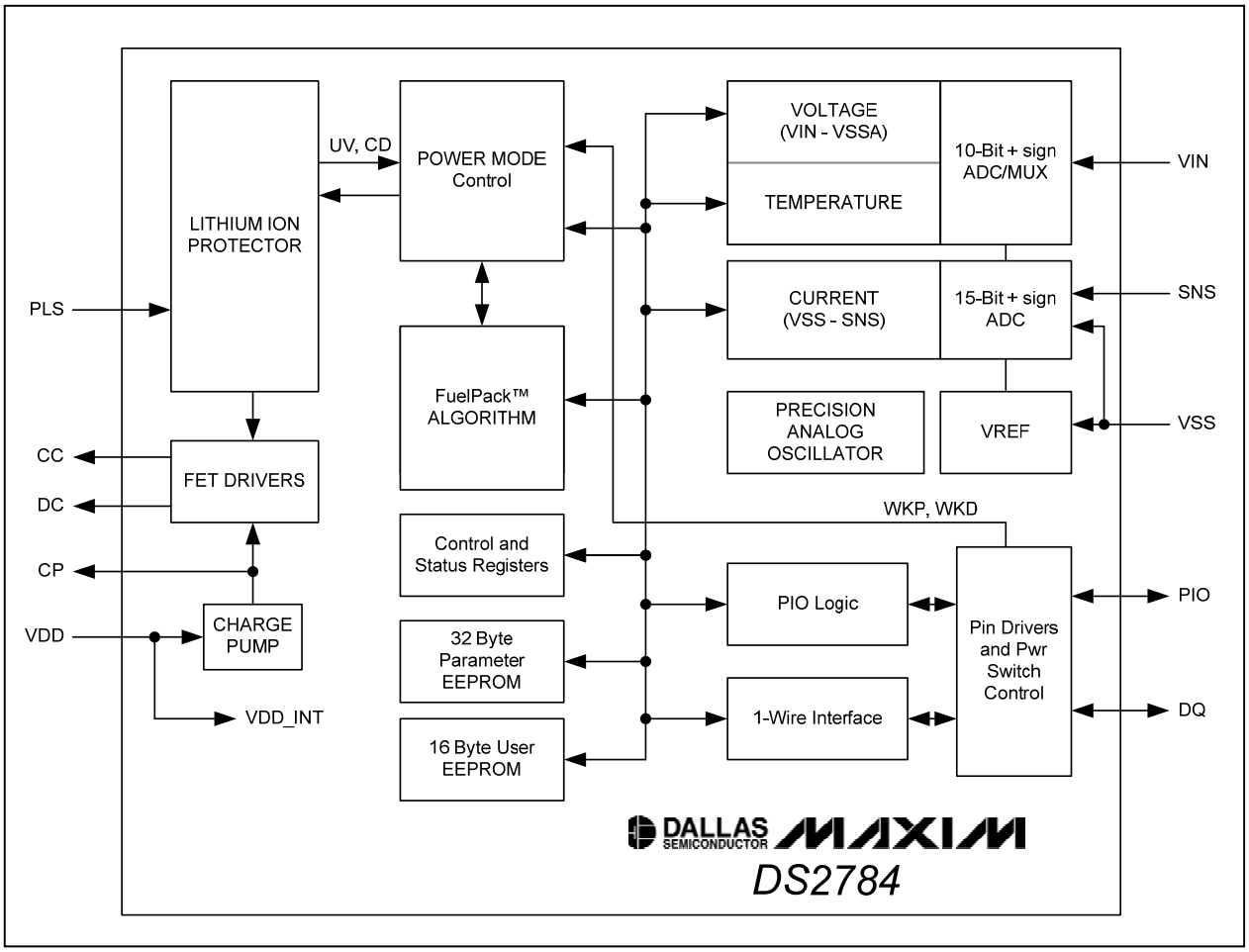
DETAILED DESCRIPTION

The DS2784 functions as an accurate fuel gauge, Li+ protector, and SHA-1-based authentication token. The fuel gauge provides accurate estimates of remaining capacity and reports timely voltage, temperature, and current-measurement data. Capacity estimates are calculated from a piecewise-linear model of the battery performance over load and temperature, and system parameters for full and empty conditions. The algorithm parameters are user programmable and can be modified in pack. Critical capacity and aging data are periodically saved to EEPROM in case of loss of power due to a short circuit or deep depletion.

The Li+ protection function ensures safe, high-performance operation. nFET protection switches are driven with a 9V charge pump that increase gate drive as the cell voltage decreases. The high-side topology preserves the ground path for serial communication while eliminating the parasitic charge path formed when the fuel gauge IC is located inside the protection FETs in a low-side configuration. The thresholds for overvoltage, overcurrent, and short-circuit current are user programmable for easy customization to each cell and application.

The 32-bit wide SHA-1 engine with 64-bit secret and 64-bit challenge words resists brute force and other attacks with financial-level HMAC security. The challenge of managing secrets in the supply chain is addressed with the compute next secret feature. The unique serial number or ROM ID can be used to assign a unique secret to each battery.

BLOCK DIAGRAM



POWER MODES

The DS2784 has two power modes: Active and Sleep. On initial power-up, the DS2784 defaults to Active mode. In Active mode, the DS2784 is fully functional with measurements and capacity estimation registers continuously updated. The protector circuit monitors the battery voltages and current for unsafe conditions. The protection FET gate drivers are enabled when conditions are deemed safe. Also, the SHA-1 authentication function is available in Active mode. When a SHA-1 computation is performed, the supply current increases to I_{DD3} for t_{SHA}. In Sleep mode, the DS2784 conserves power by disabling measurement and capacity estimation functions, but preserves register contents. Gate drive to the protection FETs is disabled in Sleep. And the SHA-1 authentication feature is not operational.

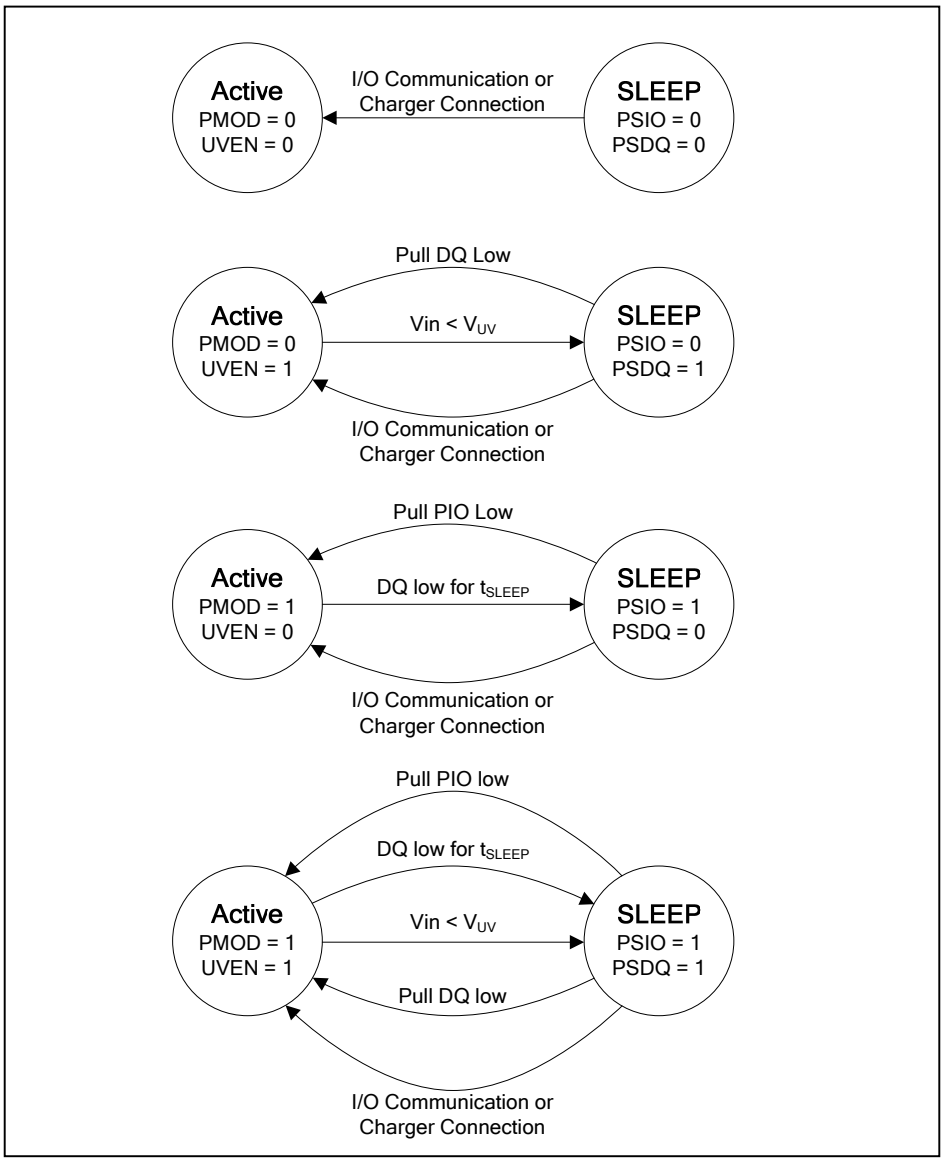
Sleep mode is entered under two different conditions: bus low and undervoltage. An enable bit makes entry into Sleep optional for each condition. Sleep mode is not entered if a charger is connected ($V_{PLS} > V_{DD}$ + 50mV) or if a charge current of 1.6mV / R_{SNS} is measured from SNS to V_{SS}. The DS2784 exits Sleep mode upon charger connection and $V_{IN} \geq V_{UV}$ or a low to high transition on DQ.

The bus-low condition, where the DQ pin is low for t_{SLEEP}, indicates pack removal or system shutdown in which the 1-Wire bus pullup voltage, V_{PULLUP}, is not present. The power mode (PMOD) bit must be set to enter Sleep when a bus-low condition occurs. After the DS2784 enters Sleep due to a bus-low condition, it is assumed that no charge or discharge current will flow and that coulomb counting is unnecessary.

The second condition to enter Sleep is an undervoltage condition, which reduces battery drain due to the DS2784 supply current and prevents over discharging the cell. The DS2784 transitions to Sleep if the V_{IN} voltage is less than V_{UV} (2.45V typical) and the undervoltage enable (UVEN) bit is set. The 1-Wire bus must be in a static state, that is, with DQ either high or low for t_{SLEEP}. The DS2784 transitions from UVEN Sleep to Active mode when DQ changes logic state.

The DS2784 has the “power switch” capability for waking the device and enabling the protection FETs when the host system is powered down. A simple dry-contact switch on the PIO pin or DQ pin can be used to wake up the battery pack. The power switch function is enabled using the PSPIO and PSDQ configuration bits in the control register. When PSPIO or PSDQ is set and a Sleep condition is satisfied, the PIO and DQ pins pull high weakly, then become armed to detect a low-going transition. A 100ms debounce period filters out glitches that can be caused when a sleeping battery is inserted into a system.

Figure 1. Sleep Mode State Diagram



CONTROL REGISTER FORMAT

All control register bits are read and write accessible. The control register is recalled from parameter EEPROM memory at power-up. Register bit values can be modified in shadow RAM after power-up. Power-up default values are saved using the Copy Data command.

ADDRESS 60h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NBEN	UVEN	PMOD	RNAOP	0	PSPIO	PSDQ	X

NBEN—Negative Blanking Enable. A value of 1 enables blanking of negative current values up to 25μV. A value of 0 disables blanking of negative currents. The power-up default of NBEN = 0.

UVEN—Undervoltage Enable. A value of 1 allows the DS2784 to enter Sleep mode when the voltage register value is less than V_{UV} and DQ is stable at either logic level for t_{SLEEP}. A value of 0 disables transitions to Sleep mode in an undervoltage condition.

PMOD—Power Mode Enable. A value of 1 allows the DS2784 to enter Sleep mode when DQ is low for t_{SLEEP}. A value of 0 disables DQ related transitions to Sleep mode.

RNAOP—Read Net Address Op Code. A value of 0 selects 33h as the op code value for the Read Net Address command. A value of 1 selects 39h as the Read Net Address opcode value.

0—Reserved bit, must be programmed to 0 for proper operation.

PSPIO—Power-Switch PIO Enable. A value of 1 enables the PIO pin as a power-switch input. A value of 0 disables the power-switch input function on PIO pin. This control is independent of the PSDQ state.

PSDQ—Power-Switch DQ Enable. A value of 1 enables the DQ pin as a power-switch input. A value of 0 disables the power-switch input function on DQ pin. This control is independent of the PSPIO state.

X—Reserved Bit.

Li+ PROTECTION CIRCUITRY

During Active mode, the DS2784 constantly monitors SNS, V_{IN}, and V_{PLS} to protect the battery from overvoltage (overcharge), undervoltage (overdischarge), and excessive charge and discharge currents (overcurrent, short circuit). Table 1 summarizes the conditions that activate the protection circuit, the response of the DS2784, and the thresholds that release the DS2784 from a protection state.

Table 1. Li+ Protection Conditions and DS2784 Responses

CONDITION	ACTIVATION			RELEASE THRESHOLD
	THRESHOLD	DELAY	RESPONSE(2)	
Overvoltage	$V_{IN} > V_{OV}$	t_{OVD}	CC Off	$V_{IN} < V_{CE}$ or ($V_{SNS} > 1.2mV$ and $V_{IN} < V_{OV}$)
Undervoltage	$V_{IN} < V_{UV}$	t_{UVD}	CC Off, DC Off, Sleep Mode	$V_{PLS} > V_{IN}$ (3) (charger connected)
Overcurrent, Charge	$V_{SNS} < V_{COC}$	t_{OCD}	CC Off, DC Off	$V_{PLS} < V_{DD} - V_{TP}$ (4) (charger removed)
Overcurrent, Discharge	$V_{SNS} > V_{DOC}$	t_{OCD}	DC Off	$V_{PLS} > V_{DD} - V_{TP}$ (5) (load removed)
Short Circuit	$V_{SNS} > V_{SC}$	t_{SCD}	DC Off	$V_{PLS} > V_{DD} - V_{TP}$ (5) (load removed)

Note 1: All voltages are with respect to V_{SS}.

Note 2: CC pin driven to V_{OLCC} (V_{DD}) for CC off response. DC pin driven to V_{OLDC} (V_{SS}) for DC off response.

Note 3: If $V_{IN} < V_{UV}$ when charger connection is detected, release is delayed until $V_{IN} \geq V_{UV}$. The recovery charge path provides an internal current limit (I_{RC}) to safely charge the battery.

Note 4: With test current I_{TST} flowing from PLS to V_{SS} (pulldown on PLS) enabled.

Note 5: With test current I_{TST} flowing from V_{DD} to PLS (pullup on PLS).

Overvoltage. If the voltage on V_{IN} exceeds the overvoltage threshold (V_{OV}) for a period longer than overvoltage delay (t_{OVD}), the CC pin is driven low to shut off the external-charge FET, and the OV flag in the protection register is set. The DC output remains high during overvoltage to allow discharging. When V_{IN} falls below the charge enable threshold, V_{CE}, the DS2784 turns the charge FET on by driving CC high. The DS2784 drives CC high before $V_{IN} < V_{CE}$ if a discharge condition persists with $V_{SNS} \geq 1.2mV$ and $V_{IN} < V_{OV}$.

Undervoltage. If V_{IN} drops below the undervoltage threshold (V_{UV}) for a period longer than undervoltage delay (t_{UVD}), the DS2784 shuts off the charge and discharge FETs and sets the UV flag in the protection register. If UVEN is set, the DS2784 also enters Sleep mode. The DS2784 provides a current-limited recovery charge path (I_{RC}) from PLS to V_{DD} to gently charge severely depleted cells. The recovery charge path is enabled when $0 \leq V_{DD} < (V_{OV} - 100mV)$. Once V_{DD} reaches 2.45V (typ), the DS2784 returns to normal operation and begins monitoring V_{IN}. Once $V_{IN} > V_{UV}$, the DS2784 transitions from Sleep to Active mode and the CC and DC outputs are driven high to turn on the charge and discharge FETs.

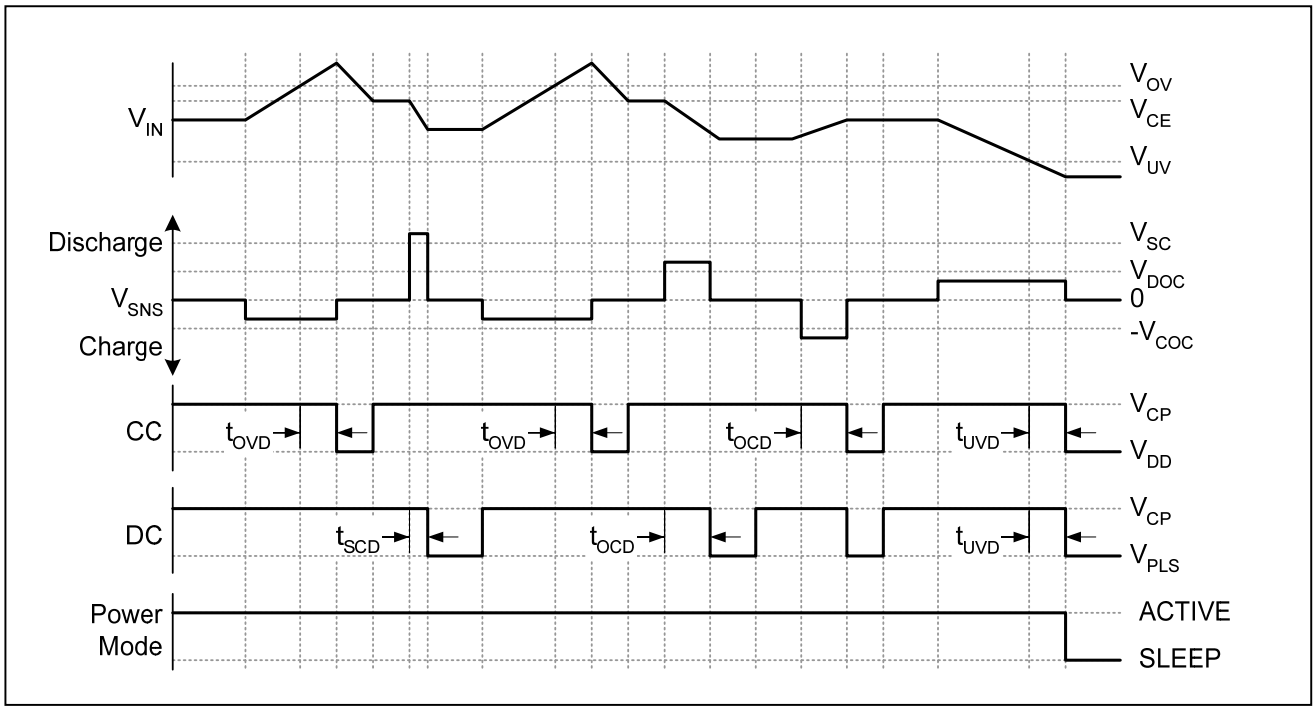
Overcurrent, Charge Direction (COC). Charge current develops a negative voltage on V_{SNS} with respect to V_{SS}. If V_{SNS} is less than the charge overcurrent threshold (V_{COC}) for a period longer than overcurrent delay (t_{OCD}), the

DS2784 shuts off both external FETs and sets the COC flag in the protection register. The charge current path is not re-established until the voltage on the PLS pin drops below V_{DD} - V_{TP}. The DS2784 provides a pulldown current (I_{TST}) from PLS to V_{SS} to pull PLS down in order to detect the removal of the offending charge current source.

Overcurrent, Discharge Direction (DOC). Discharge current develops a positive voltage on V_{SNS} with respect to V_{SS}. If V_{SNS} exceeds the discharge overcurrent threshold (V_{DOC}) for a period longer than t_{OCD}, the DS2784 shuts off the external discharge FET and sets the DOC flag in the protection register. The discharge current path is not re-established until the voltage on PLS rises above V_{DD} - V_{TP}. The DS2784 provides a test current (I_{TST}) from V_{DD} to PLS to pull PLS up in order to detect the removal of the offending low-impedance load.

Short Circuit. If V_{SNS} exceeds short-circuit threshold V_{SC} for a period longer than short-circuit delay (t_{SCD}), the DS2784 shuts off the external discharge FET and sets the DOC flag in the protection register. The discharge current path is not re-established until the voltage on PLS rises above V_{DD} - V_{TP}. The DS2784 provides a test current of value (I_{TST}) from V_{DD} to PLS to pull PLS up in order to detect the removal of the short circuit.

Figure 2. Li+ Protection Circuitry Example Waveforms



Summary. All the protection conditions previously described are logic ANDed to affect the CC and DC outputs.

CC = ($\overline{\text{Overvoltage}}$) AND ($\overline{\text{Undervoltage}}$) AND ($\overline{\text{Overcurrent}}$, Charge Direction)
AND (Protection Register Bit CE)

DC = ($\overline{\text{Undervoltage}}$) AND ($\overline{\text{Overcurrent}}$, Either Direction) AND ($\overline{\text{Short Circuit}}$)
AND (Protection Register Bit DE)

PROTECTION REGISTER FORMAT

The protection register reports events detected by the Li+ safety circuit on bits 2 to 7. Bits 0 and 1 are used to disable the charge and discharge FET gate drivers. Bits 2 to 7 are set by internal hardware only. Bits 2 and 3 are cleared by hardware only. Bits 4 to 7 are cleared by writing the register with a 0 in the bit position of interest. Writing

a 1 to bits 4 to 7 has no effect on the register. Bits 0 and 1 are set on power-up and a transition from Sleep to Active modes. While in Active mode, these bits can be cleared to disable the FET gate drive of either or both FETs. Setting these bits only turns on the FETs if there are no protection faults.

ADDRESS 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OV	UV	COC	DOC	CC	DC	CE	DE

OV—Overvoltage Flag. OV is set to indicate that an overvoltage condition has been detected. The voltage on V_{IN} has persisted above the V_{OV} threshold for t_{OV}. OV remains set until written to a 0 or cleared by a power-on reset or transition to Sleep mode.

UV—Undervoltage Flag. UV is a read-only mirror of the UVF flag located in the status register. UVF is set to indicate that $V_{IN} < V_{UV}$. The UVF bit must be written to 0 to clear UV and UVF.

COC—Charge Overcurrent Flag. COC is set to indicate that an overcurrent condition has occurred during a charge. The sense-resistor voltage has persisted above the V_{COC} threshold for t_{OC}. COC remains set until written to a 0, cleared by a power-on reset, or transition to Sleep mode.

DOC—Discharge Overcurrent Flag. DOC is set to indicate that an overcurrent condition has occurred during a discharge. The sense-resistor voltage has persisted above the V_{DOC} threshold for t_{OC}. DOC remains set until written to a 0, cleared by a power-on reset, or transition to Sleep mode.

CC—Charge Control Flag. CC indicates the logic state of the CC pin driver. CC flag is set to indicate CC high. CC flag is cleared to indicate CC low. CC flag is read only.

DC—Discharge Control Flag. DC indicates the logic state of the DC pin driver. DC flag is set to indicate DC high. DC flag is cleared to indicate DC low. DC flag is read only.

CE—Charge Enable Bit. CE must be set to allow the CC pin to drive the charge FET to the on state. CE acts as an enable input to the safety circuit. If all safety conditions are met AND CE is set, the CC pin drives to V_{CP}. If CE is cleared, the CC pin is driven low to disable the charge FET.

DE—Discharge Enable Bit. DE must be set to allow the DC pin to drive the discharge FET to the on state. DE acts as an enable input to the safety circuit. If all safety conditions are met AND DE is set, the DC pin drives to V_{CP}. If DE is cleared, the DC pin is driven low to disable the charge FET.

PROTECTOR THRESHOLD REGISTER FORMAT

The 8-bit threshold register consists of bit fields for setting the overvoltage threshold, charge overcurrent threshold, discharge overcurrent threshold, and short-circuit threshold for the protection circuit.

ADDRESS 7Fh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VOV4	VOV3	VOV2	VOV1	VOV0	SC0	OC1	OC0

Table 2. VOV Threshold

VOV BIT FIELD	V_{OV}	VOV BIT FIELD	V_{OV}
0 0 0 0 0	4.248	1 0 0 0 0	4.404
0 0 0 0 1	4.258	1 0 0 0 1	4.414
0 0 0 1 0	4.268	1 0 0 1 0	4.424
0 0 0 1 1	4.277	1 0 0 1 1	4.434
0 0 1 0 0	4.287	1 0 1 0 0	4.443
0 0 1 0 1	4.297	1 0 1 0 1	4.453
0 0 1 1 0	4.307	1 0 1 1 0	4.463
0 0 1 1 1	4.316	1 0 1 1 1	4.473
0 1 0 0 0	4.326	1 1 0 0 0	4.482
0 1 0 0 1	4.336	1 1 0 0 1	4.492
0 1 0 1 0	4.346	1 1 0 1 0	4.502
0 1 0 1 1	4.356	1 1 0 1 1	4.512
0 1 1 0 0	4.365	1 1 1 0 0	4.522
0 1 1 0 1	4.375	1 1 1 0 1	4.531
0 1 1 1 0	4.385	1 1 1 1 0	4.541
0 1 1 1 1	4.395	1 1 1 1 1	4.551

Table 3. COC, DOC Threshold

OC[1:0] BIT FIELD	V_{COC} (mV)	V_{DOC} (mV)
0 0	-23.5	35.5
0 1	-36	48
1 0	-48	72
1 1	-72	96

Table 4. SC Threshold

SC0 BIT FIELD	V_{SC} (mV)
0	150
1	300

VOLTAGE MEASUREMENT

Battery voltage is measured every 440ms on the V_{IN} pin with respect to V_{SS}. Measurements have a 0 to 4.99V range and a 4.88mV resolution. The value is stored in the voltage register in two's complement form and is updated every 440ms. Voltages above the maximum register value are reported at the maximum value; voltages below the minimum register value are reported at the minimum value.

VOLTAGE REGISTER FORMAT

MSB—ADDRESS 0Ch

S	2^9	2^8	2^7	2^6	2^5	2^4	2^3

MSb LSb

LSB—ADDRESS 0Dh

2^2	2^1	2^0	X	X	X	X	X

MSb LSb

"S": Sign Bit(s), "X": Reserved

Units: 4.886mV

TEMPERATURE MEASUREMENT

The DS2784 uses an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 440ms and placed in the temperature register in two's complement form.

TEMPERATURE REGISTER FORMAT

MSB—ADDRESS 0Ah

S	2^9	2^8	2^7	2^6	2^5	2^4	2^3
MSb							LSb

LSB—ADDRESS 0Bh

2^2	2^1	2^0	X	X	X	X	X
MSb							LSb

"S": Sign Bit(s), "X": Reserved

Units: 0.125°C

Note: Temperature and battery voltage (V_{IN}) are measured using the same ADC. Therefore, measurements are a 220ms average updated every 440ms.

CURRENT MEASUREMENT

The DS2784 continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}. The voltage-sense range between SNS and V_{SS} is ±51.2mV. The input linearly converts peak-signal amplitudes up to 102.4mV as long as the continuous signal level (average over the conversion cycle period) does not exceed ±51.2mV. The ADC samples the input differentially at 18.6kHz and updates the current register at the completion of each conversion cycle (3.52s). Charge currents above the maximum register value are reported as 7FFFh. Discharge currents below the minimum register value are reported as 8000h.

CURRENT REGISTER FORMAT

MSB—ADDRESS 0Eh

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
MSb							LSb

LSB—ADDRESS 0Fh

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb

"S": Sign Bit(s)

Units: $1.5625\mu V/R_{SNS}$

The average current register reports an average current level over the preceding 28s. The register value is updated every 28s in two's complement form, and represents an average of the eight preceding current register values.

AVERAGE CURRENT REGISTER FORMAT

MSB—ADDRESS 08h

S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
MSb							LSb

LSB—ADDRESS 09h

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb

"S": Sign Bit(s)

Units: $1.5625\mu V/R_{SNS}$

CURRENT OFFSET CORRECTION

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the sense-resistor signal. A maximum error of 1/1024 in the accumulated current register (ACR) is possible; however, to reduce the error, the current

measurement made just prior to the offset conversion is retained in the current register and is substituted for the dropped current measurement in the current accumulation process. Therefore, the accumulated current error due to offset correction is typically much less than 1/1024.

CURRENT OFFSET BIAS

The current offset bias (COB) value allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus COB is displayed as the current measurement result in the current register, and is used for current accumulation. COB can be used to correct for a static offset error, or can be used to intentionally skew the current results and, therefore, the current accumulation.

Read and write access is allowed to COB. Whenever the COB is written, the new value is applied to all subsequent current measurements. COB can be programmed in 1.56µV steps to any value between +198.1µV and -199.7µV. The COB value is stored as a two's complement value in EEPROM. The COB is loaded on power-up from EEPROM memory. The factory default value is 00h.

The difference between the CAB and COB is that the CAB is not subject to current blanking. Offset currents between 100µV and -25µV are not accumulated if the offset is made by the COB. Offset currents between 100µV and -25µV are accumulated if they are made by the CAB.

CURRENT OFFSET BIAS REGISTER FORMAT

ADDRESS 7Bh

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb

"S": Sign Bit(s)

Units: 1.56µV/R_{SNS}

CURRENT BLANKING

The current blanking feature modifies current measurement result prior to being accumulated in the ACR. Current blanking occurs conditionally when a current measurement (raw current + COBR) falls in one of two defined ranges. The first range prevents charge currents less than 100µV from being accumulated. The second range prevents discharge currents less than 25µV in magnitude from being accumulated. Charge current blanking is always performed; however, discharge current blanking must be enabled by setting the NBEN bit in the control register. See the register description for additional information.

CURRENT MEASUREMENT CALIBRATION

The DS2784's current measurement gain can be adjusted through the RSGAIN register, which is factory calibrated to meet the data sheet-specified accuracy. RSGAIN is user accessible and can be reprogrammed after module or pack manufacture to improve the current measurement accuracy. Adjusting RSGAIN can correct for variation in an external sense resistor's nominal value, and allows the use of low-cost, nonprecision, current-sense resistors. RSGAIN is an 11-bit value stored in 2 bytes of the parameter EEPROM memory block. The RSGAIN value adjusts the gain from 0 to 1.999 in steps of 0.001 (precisely 2^{-10}). The user must program RSGAIN cautiously to ensure accurate current measurement. When shipped from the factory, the gain calibration value is stored in two separate locations in the parameter EEPROM block: RSGAIN, which is reprogrammable, and FRSGAIN, which is read only. RSGAIN determines the gain used in the current measurement. The FRSGAIN value is provided to preserve the factory calibration value only and is not used to calibrate the current measurement. The 16-bit FRSGAIN value is readable from addresses B0h and B1h.

CURRENT MEASUREMENT GAIN REGISTER FORMAT

MSB—ADDRESS 78h

X	X	X	X	X	2^{10}	2^9	2^8

MSb LSb

LSB—ADDRESS 79h

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

Units: 2^{-10}

SENSE RESISTOR TEMPERATURE COMPENSATION

The DS2784 can of temperature compensate the current-sense resistor to correct for variation in a sense resistor's value overtemperature. The DS2784 is factory programmed with the sense-resistor temperature coefficient, RSTC, set to zero, which turns off the temperature compensation function. RSTC is user accessible and can be reprogrammed after module or pack manufacture to improve the current accuracy when using a high-temperature coefficient current-sense resistor. RSTC is an 8-bit value stored in the parameter EEPROM memory block. The RSTC value sets the temperature coefficient from 0 to +7782ppm/ºC in steps of 30.5ppm/ºC. The user must program RSTC cautiously to ensure accurate current measurement.

Temperature compensation adjustments are made when the temperature register crosses 0.5°C boundaries. The temperature compensation is most effective with the resistor placed as close as possible to the V_{SS} terminal. This optimizes thermal coupling of the resistor to the on-chip temperature sensor.

SENSE RESISTOR TEMPERATURE COMPENSATION REGISTER FORMAT

ADDRESS 7Ah

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

Units: 30.5ppm/ºC

CURRENT ACCUMULATION

Current measurements are internally summed, or accumulated, at the completion of each conversion period and the results are stored in the ACR. The accuracy of the ACR is dependent on both the current measurement and the conversion time base. The ACR has a range of 0 to 409.6mVh with an LSb of 6.25μVh. Additional registers hold fractional results of each accumulation to avoid truncation errors. The fractional result bits are not user accessible. Accumulation of charge current above the maximum register value is reported at the maximum value; conversely, accumulation of discharge current below the minimum register value is reported at the minimum value.

Charge currents (positive current register values) less than 100μV are not accumulated in order to mask the effect of accumulating small positive offset errors over long periods. This limits the minimum charge current, for coulomb-counting purposes, to 5mA for R_{SNS} = 0.020Ω and 20mA for R_{SNS} = 0.005Ω.

Read and write access is allowed to the ACR. The ACR must be written MSB first then LSB. Whenever the ACR is written, the fractional accumulation result bits are cleared. The write must be completed in 3.5s (one ACR update period). A write to the ACR forces the ADC to perform an offset correction conversion and update the internal offset correction factor. The current measurement and accumulation begin with the second conversion following a write to the ACR.

The ACR value is backed up to EEPROM in case of power loss. The ACR value is recovered from EEPROM on power-up. See Table 8 for specific address location and backup frequency.

ACCUMULATED CURRENT REGISTER FORMAT

MSB—ADDRESS 10h

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
MSb							LSb

LSB—ADDRESS 11h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

Units: 6.25µVh/R_{SNS}

Table 5. Resolution and Range vs. Sense Resistor

	V_{SS} - V_{SNS}	R_{SNS}			
		20mΩ	15mΩ	10mΩ	5mΩ
Current Resolution	1.5625µV	78.13µA	104.2µA	156.3µA	312.5µA
Current Range	±51.2mV	±2.56A	±3.41A	±5.12A	±10.24A
ACR Resolution	6.25µVh	312.5µAh	416.7µAh	625µAh	1.250mAh
ACR Range	409.6mVh	20.48Ah	27.31Ah	40.96Ah	81.92Ah

ACCUMULATION BIAS

In some designs a systematic error or an application preference requires the application of an arbitrary bias to the current accumulation process. The current accumulation bias register (CAB) allows a user-programmed constant positive or negative polarity bias to be included in the current accumulation process. The value in CAB can be used to estimate battery currents that do not flow through the sense resistor, estimate battery self-discharge or estimate current levels below the current measurement resolution. The user programmed two's complement value, with bit weighting the same as the current register, is added to the ACR once per current conversion cycle. The CAB is loaded on power-up from EEPROM memory.

The difference between the CAB and COB is that the CAB is not subject to current blanking. Offset currents between 100µV and -25µV are not accumulated if the offset is made by the COB. Offset currents between 100µV and -25µV are accumulated if they are made by the CAB.

CURRENT ACCUMULATION BIAS REGISTER FORMAT

ADDRESS 61h

S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

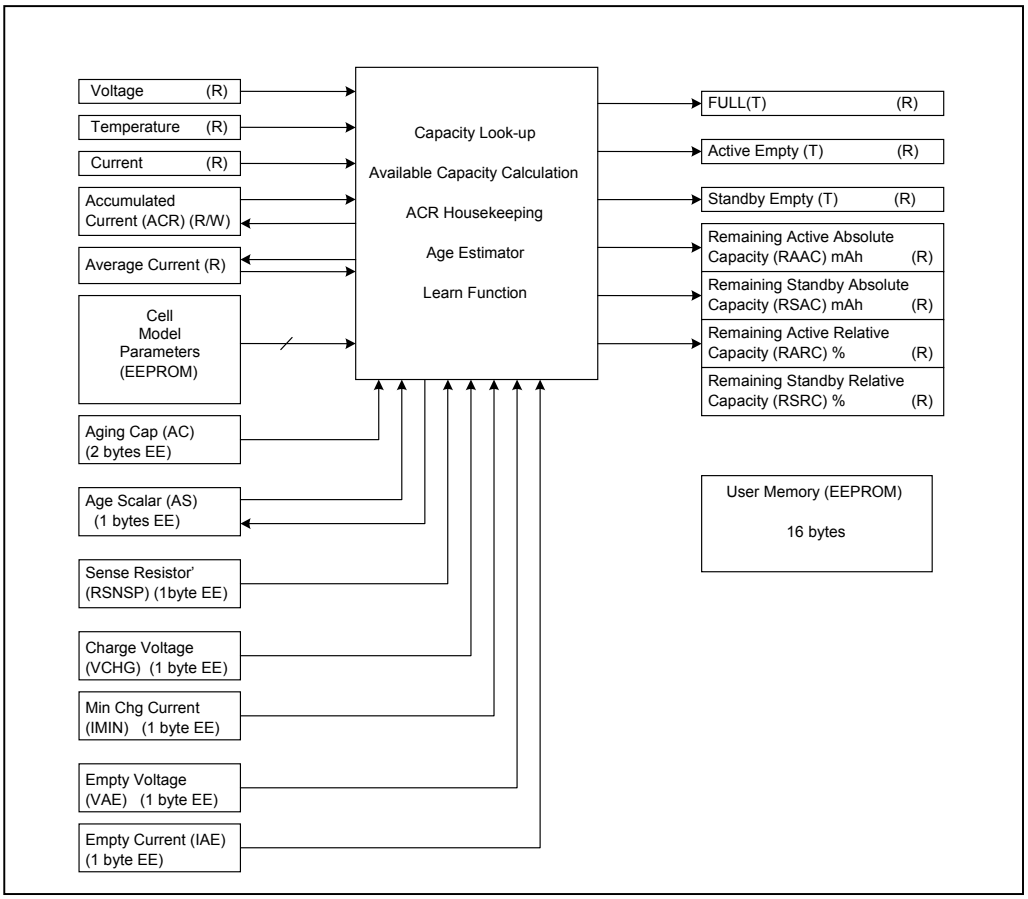
"S": Sign Bit

Units: 1.5625µV/R_{SNS}

CAPACITY ESTIMATION ALGORITHM

Remaining capacity estimation uses real-time measured values, stored parameters describing the cell characteristics, and application operating limits. Figure 2 describes the algorithm inputs and outputs.

Figure 2. Top-Level Algorithm Diagram

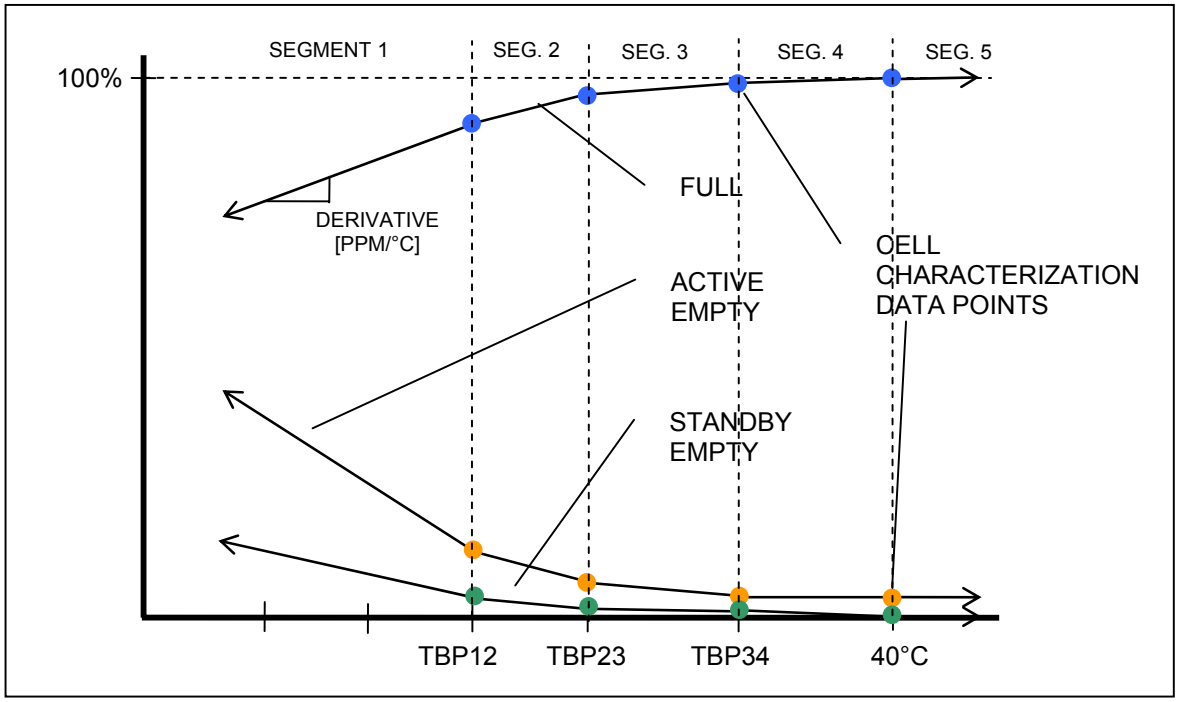


MODELING CELL CHARACTERISTICS

To achieve reasonable accuracy in estimating remaining capacity, the cell performance characteristics overtemperature, load current, and charge-termination point must be considered. Since the behavior of Li+ cells is nonlinear, these characteristics must be included in the capacity estimation to achieve an acceptable level of accuracy in the capacity estimation. The FuelPack™ method used in the DS2784 is described in general in Application Note 131: *Lithium-Ion Cell Fuel Gauging with Dallas Semiconductor Battery Monitor ICs.* To facilitate efficient implementation in hardware, a modified version of the method outlined in AN131 is used to store cell characteristics in the DS2784. Full and empty points are retrieved in a lookup process which retraces a piece-wise linear model consisting of three model curves named full, active empty, and standby empty. Each model curve is constructed with 5-line segments, numbered 1 through 5. Above 40°C, the segment 5 model curves extend infinitely with zero slope, approximating the nearly flat change in capacity of Li+ cells at temperatures above 40°C. Segment 4 of each model curves originates at +40C on its upper end and extends downward in temperature to the junction with segment 3. Segment 3 joins with segment 2, which in turn joins with segment 1. Segment 1 of each model curve extends from the junction with segment 2 to infinitely colder temperatures. The three junctions or breakpoints that join the segments (labeled TBP12, TBP23, and TBP34 in Figure 3) are programmable in 1°C increments from -128°C to +40°C. The slope or derivative for segments 1, 2, 3, and 4 are also programmable over a range of 0 to 15,555ppm, in steps of 61ppm.

FuelPack is a trademark of Dallas Semiconductor, a wholly owned subsidiary of Maxim Integrated Products, Inc.

Figure 3. Cell Model Example Diagram



Full—The full curve defines how the full point of a given cell varies over temperature for a given charge termination. The application's charge termination method should be used to determine the table values. The DS2784 reconstructs the full line from the cell characteristic table to determine the full capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Active Empty—The active-empty curve defines the variation of the active-empty point over temperature. The active-empty point is defined as the minimum voltage required for system operation at a discharge rate based on a high-level load current (one that is sustained during a high-power operating mode). This load current is programmed as the active-empty current (IAE), and should be a 3.5s average value to correspond to values read from the current register. The specified minimum voltage, or active empty voltage (VAE), should be a 220ms average value to correspond to the values read from the voltage register. The DS2784 reconstructs the active empty line from the cell characteristic table to determine the active empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Standby Empty—The standby-empty curve defines the variation of the standby-empty point over temperature. The standby-empty point is defined as the minimum voltage required for standby operation at a discharge rate dictated by the application standby current. In typical handheld applications, standby empty represents the point that the battery can no longer support DRAM refresh and thus the standby voltage is set by the minimum DRAM voltage-supply requirements. In other applications, standby empty can represent the point that the battery can no longer support a subset of the full application operation, such as games or organizer functions. The standby load current and voltage are used for determining the cell characteristics but are not programmed into the DS2784. The DS2784 reconstructs the standby-empty line from the cell characteristic table to determine the standby-empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

CELL MODEL CONSTRUCTION

The model is constructed with all points normalized to the fully charged state at +40°C. All values are stored in the cell parameter EEPROM block. The +40°C full value is stored in µVhr with an LSB of 6.25µVhr. The +40°C active empty value is stored as a percentage of +40°C full with a resolution of 2^{-10}. Standby empty at +40°C is, by definition, zero and, therefore, no storage is required. The slopes (derivatives) of the 4 segments for each

model curve are stored in the cell parameter EEPROM block as ppm/°C. The breakpoint temperatures of each segment are stored there also (see Application Note 3584: *Storing Battery Fuel Gauge Parameters in DS2780* for more details on how values are stored). An example of data stored in this manner is shown in Table 6.

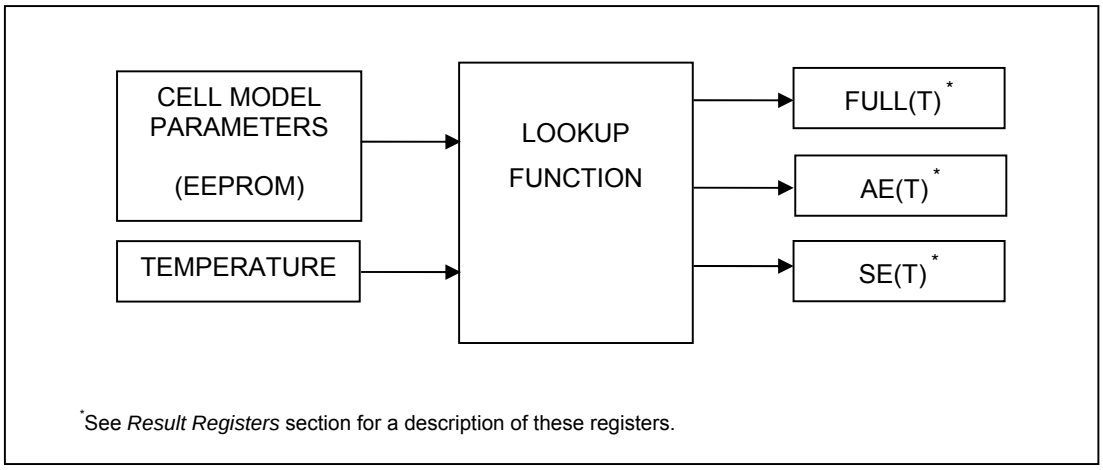
Table 6. Example Cell Characterization Table (Normalized to +40°C)

Manufacturer's Rated Cell Capacity: 1000mAh	
Charge Voltage: 4.2V	**Termination Current: 50mA**
Active Empty (V): 3.0V	**Active Empty (I): 300mA**
Sense Resistor: 0.020Ω	

	TBP12	**TBP23**	**TBP34**
Segment Breakpoints	**-12°C**	**0°C**	**18°C**

	+40°C Nominal (mAh)	**Seg. 1 ppm/°C**	**Seg. 2 ppm/°C**	**Seg. 3 ppm/°C**	**Seg. 4 ppm/°C**
Full	**1051**	**3601**	**3113**	**1163**	**854**
Active Empty		**2380**	**1099**	**671**	**305**
Standby Empty		**1404**	**427**	**244**	**183**

Figure 4. Lookup Function Diagram



*See *Result Registers* section for a description of these registers.

APPLICATION PARAMETERS

In addition to cell model characteristics, several application parameters are needed to detect the full and empty points, as well as calculate results in mAh units.

Sense Resistor Prime (R_{SNSP}[1/Ω])—R_{SNSP} stores the value of the sense resistor for use in computing the absolute capacity results. The resistance is stored as a 1-byte conductance value with units of mhos (1/Ω). R_{SNSP} supports resistor values of 1Ω to 3.922mΩ. R_{SNS} is located in the parameter EEPROM block.

$$R_{SNSP} = 1/R_{SNS} \quad \text{(units of mhos; 1/}\Omega\text{)}$$

Charge Voltage (VCHG)—VCHG stores the charge voltage threshold used to detect a fully charged state. The voltage is stored as a 1-byte value with units of 19.5mV and can range from 0V to 4.978V. VCHG should be set marginally less than the cell voltage at the end of the charge cycle to ensure reliable charge termination detection. VCHG is located in the parameter EEPROM block.

Minimum Charge Current (IMIN)—IMIN stores the charge current threshold used to detect a fully charged state. It is stored as a 1-byte value with units of 50μV (IMIN x R_{SNS}) and can range from 0 to 12.75mV. Assuming R_{SNS} = 20mΩ, IMIN can be programmed from 0mA to 637.5mA in 2.5mA steps. IMIN should be set marginally greater than the charge current at the end of the charge cycle to ensure reliable charge termination detection. IMIN is located in the parameter EEPROM block.

Active Empty Voltage (VAE)—VAE stores the voltage threshold used to detect the active empty point. The value is stored in 1-byte with units of 19.5mV and can range from 0V to 4.978V. VAE is located in the parameter EEPROM block. See the *Cell Characteristics* section for more information.

Active Empty Current (IAE)—IAE stores the discharge current threshold used to detect the active empty point. The unsigned value represents the magnitude of the discharge current and is stored in 1-byte with units of 200μV and can range from 0 to 51.2mV. Assuming R_{SNS} = 20mΩ, IAE can be programmed from 0mA to 2550mA in 10mA steps. IAE is located in the Parameter EEPROM block. See the *Cell Model Construction* section for more information.

Aging Capacity (AC)—AC stores the rated cell capacity, which is used to estimate the decrease in battery capacity that occurs during normal use. The value is stored in 2 bytes in the same units as the ACR (6.25μVh). When set to the manufacturer's rated cell capacity the aging estimation rate is approximately 2.4% per 100 cycles of equivalent full capacity discharges. Partial discharge cycles are added to form equivalent full capacity discharges. The default aging estimation results in 88% capacity after 500 equivalent cycles. The aging estimation rate can be adjusted by setting the AC to a value other than the cell manufacturer's rating. Setting AC to a lower value, accelerates the aging estimation rate. Setting AC to a higher value, retards the aging estimation rate. The AC is located in the parameter EEPROM block.

Age Scalar (AS)—AS adjusts the cell capacity estimation results downward to compensate for aging. The AS is a 1-byte value that has a range of 49.2% to 100%. The LSB is weighted at 0.78% (precisely 2^{-7}). A value of 100% (128 decimal or 80h) represents an unaged battery. A value of 95% is recommended as the starting AS value at the time of pack manufacture to allow the learning of a larger capacity on batteries that have an initial capacity greater than the rated cell capacity programmed in the cell characteristic table. The AS is modified by aging estimation introduced under aging capacity and by the capacity-learn function. The host system has read and write access to the AS, however caution should exercised when writing it to ensure that the cumulative aging estimate is not overwritten with an incorrect value. The AS is automatically saved to EEPROM (see Table 7 for details). The EEPROM value is recalled on power-up.

Full capacity estimation based on the learn function is more accurate than the cycle-count-based estimation. The learn function reflects the current performance of the cell. Cycle count based estimation is an approximation derived from the manufacturer's recommendation for a typical cell. Batteries are typically considered worn-out when the full capacity reaches 80% of the rated capacity, therefore, the AS value is not required to range to 0%. It is clamped to 50% (64d or 40h). If a value of 50% is read from the AS, the host should prompt the user to initiate a learning cycle.

CAPACITY ESTIMATION OPERATION

Aging Estimation

As discussed above, the AS register value is adjusted occasionally based on cumulative discharge. As the ACR register decrements during each discharge cycle, an internal counter is incremented until equal to 32 times the AC. The AS is then decremented by one, resulting in a decrease of the scaled full battery capacity by 0.78% (approximately 2.4% per 100 cycles). See the AC register description above for recommendations on customizing the age-estimation rate.

Learn Function

Since Li+ cells exhibit charge efficiencies near unity, the charge delivered to a Li+ cell from a known empty point to a known full point is a dependable measure of the cell capacity. A continuous charge from empty to full results in a learn cycle. First, the active empty point must be detected. The learn flag (LEARNF) is set at this point. Then, once charging starts, the charge must continue uninterrupted until the battery is charged to full. Upon detecting full,

LEARNF is cleared, the charge to full (CHGTF) flag is set, and the age scalar (AS) is adjusted according to the learned capacity of the cell.

ACR Housekeeping
The ACR value is adjusted occasionally to maintain the coulomb count within the model curve boundaries. When the battery is charged to full (CHGTF set), the ACR is set equal to the age scaled full lookup value at the present temperature. If a learn cycle is in progress, correction of the ACR value occurs after the age scalar (AS) is updated.

When an empty condition is detected (LEARNF and/or AEF set), the ACR adjustment is conditional:
- If the AEF is set and the LEARNF is not set, then the active-empty point was not detected. The battery is likely below the active-empty capacity of the model. The ACR is set to the active-empty model value at present temp only if it is greater than the active-empty model value at present temp.
- If the AEF is set, the LEARNF is not set, and the ACR is below the active-empty model value at present temp the ACR is NOT updated.
- If the LEARNF is set, then the battery is at the active-empty point and the ACR is set to the active-empty model value.

Full Detect
Full detection occurs when the voltage (V) readings remain continuously above the charge voltage (VCHG) threshold for the duration of two average current (IAVG) readings, and both IAVG readings are below terminating current (IMIN). The two consecutive IAVG readings must also be positive and nonzero (> 16 LSB). This ensures that removing the battery from the charger does not result in a false detection of full. Full detect sets the charge to full (CHGTF) bit in the status register.

Active-Empty Point Detect
Active-empty point detection occurs when the voltage register drops below the VAE threshold AND the two previous current readings are above IAE. This captures the event of the battery reaching the active-empty point. Note that the two previous current readings must be negative and greater in magnitude than IAE, that is, a larger discharge current than specified by the IAE threshold. Qualifying the voltage level with the discharge rate ensures that the active-empty point is not detected at loads much lighter than those used to construct the model. Also, the active-empty point must not be detected when a deep discharge at a very light load is followed by a load greater than IAE. Either case would cause a learn cycle on the following charge to include part of the standby capacity in the measurement of the active capacity. Active-empty point detection sets the learn flag (LEARNF) bit in the status register. *Do not confuse the active-empty point with the active-empty flag. The active-empty flag is set only when the VAE threshold is passed.*

STATUS REGISTER FORMAT
The status register contains bits that report the device status. All bits are set internally. The CHGTF, AEF, SEF, and LEARNF bits are read only. The UVF and PORF bits can be cleared by writing a zero to the bit locations.

ADDRESS 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CHGTF	AEF	SEF	LEARNF	X	UVF	PORF	X

CHGTF—Charge-Termination Flag. CHGTF is set to indicate that the voltage and average current register values have persisted above the VCHG and below the IMIN thresholds sufficiently long to detect a fully charged condition. CHGF is cleared when RARC is less than 90%. CHGF is read only.

AEF—Active-Empty Flag. AEF is set to indicate that the battery is at or below the active-empty point. AEF is set when the voltage register value is less than the VAE threshold. AEF is cleared when RARC is greater than 5%. AEF is read only.

SEF—Standby-Empty Flag. SEF is set to indicate RSRC is less than 10%. SEF is cleared when RSRC is greater than 15%. SEF is read only.

LEARNF—Learn Flag. LEARNF indicates that the current charge cycle can be used to learn the battery capacity. LEARNF is set when the active-empty point is detected. This occurs when the voltage register value drops below the VAE threshold AND the two previous current register values were negative and greater in magnitude than the IAE threshold. See the *Active-Empty Point Detect* section for additional information. LEARNF is cleared when any of the following occur:

1) Learn cycle completes (CHGTF set).
2) Current register value becomes negative indicating discharge current flow.
3) ACR = 0
4) ACR value is written or recalled from EEPROM.
5) Sleep mode is entered.

LEARNF is read only.

UVF—Undervoltage Flag. UVF is set to indicate that the voltage measurement of the V_{IN} pin is less than V_{UV}, and must be written to a 0 to allow subsequent undervoltage events to be reported. UVF is not cleared internally. Writing UVF to 0 is effective only when V_{IN} is greater or equal to V_{UV}, otherwise, UV remains set due to the persistent undervoltage condition. UVF is set on power-up.

PORF—Power-On Reset Flag. PORF is set to indicate initial power-up. PORF is not cleared internally. The user must write this flag value to a 0 to use it to indicate subsequent power-up events. If PORF indicates a power-on reset, the ACR could be misaligned with the actual battery state of charge. The system can request a charge to full to synchronize the ACR with the battery charge state. PORF is read/write-to-zero.

X—Reserved Bits.

RESULT REGISTERS

The DS2784 processes measurement and cell characteristics on a 3.5s interval and yields seven result registers. The result registers are sufficient for direct display to the user in most applications. The host system can produce customized values for system use or user display by combining measurement, result and user EEPROM values.

FULL(T) [ ]—The full capacity of the battery at the present temperature is reported normalized to the 40°C full value. This 15-bit value reflects the cell model Full value at the given temperature. FULL(T) reports values between 100% and 50% with a resolution of 61ppm (precisely 2^{-14}). The register is clamped to a maximum value of 100% even though the register format permits values greater than 100%.

Active Empty, AE(T) [ ]—The active-empty capacity of the battery at the present temperature is reported normalized to the 40°C full value. This 13-bit value reflects the cell model active-empty value at the given temperature. AE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

Standby Empty, SE(T) [ ]—The standby-empty capacity of the battery at the present temperature is reported normalized to the 40°C full value. This 13-bit value reflects the cell model standby-empty value at the current temperature. SE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

Remaining Active Absolute Capacity (RAAC) [mAh]—RAAC reports the remaining battery capacity available under the current temperature conditions to the active-empty point in absolute units of milliamp-hours (mAhr). RAAC is 16 bits.

MSB—ADDRESS 02h

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
MSb							LSb

LSB—ADDRESS 03h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

Units: 1.6mAhr

Remaining Standby Absolute Capacity (RSAC) [mAh]—RSAC reports the remaining battery capacity available under the current temperature conditions to the standby-empty point capacity in absolute units of milliamp-hours (mAhr). RSAC is 16 bits.

MSB—ADDRESS 04h

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
MSb							LSb

LSB—ADDRESS 05h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

Units: 1.6mAhr

Remaining Active Relative Capacity (RARC) [%]—RARC reports the remaining battery capacity available under the current temperature conditions to the active-empty point in relative units of percent. RARC is 8 bits.

ADDRESS 06h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

Units: 1%

Remaining Standby Relative Capacity (RSRC) [%]—RSRC reports the remaining battery capacity available under the current temperature conditions to the standby-empty point capacity in relative units of percent. RSRC is 8 bits.

ADDRESS 07h

2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MSb							LSb

Units: 1%

Calculation of Results

RAAC [mAh] = (ACR[mVh] - AE(T) * FULL40[mVh]) * RSNSP [mhos]
Note: RSNSP = 1/RSNS

RSAC [mAh] = (ACR[mVh] - SE(T) * FULL40[mVh]) * RSNSP [mhos]
Note: RSNSP = 1/RSNS

RARC [%] = 100% * (ACR[mVh] - AE(T) * FULL40[mVh]) /
{(AS * FULL(T) - AE(T)) * FULL40[mVh]}

RSRC [%] = 100%* (ACR[mVh] - SE(T) * FULL40[mVh]) /
{(AS * FULL(T) - SE(T)) * FULL40[mVh]}

SPECIAL FEATURE REGISTER FORMAT

All register bits are read and write accessible, with default values specified in each bit definition.

ADDRESS 15H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	X	PIOB

PIOB—PIO Pin Sense and Control Bit. Writing a 0 to the PIOB bit activates the PIO pin open-drain output driver, forcing the PIO pin low. Writing a 1 to PIOB disables the output driver, allowing the PIO pin to be pulled high or used as an input. Reading PIOB returns the logic level forced on the PIO pin. Note that if the PIO pin is left floating with PIOB set, a weak pulldown current source pulls the PIO pin to V_{SS}. PIOB is set to a 1 on power-up. PIOB is also set in Sleep mode to ensure the PIO pin is high-impedance in sleep mode.

Note: Do not write PIOB to 0 if PSPIO is enabled.

X—Reserved Bits.

EEPROM REGISTER

The EEPROM register provides access control of the EEPROM blocks. EEPROM blocks can be locked to prevent alteration of data within the block. Locking a block disables write access to the block. Once a block is locked, it cannot be unlocked. Read access to EEPROM blocks is unaffected by the lock/unlock status.

EEPROM REGISTER FORMAT

ADDRESS 1Fh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EEC	LOCK	X	X	X	X	BL1	BL0

EEC—EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data Function command is in progress. While this bit is high, writes to EEPROM addresses are ignored. A 0 value in this bit indicates that data can be written to unlocked EEPROM.

LOCK—EEPROM Lock Enable. When the lock bit is 0, the Lock Function command is ignored. Writing a 1 to this bit enables the Lock Function command. After setting the lock bit the lock function command must be issued as the next command, or else the lock bit is reset to 0. After the lock operation is completed, the lock bit is reset to 0. The lock bit is a volatile R/W bit, initialized to 0 upon POR.

BL1—Parameter EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 1 (addresses 60h to 7Fh) is locked (read only) while a 0 indicates block 1 is unlocked (read/write).

BL0—User EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 0 (addresses 20h to 2Fh is locked (read only) while a 0 indicates block 0 is unlocked (read/write).

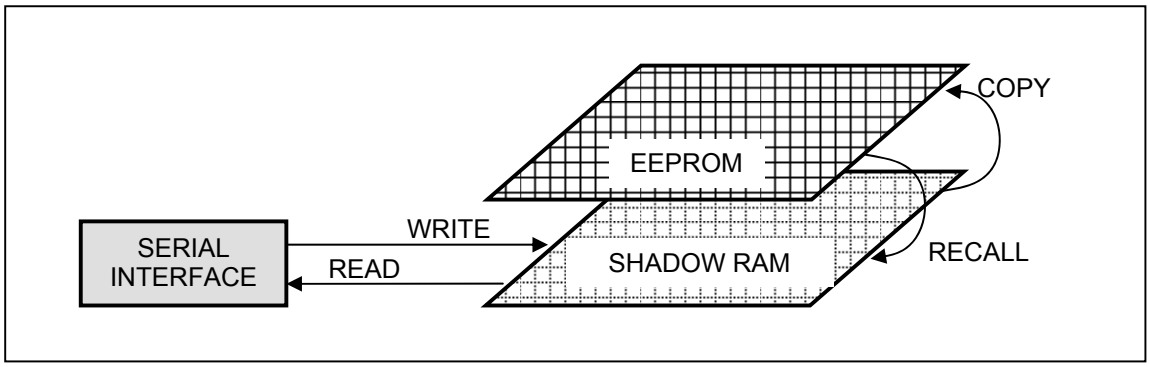
X – Reserved Bits.

MEMORY

The DS2784 has a 256-byte linear memory space with registers for instrumentation, status, and control, as well as EEPROM memory blocks to store parameters and user information. Byte addresses designated as "Reserved" typically return FFh when read. These bytes should not be written. Several byte registers are paired into two-byte registers in order to store 16-bit values. The most significant byte (MSB) of the 16-bit value is located at the even address and the least significant byte (LSB) is located at the next address (odd) byte. When the MSB of a two-byte register is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data command. This prevents updates to the LSB during the read ensuring synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same read data sequence.

EEPROM memory consists of nonvolatile (NV) EEPROM cells overlaying volatile shadow RAM. The read data and write data protocols allow the 1-Wire interface to directly accesses the shadow RAM only. The Copy Data and Recall Data Function commands transfer data between the EEPROM cells and the shadow RAM. In order to modify the data stored in the EEPROM cells, data must be written to the shadow RAM and then copied to the EERPOM. To verify the data stored in the EEPROM cells, the EEPROM data must be recalled to the shadow RAM and then read from the shadow. After issuing the Copy Data Function command, access to the EEPROM block is not available until the EEPROM copy completes, which takes 2ms typically (see t_{EEC} in the *Electrical Characteristics* table).

Figure 5. EEPROM Access via Shadow RAM



USER EEPROM—BLOCK 0

A 16-byte user EEPROM memory (block 0, addresses 20h–2Fh) provides NV memory that is uncommitted to other DS2784 functions. Accessing the user EEPROM block does not affect the operation of the DS2784. User EEPROM is lockable; once locked, write access is not allowed. The battery pack or host system manufacturer can program lot codes, date codes, and other manufacturing or warranty or diagnostic information and then lock it to safeguard the data. User EEPROM can also store parameters for charging to support different size batteries in a host device as well as auxiliary model data such as time to full charge estimation parameters.

PARAMETER EEPROM—BLOCK 1

Model data for the cells, as well as application operating parameters, are stored in the parameter EEPROM (block 1, addresses 60h–7Fh). The ACR (MSB and LSB) and AS registers are automatically saved to EEPROM when the RARC result crosses 4% boundaries. This allows the DS2784 to be located outside the protection FETs.

Table 7. Parameter EEPROM Memory Block

ADDRESS (HEX)	DESCRIPTION	ADDRESS (HEX)	DESCRIPTION
60	**CONTROL**—Control Register	70	AE Segment 4 Slope
61	**AB**— Accumulation Bias	71	AE Segment 3 Slope
62	**AC**—Aging Capacity MSB	72	AE Segment 2 Slope
63	**AC**—Aging Capacity LSB	73	AE Segment 1 Slope
64	**VCHG**—Charge Voltage	74	SE Segment 4 Slope
65	**IMIN**—Minimum Charge Current	75	SE Segment 3 Slope
66	**VAE**—Active-Empty Voltage	76	SE Segment 2 Slope
67	**IAE**—Active-Empty Current	77	SE Segment 1 Slope
68	Active Empty 40	78	**RSGAIN**—Sense Resistor Gain MSB
69	$\mathbf{R_{SNSP}}$—Sense Resistor Prime	79	**RSGAIN**—Sense Resistor Gain LSB
6A	Full 40 MSB	7A	**RSTC**—Sense Resistor Temp Coefficient
6B	Full 40 LSB	7B	**COB**—Current Offset Bias
6C	Full Segment 4 Slope	7C	**TBP34**
6D	Full Segment 3 Slope	7D	**TBP23**
6E	Full Segment 2 Slope	7E	**TBP12**
6F	Full Segment 1 Slope	7F	**Protector Threshold Register**

Table 8. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Protection Register	R/W
01	Status Register	R/W
02	RAAC MSB	R
03	RAAC LSB	R
04	RSAC MSB	R
05	RSAC LSB	R
06	RARC	R
07	RSRC	R
08	Average Current Register MSB	R
09	Average Current Register LSB	R
0A	Temperature Register MSB	R
0B	Temperature Register LSB	R
0C	Voltage Register MSB	R
0D	Voltage Register LSB	R
0E	Current Register MSB	R
0F	Current Register LSB	R
10	Accumulated Current Register MSB	R/W *
11	Accumulated Current Register LSB	R/W *
12	Accumulated Current Register LSB-1	R
13	Accumulated Current Register LSB-2	R
14	Age Scalar	R/W *
15	Special Feature Register	R/W
16	Full MSB	R
17	Full LSB	R
18	Active-Empty MSB	R
19	Active-Empty LSB	R
1A	Standby-Empty MSB	R
1B	Standby-Empty LSB	R
1C to 1E	Reserved	—
1F	EEPROM Register	R/W
20 to 2F	User EEPROM, Lockable, Block 0	R/W
38 to 5F	Reserved	—
60 to 7F	Parameter EEPROM, Lockable, Block 1	R/W
80 to AF	Reserved	—
B0	Factory Gain RSGAIN MSB	R
B1	Factory Gain RSGAIN LSB	R
B2 to FF	Reserved	—

* Register value is automatically saved to EEPROM during Active mode operation and recalled from EEPROM on power-up.

AUTHENTICATION

Authentication is performed using a FIPS-180-compliant SHA-1 one-way hash algorithm on a 512-bit message block. The message block consists of a 64-bit secret, a 64-bit challenge and 384 bits of constant data. Optionally, the 64-bit net address replaces 64 of the 384 bits of constant data used in the hash operation. Contact Maxim for details of the message block organization.

The host and the DS2784 both calculate the result based on the mutually known secret. The result of the hash operation is known as the message authentication code (MAC) or message digest. The MAC is returned by the DS2784 for comparison to the host's MAC. Note that the secret is never transmitted on the bus and thus cannot be captured by observing bus traffic. Each authentication attempt is initiated by the host system by providing a 64-bit random challenge by the Write Challenge command. The host then issues the compute MAC or compute MAC with ROM ID command. The MAC is computed per FIPS 180, and then returned as a 160-bit serial stream, beginning with the least significant bit.

DS2784 AUTHENTICATION COMMANDS

WRITE CHALLENGE [0Ch]. This command writes the 64-bit challenge to the DS2784. The LSB of the 64-bit data argument can begin immediately after the MSB of the command has been completed. If more than 64-bits are written, the final value in the challenge register will be indeterminate. The Write Challenge command must be issued prior to every Compute MAC or Compute Next Secret command for reliable results.

COMPUTE MAC WITHOUT ROM ID [36h]. This command initiates a SHA-1 computation without including the ROM ID in the message block. Since the ROM ID is not used, this command allows the use of a master secret and MAC response independent of the ROM ID. The DS2784 computes the MAC in t_{SHA} after receiving the last bit of this command. After the MAC computation is complete, the host must write 8 write-zero time slots and then issue 160 read-time slots to receive the 20-byte MAC. See Figure 9 for command timing.

COMPUTE MAC WITH ROM ID [35h]

This command is structured the same as the compute MAC without ROM ID, except that the ROM ID is included in the message block. With the ROM ID unique to each DS2784 included in the MAC computation, the MAC is unique to each token. See White Paper 4: *Glossary of 1-Wire SHA-1 Terms*, for more information. See Figure 9 for command timing.

SHA-1-related commands used while authenticating a battery or peripheral device are summarized in Table 9 for convenience. Four additional commands for clearing, computing, and locking of the secret are described in detail in the following section.

Table 9. Authentication Function Commands

COMMAND	HEX	FUNCTION
Write Challenge	0C	Writes 64-bit challenge for SHA-1 processing. Required prior to issuing Compute MAC and Compute Next Secret commands.
Compute MAC *Without* ROM ID and Return MAC	36	Computes hash operation of the message block with logical 1s in place of the ROM ID. Returns the 160-bit MAC.
Compute MAC *With* ROM ID and Return MAC	35	Computes hash operation of the message block including the ROM ID. Returns the 160-bit MAC.

SECRET MANAGEMENT FUNCTION COMMANDS

CLEAR SECRET [5Ah]. This command sets the 64-bit secret to all 0s (0000 0000 0000 0000h). The host must wait t_{EEC} for the DS2784 to write the new secret value to EEPROM. See Figure 12 for command timing.

COMPUTE NEXT SECRET WITHOUT ROM ID [30h]. This command initiates a SHA-1 computation of the MAC and uses a portion of the resulting MAC as the next or new secret. The hash operation is performed with the current 64-bit secret and the 64-bit challenge. Logical 1s are loaded in place of the ROM ID. 64 bits of the output MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{EEC} for the DS2784 to write the new secret value to EEPROM. See Figure 10 for command timing.

COMPUTE NEXT SECRET WITH ROM ID [33h]. This command initiates a SHA-1 computation of the MAC and uses a portion of the resulting MAC as the next or new secret. The hash operation is performed with the current 64-bit secret, the 64-bit ROM ID and the 64-bit challenge. 64 bits of the output MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{EEC} for the DS2784 to write the new secret value to EEPROM. See Figure 10 for command timing.

LOCK SECRET [60h]. This command write protects the 64-bit secret to prevent accidental or malicious overwrite of the secret value. The secret value stored in EEPROM becomes “final”. The host must wait t_{EEC} for the DS2784 to write the lock secret bit to EEPROM. See Figure 12 for command timing.

Table 10. Secret Loading Function Commands

COMMAND	HEX	FUNCTION
Clear Secret	5A	Clears the 64-bit Secret to 0000 0000 0000 0000h.
Compute Next Secret *Without* ROM ID	30	Generates new global secret.
Compute Next Secret *With* ROM ID	33	Generates new unique secret.
Lock Secret	60	Sets lock bit to prevent changes to the secret.

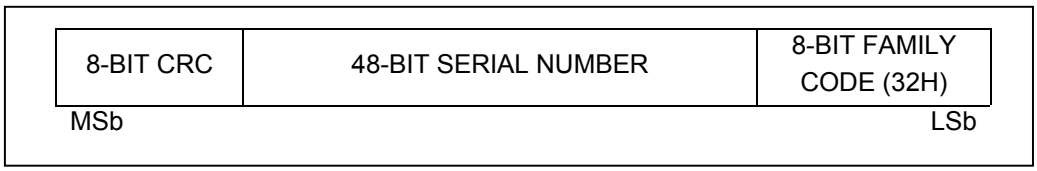
1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. A multidrop bus is a 1-Wire bus with multiple slaves, while a single-drop bus has only one slave device. In all instances, the DS2784 is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of five topics: 64-bit net address, CRC generation, hardware configuration, transaction sequence, and 1-Wire signaling.

64-BIT NET ADDRESS (ROM ID)

Each DS2784 has a unique, factory-programmed 1-Wire net address that is 64 bits in length. The term net address is synonymous with the ROM ID or ROM code terms used in the DS2502 and other 1-Wire documentation. The first eight bits of the net address are the 1-Wire family code (32h). The next 48 bits are a unique serial number. The last eight bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 6). The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the DS2784 to communicate through the 1-Wire protocol detailed in this data sheet.

Figure 6. 1-Wire Net Address Format



CRC GENERATION

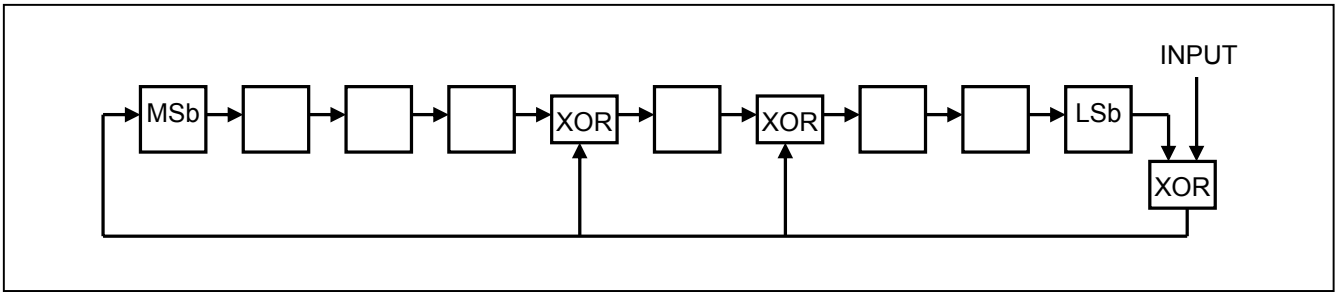
The DS2784 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address and generates a CRC during some command protocols. To ensure error-free transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2784.

The host system is responsible for verifying the CRC value and taking action as a result. The DS2784 does not compare CRC values and does not prevent a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC can result in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 7, or it can be generated in software using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor iButton Products*.

In the circuit in Figure 7, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value.

Figure 7. 1-Wire CRC Generation Block Diagram



During some command sequences, the DS2784 also generates an 8-bit CRC and provides this value to the bus master to facilitate validation for the transfer of command, address, and data from the bus master to the DS2784. The DS2784 computes an 8-bit CRC for the command and address bytes received from the bus master for the read memory, read status, and read/generate CRC commands to confirm that these bytes have been received correctly. The CRC generator on the DS2784 is also used to provide verification of error-free data transfer as each EEPROM page is sent to the master during a Read Data/Generate CRC command and for the 8 bytes of information in the status memory field.

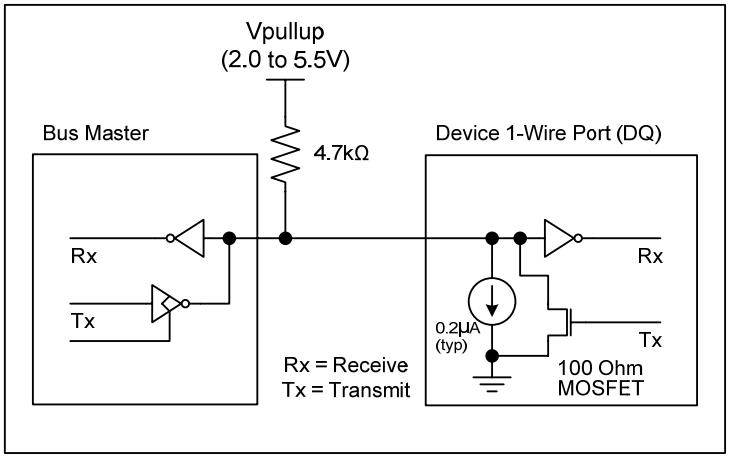
In each case where a CRC is used for data transfer validation, the bus master must calculate the CRC value using the same polynomial function and compare the calculated value to the CRC either stored in the DS2784 Net Address or computed by the DS2784. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry in the DS2784 that prevents the command sequence from proceeding if the stored or calculated CRC from the DS2784 and the calculated CRC from the host do not match.

HARDWARE CONFIGURATION

Because the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The DS2784 uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 8. If a bidirectional pin is not available on the bus master, separate output, and input pins can be connected together.

The 1-Wire bus must have a pullup resistor at the bus-master end of the bus. A value of between 2kΩ and 5kΩ is recommended. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state to properly resume the transaction later. Note that if the bus is left low for more than t_{LOW0}, slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

Figure 8. 1-Wire Bus Interface Circuitry



TRANSACTION SEQUENCE

The protocol for accessing the DS2784 through the 1-Wire port is as follows:

- Initialization
- Net Address Command
- Function Command(s)
- Data Transfer (not all commands have data transfer)

All transactions of the 1-Wire bus begin with an initialization sequence consisting of a reset pulse transmitted by the bus master, followed by a presence pulse simultaneously transmitted by the DS2784 and any other slaves on the bus. The presence pulse tells the bus master that one or more devices are on the bus and ready to operate. For more details, see the *1-Wire Signaling* section.

NET ADDRESS COMMANDS

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following paragraphs. The name of each net address command (ROM command) is followed by the 8-bit op code for that command in square brackets.

Read Net Address [33h]. This command allows the bus master to read the DS2784's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result).

Match Net Address [55h]. This command allows the bus master to specifically address one DS2784 on the 1-Wire bus. Only the addressed DS2784 responds to any subsequent function command. All other slave devices ignore the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]. This command saves time when there is only one DS2784 on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]. This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the *Book of iButton® Standards* for a comprehensive discussion of a net address search, including an actual example (www.maxim-ic.com/iButtonBook).

FUNCTION COMMANDS

After successfully completing one of the net address commands, the bus master can access the features of the DS2784 with any of the function commands described in the following paragraphs. The name of each function is followed by the 8-bit op code for that command in square brackets. The function commands are summarized below in Table 11.

Read Data [69h, XX]. This command reads data from the DS2784 starting at memory address XX. The LSb of the data in address XX is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address XX + 1 is available to be read immediately after the MSb of the data at address XX. If the bus master continues to read beyond address FFh, data is read starting at memory address 00 and the address is automatically incremented until a reset pulse occurs. Addresses labeled “Reserved” in the memory map contain undefined data values. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary. Reads from EEPROM block addresses return the data in the shadow RAM. A Recall Data command is required to transfer data from the EEPROM to the shadow. See Table 7 for more details.

Write Data [6Ch, XX]. This command writes data to the DS2784 starting at memory address XX. The LSb of the data to be stored at address XX can be written immediately after the MSb of address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address XX + 1 can be written immediately after the MSb to be stored at address XX. If the bus master continues to write beyond address FFh, the data starting at address 00 is overwritten. Writes to read-only addresses, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM block addresses modify the shadow RAM. A Copy Data command is required to transfer data from the shadow to the EEPROM. See Table 7 for more details.

Copy Data [48h, XX]. This command copies the contents of the EEPROM shadow RAM to EEPROM cells for the EEPROM block containing address XX. Copy Data commands that address locked blocks are ignored. While the copy data command is executing, the EEC bit in the EEPROM register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while the copy is in progress. The Copy Data command takes t_{EEC} time to execute, starting on the next falling edge after the address is transmitted.

Recall Data [B8h, XX]. This command recalls the contents of the EEPROM cells to the EEPROM shadow memory for the EEPROM block containing address XX.

Lock [6Ah, XX]. This command locks (write protects) the block of EEPROM containing address XX. The lock bit in the EEPROM register must be set to 1 before the Lock command is executed. To help prevent unintentional locks, one must issue the Lock command immediately after setting the lock bit (EEPROM register, address 1Fh, bit 06) to a 1. If the lock bit is 0 or if setting the lock bit to 1 does not immediately precede the Lock command, the Lock command has no effect. The Lock command is permanent; a locked block can never be written again.

Table 11. All Function Commands

COMMAND	HEX	DESCRIPTION
Write Challenge	0C	Writes 64-bit challenge for SHA-1 processing. Required immediately prior to all Compute MAC and Compute Next Secret commands.
Compute MAC *Without* ROM ID and Return MAC	36	Computes hash operation of message block with logical 1s in place of the ROM ID.
Compute MAC *With* ROM ID and Return MAC	35	Computes hash operation of message block using the ROM ID.
Clear Secret	5A	Clears the 64-bit secret to 0000 0000 0000 0000h.
Compute Next Secret *Without* ROM ID	30	Generates new global secret.
Compute Next Secret *With* ROM ID	33	Generates new unique secret.
Lock Secret	60	Sets lock bit to prevent changes to the secret.
Read Data	69, XX	Reads data from memory starting at address XX.
Write Data	6C, XX	Writes data to memory starting at address XX.
Copy Data	48, XX	Copies shadow RAM data to EEPROM block containing address XX.
Recall Data	B8, XX	Recalls EEPROM block containing address XX to RAM.
Lock	6A, XX	Permanently locks the block of EEPROM containing address XX.
Set Overdrive	8B	Sets 1-Wire interface timings to overdrive.
Clear Overdrive	8D	Sets 1-Wire interface timings to standard (factory default).
Reset	C4	Resets DS2784 (software POR).

Table 12. Guide to Function Command Requirements

COMMAND	ISSUE MEMORY ADDRESS	ISSUE 00h BEFORE READ	READ/WRITE TIME SLOTS
Write Challenge	—	—	Write: 64
Compute MAC	—	Yes	Read: up to 160
Compute Next Secret	—	—	—
Clear/Lock Secret, Set/Clear Overdrive	—	—	—
Read Data	8 bits	—	Read: up to 2048
Write Data	8 bits	—	Write: up to 2048
Copy Data	8 bits	—	—
Recall Data	8 bits	—	—
Lock	8 bits	—	—
Reset	—	—	—

Figure 9. Compute MAC Function Command

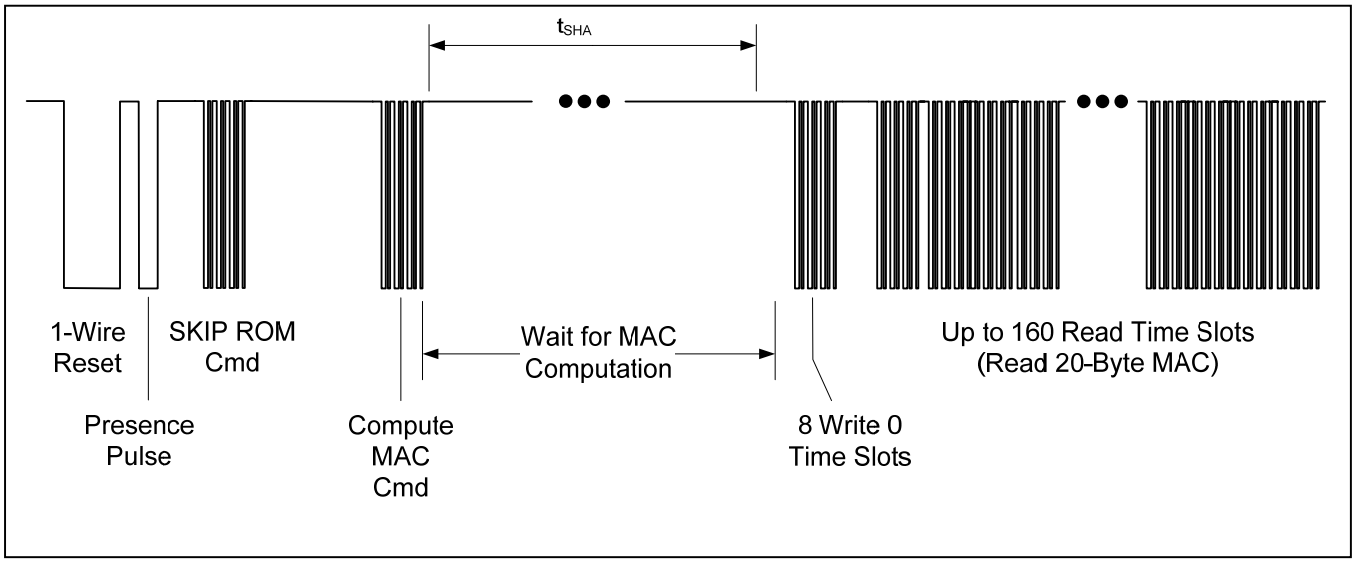


Figure 10. Compute Next Secret Function Command

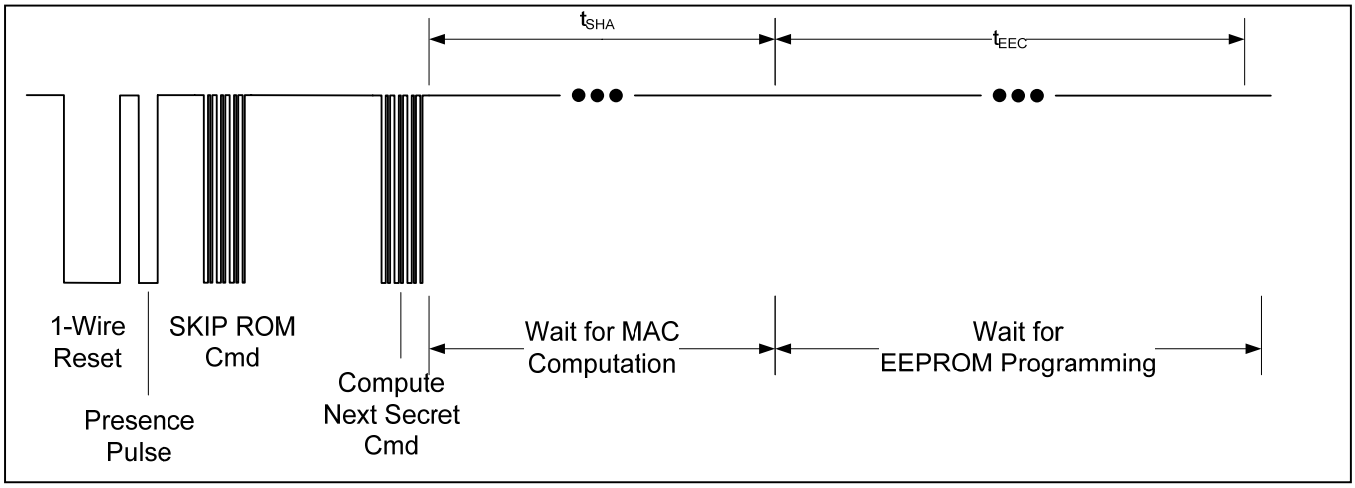


Figure 11. Copy Function Command

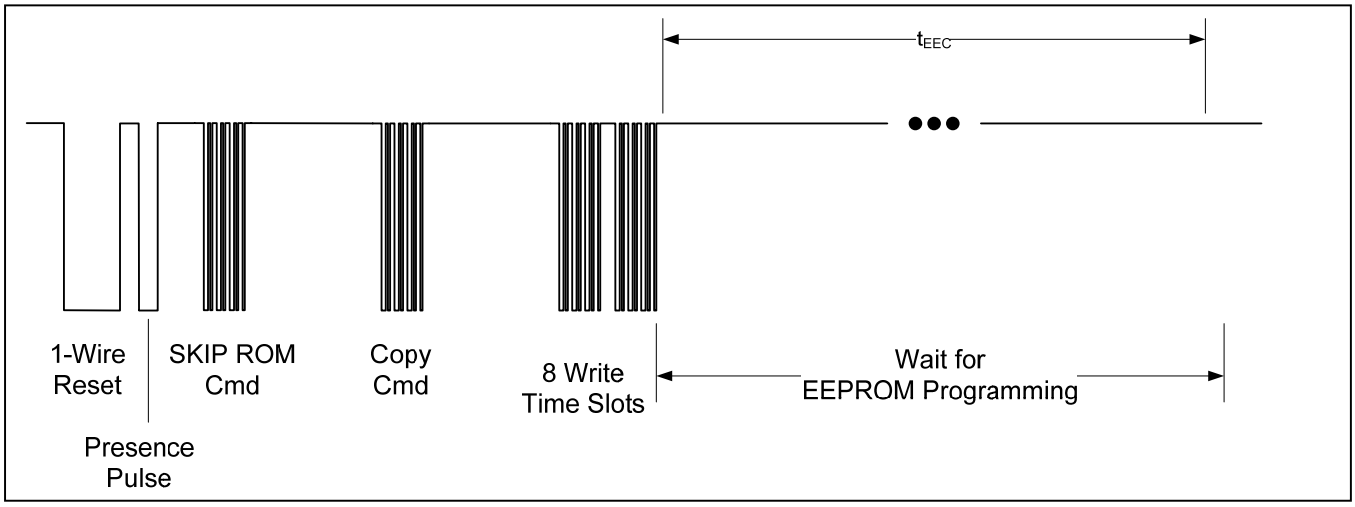
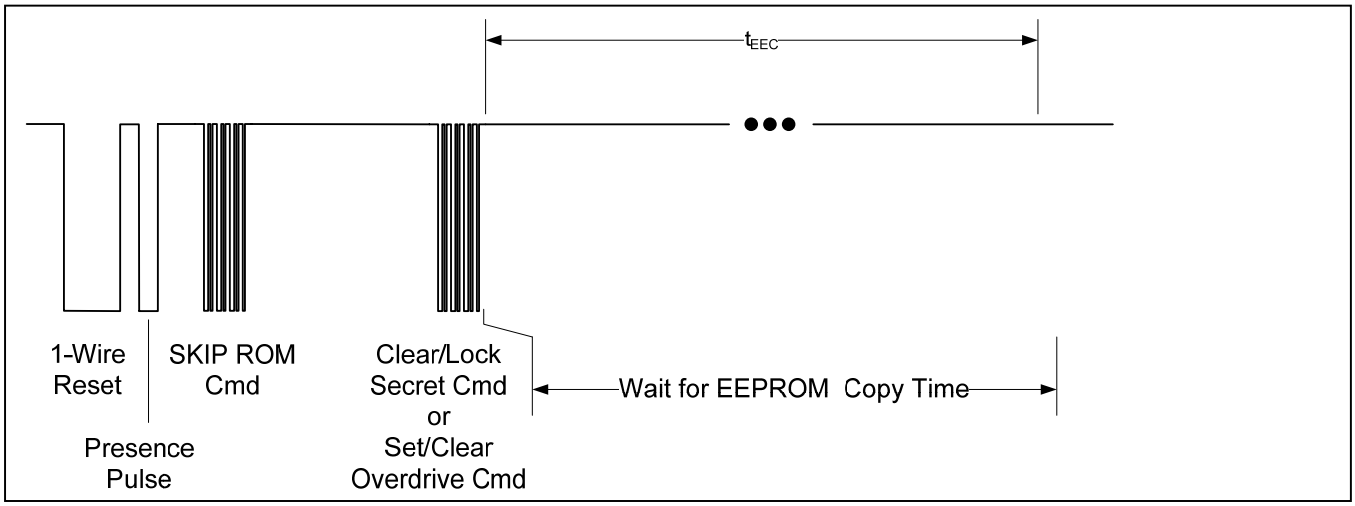


Figure 12. Clear/Lock Secret, Set/Clear Overdrive Function Commands

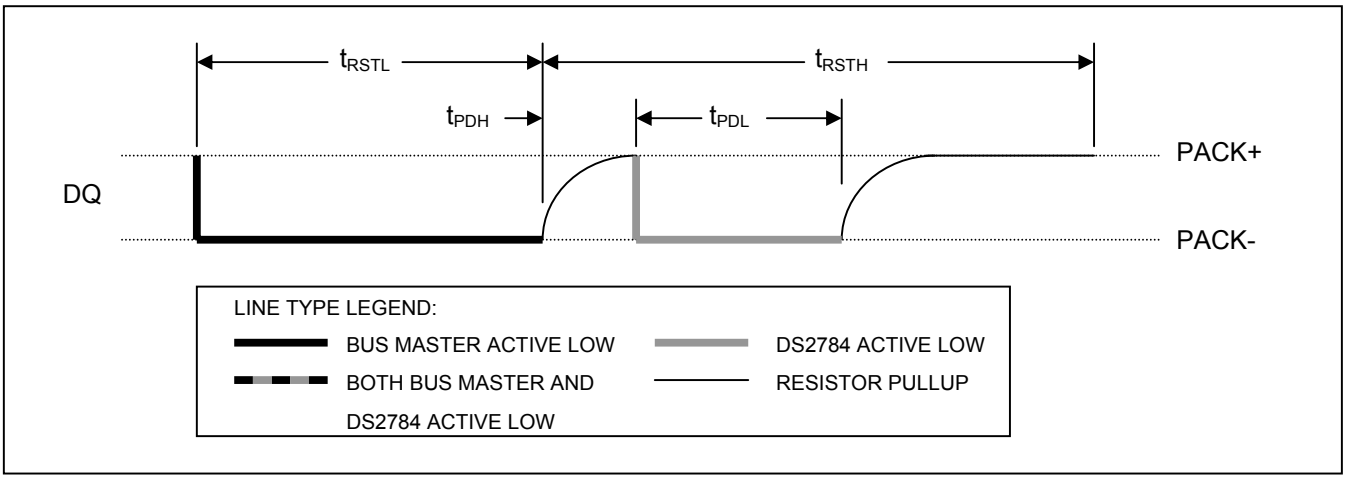


I/O SIGNALING

The 1-Wire bus requires strict signaling protocols to ensure data integrity. The four protocols used by the DS2784 are as follows: the initialization sequence (reset pulse followed by presence pulse), write 0, write 1, and read data. The bus master initiates all these types of signaling except the presence pulse.

The initialization sequence required to begin any communication with the DS2784 is shown in Figure 13. A presence pulse following a reset pulse indicates that the DS2784 is ready to accept a net address command. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into Receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the DS2784 waits for t_{PDH} and then transmits the presence pulse for t_{PDL}.

Figure 13. 1-Wire Initialization Sequence



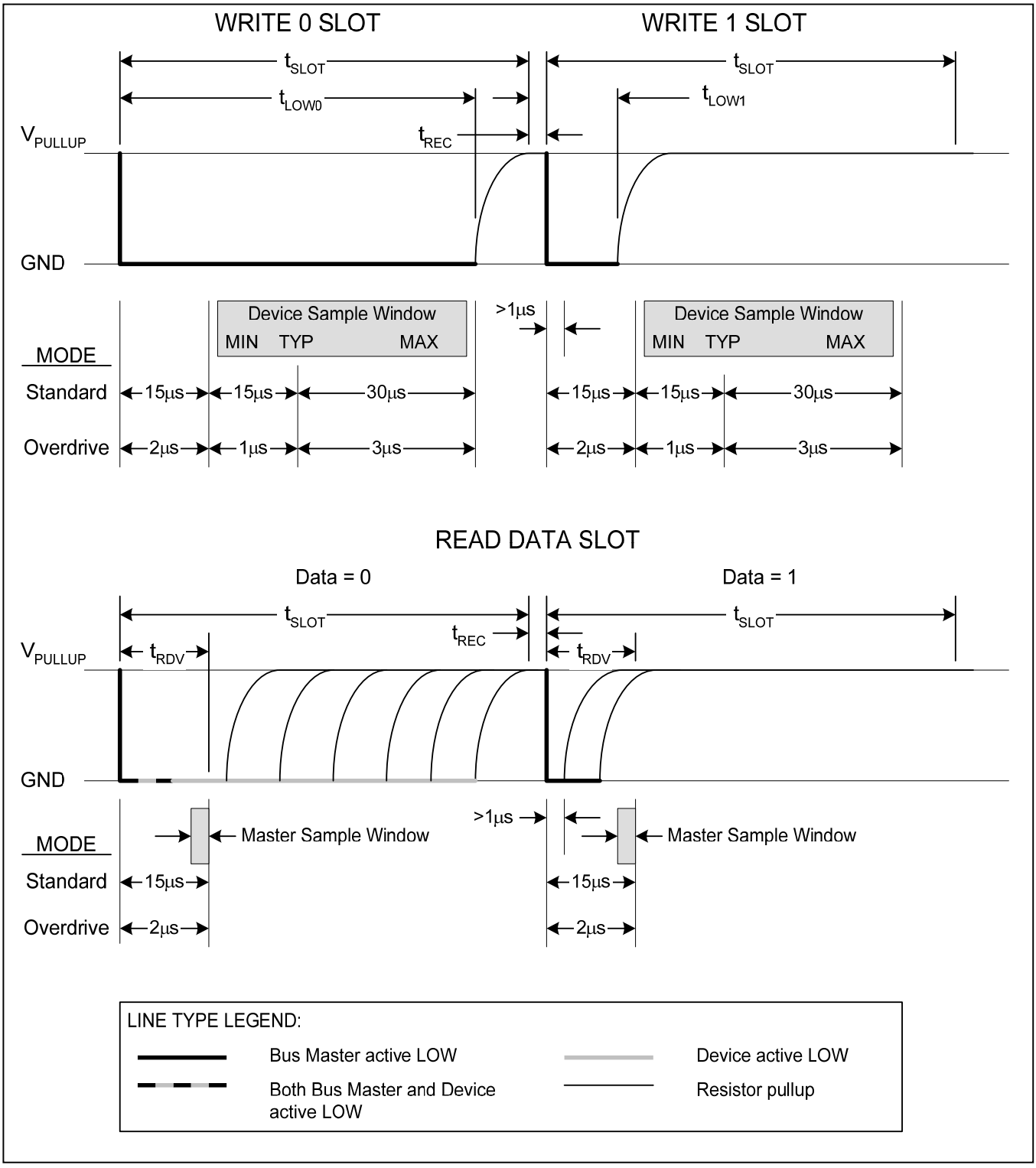
WRITE-TIME SLOTS

A write-time slot is initiated when the bus master pulls the 1-Wire bus from a logic-high (inactive) level to a logic-low level. There are two types of write-time slots: write 1 and write 0. All write-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The DS2784 samples the 1-Wire bus line between t_{LOW1_MAX} and t_{LOW0_MIN} after the line falls. If the line is high when sampled, a write 1 occurs. If the line is low when sampled, a write 0 occurs. The sample window is illustrated in Figure 14. For the bus master to generate a write-1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high less than t_{RDV} after the start of the write time slot. For the host to generate a write 0 time slot, the bus line must be pulled low and held low for the duration of the write-time slot.

READ-TIME SLOTS

A read-time slot is initiated when the bus master pulls the 1-Wire bus line from a logic-high level to a logic-low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the DS2784 to present valid data. The bus master can then sample the data t_{RDV} from the start of the read-time slot. By the end of the read-time slot, the DS2784 releases the bus line and allows it to be pulled high by the external pullup resistor. All read-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. See Figure 14 and the timing specifications in the *Electrical Characteristics* table for more information.

Figure 14. 1-Wire Write and Read-Time Slots



PACKAGE INFORMATION

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