

FEATURES:

- Four 128k x 8-bit EEPROMs MCM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
 - > 100 krad (Si)
 - Dependent upon orbit
- Excellent Single Event Effects
 - SEL > 120 MeV/mg/cm²
 - SEU > 90 MeV/mg/cm² read mode
 - SEU = 18 MeV/mg/cm² write mode
- Package: 40 pin RAD-PAK® flat pack
- High speed:
 - 120, 150, and 200 ns maximum access times available
- Data Polling and Ready/Busy signal
- Software data protection
- Write protection by RES pin
- High endurance
 - 10,000 erase/write (in Page Mode), 10 year data retention
- Page write mode: 1 to 128 byte page
- Low power dissipation
 - 88 mW/MHz active mode
 - 440 µW standby mode

DESCRIPTION:

Maxwell Technologies' 79C0408 multi-chip module (MCM) memory features a greater than 100 krad (Si) total dose tolerance, dependent upon orbit. Using Maxwell Technologies' patented radiation-hardened RAD-PAK® MCM packaging technology, the 79C0408 is the first radiation-hardened 4 Megabit MCM EEPROM for space applications. The 79C0408 uses four 1 Megabit high-speed CMOS die to yield a 4 Megabit product. The 79C0408 is capable of in-system electrical Byte and Page programmability. It has a 128 bytes Page Programming function to make its erase and write operations faster. It also features Data Polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 79C0408, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC optional standard algorithm.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class K.

TABLE 1. 79C0408 PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
16-9, 32-31, 28, 30, 8, 33, 7, 36, 6	A0 to A16	Address Input
17-19, 22-26	I/O0 to I/O7	Data Input/Output
29	\overline{OE}	Output Enable
2, 3, 38, 39	$\overline{CE1-4}$	Chip Enable 1 through 4
34	\overline{WE}	Write Enable
1, 27, 40	VCC	Power Supply
4, 20, 21, 37	VSS	Ground
4	RDY/BUSY	Ready/Busy
35	\overline{RES}	Reset

TABLE 2. 79C0408 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	-0.6	7.0	V
Input Voltage	V_{IN}	-0.5 ¹	7.0	V
Operating Temperature Range	T_{OPR}	-55	125	°C
Storage Temperature Range	T_{STG}	-65	150	°C

1. $V_{IN\ MIN} = -3.0V$ FOR PULSE WIDTH $\leq 50NS$.

TABLE 3. 79C0408 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Supply Voltage	1	V_{CC}	4.5	5.5	V
Input Voltage	1	V_{IL}	-0.3 ¹	0.8	V
		V_{IH}	2.2	$V_{CC} + 0.3$	V
		V_H	$V_{CC} - 0.5$	$V_{CC} + 1$	V
Case Operating Temperature	1	T_C	-55	125	°C

1. $V_{IL\ min} = -1.0V$ for pulse width $\leq 50\ ns$

TABLE 4. 79C0408 CAPACITANCE¹
(T_A = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance: V _{IN} = 0 V ²	C _{IN}			pf
\overline{WE}		--	24	
\overline{CE}_{1-4}		--	6	
\overline{OE}		--	24	
A ₀₋₁₆		--	24	
Output Capacitance: V _{OUT} = 0 V ²	C _{OUT}		48	pF

1. Guaranteed by design.
2. Guaranteed by design.

TABLE 5. 79C0408 DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ±10%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITION	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V _{CC} = 5.5V, V _{IN} = 5.5V ¹	1, 2, 3	I _{IL}			μA
	\overline{CE}_{1-4}	1, 2, 3		--	2 ¹	
	\overline{OE} , \overline{WE}_{1-4}	1, 2, 3		--	4	
	A ₀₋₁₆	1, 2, 3		--	4	
Output Leakage Current	V _{CC} = 5.5V, V _{OUT} = 5.5V/0.4V	1, 2, 3	I _{LO}	--	2	μA
Standby V _{CC} Current ²	$\overline{CE} = V_{CC}$	1, 2, 3	I _{CC1}	--	20	μA
	$\overline{CE} = V_{IH}$	1, 2, 3	I _{CC2}	--	1	mA
Operating V _{CC} Current	I _{OUT} = 0mA, Duty = 100%, Cycle = 1μs at V _{CC} = 5.5V	1, 2, 3	I _{CC3}	--	15	mA
	I _{OUT} = 0mA, Duty = 100%, Cycle = 150ns at V _{CC} = 5.5V	1, 2, 3		--	50	
Input Voltage RES_PIN		1, 2, 3	V _{IL}	--	0.8	V
		1, 2, 3	V _{IH}	2.2	--	
		1, 2, 3	V _H	V _{CC} - 0.5	--	
Output Voltage	I _{OL} = 2.1 mA	1, 2, 3	V _{OL}	--	0.4	V
	I _{OH} = -0.4 mA	1, 2, 3	V _{OH}	2.4	--	

1. I_{IL} on RES = 100 uA max.
2. One \overline{CE} active.

TABLE 6. 79C0408 AC ELECTRICAL CHARACTERISTICS FOR READ OPERATIONS¹
 ($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125^\circ\text{C}$)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Address Access Time $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{ACC}	-- -- --	120 150 200	ns
Chip Enable Access Time $\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{CE}	-- -- --	120 150 200	ns
Output Enable Access Time $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{OE}	0 0 0	75 75 125	ns
Output Hold to Address Change $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{OH}	0 0 0	-- -- --	ns
Output Disable to High-Z ² $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{DF}	0 0 0	50 50 60	ns
$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	9, 10, 11	t_{DFR}	0 0 0	300 350 450	
RES to Output Delay $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ ³ -120 -150 -200		t_{RR}	-- -- --	400 450 650	ns

1. Test conditions: Input pulse levels - 0.4V to 2.4V; input rise and fall times < 20ns; output load - 1 TTL gate + 100pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.
2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

TABLE 7. 79C0408 AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATIONS
 ($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125^\circ\text{C}$)

PARAMETER	SUBGROUPS	SYMBOL	MIN ¹	MAX	UNIT
Address Setup Time -120 -150 -200	9, 10, 11	t_{AS}	0 0 0	-- -- --	ns
Chip Enable to Write Setup Time (\overline{WE} Controlled) -120 -150 -200	9, 10, 11	t_{CS}	0 0 0	-- -- --	ns
Write Pulse Width CE Controlled -120 -150 -200 WE Controlled -120 -150 -200	9, 10, 11	t_{CW} t_{WP}	 200 250 350 200 250 350	 -- -- -- -- -- --	ns
Address Hold Time -120 -150 -200	9, 10, 11	t_{AH}	150 150 200	-- -- --	ns
Data Setup Time -120 -150 -200	9, 10, 11	t_{DS}	75 100 150	-- -- --	ns
Data Hold Time -120 -150 -200	9, 10, 11	t_{DH}	10 10 20	-- -- --	ns
Chip Enable Hold Time (\overline{WE} Controlled) -120 -150 -200	9, 10, 11	t_{CH}	0 0 0	-- -- --	ns
Write Enable to Write Setup Time (\overline{CE} Controlled) -120 -150 -200	9, 10, 11	t_{WS}	0 0 0	-- -- --	
Write Enable Hold Time (\overline{CE} Controlled) -120 -150 -200	9, 10, 11	t_{WH}	0 0 0	-- -- --	

TABLE 7. 79C0408 AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATIONS
 ($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125^\circ\text{C}$)

PARAMETER	SUBGROUPS	SYMBOL	MIN ¹	MAX	UNIT
Output Enable to Write Setup Time -120 -150 -200	9, 10, 11	t_{OES}	0 0 0	-- -- --	ns
Output Enable Hold Time -120 -150 -200	9, 10, 11	t_{OEH}	0 0 0	-- -- --	ns
Write Cycle Time ² -120 -150 -200	9, 10, 11	t_{WC}	-- -- --	10 10 20	ms
Data Latch Time -120 -150 -200	9, 10, 11	t_{DL}	250 300 400	-- -- --	ns
Byte Load Window -120 -150 -200	9, 10, 11	t_{BL}	100 100 200	-- -- --	μs
Byte Load Cycle -120 -150 -200	9, 10, 11	t_{BLC}	0.55 0.55 0.95	30 30 30	μs
Time to Device Busy -120 -150 -200	9, 10, 11	t_{DB}	100 120 170	-- -- --	ns
Write Start Time ³ -120 -150 -200	9, 10, 11	t_{DW}	150 150 250	-- -- --	ns
RES to Write Setup Time -120 -150 -200	9, 10, 11	t_{RP}	100 100 200	-- -- --	μs
V_{CC} to RES Setup Time ⁴ -120 -150 -200	9, 10, 11	t_{RES}	1 1 3	-- -- --	μs

1. Use this device in a longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/BUSY are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/BUSY are used.
4. Gauranteed by design.

TABLE 8. 79C0408 MODE SELECTION 1, 2

PARAMETER	\overline{CE}^3	\overline{OE}	\overline{WE}	I/O	\overline{RES}	RDY/ \overline{BUSY}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	High-Z
Standby	V_{IH}	X	X	High-Z	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	High-Z --> V_{OL}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O7)	V_H	V_{OL}
Program	X	X	X	High-Z	V_{IL}	High-Z

1. X = Don't care.
2. Refer to the recommended DC operating conditions.
3. For \overline{CE}_{1-4} only one \overline{CE} can be used ("on") at a time.

FIGURE 1. READ TIMING WAVEFORM

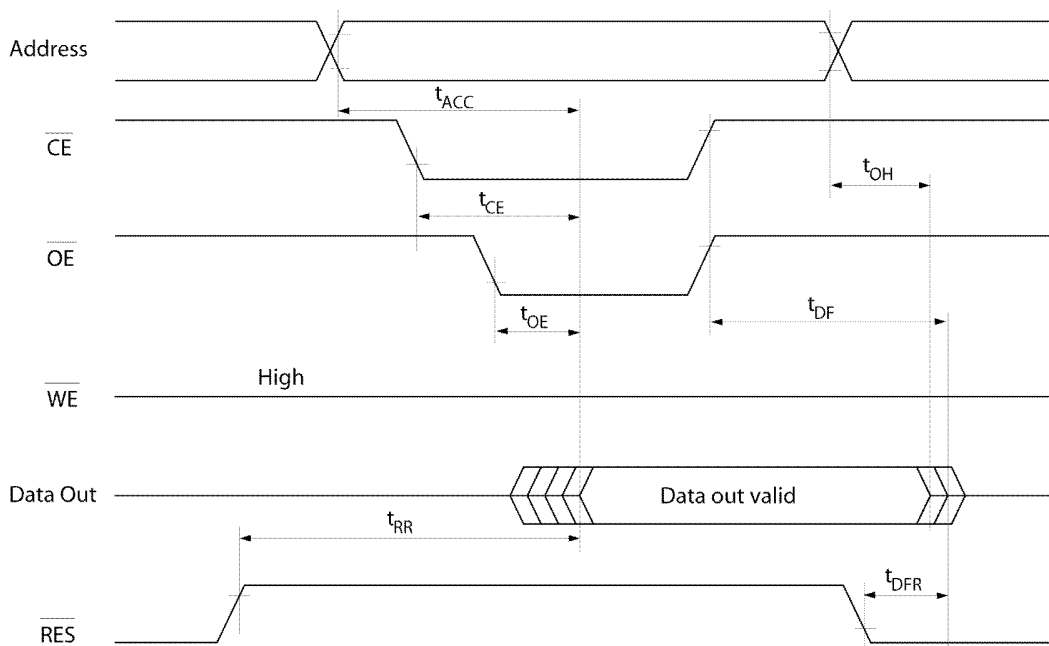


FIGURE 2. BYTE WRITE TIMING WAVEFORM(1) (\overline{WE} CONTROLLED)

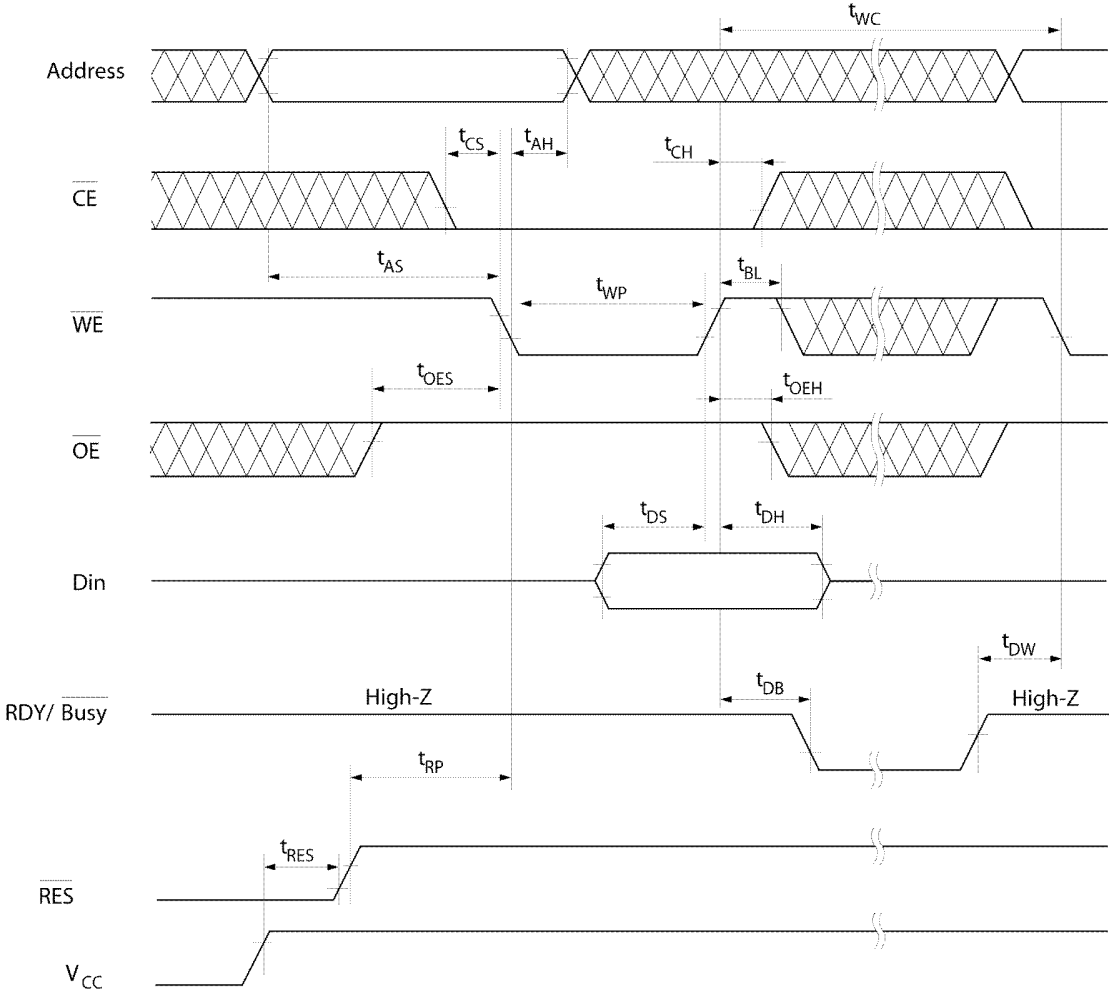


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) (\overline{CE} CONTROLLED)

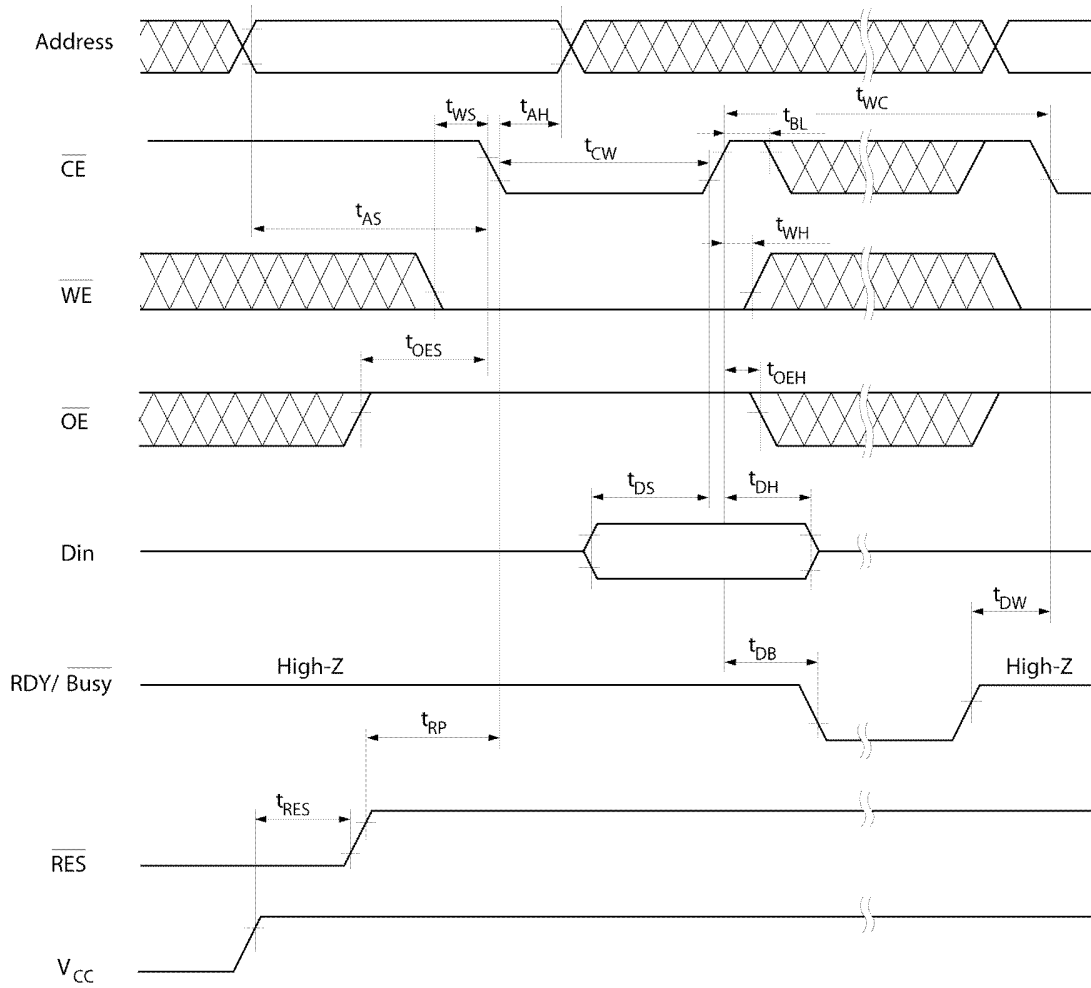


FIGURE 4. PAGE WRITE TIMING WAVEFORM(1) (\overline{WE} CONTROLLED)

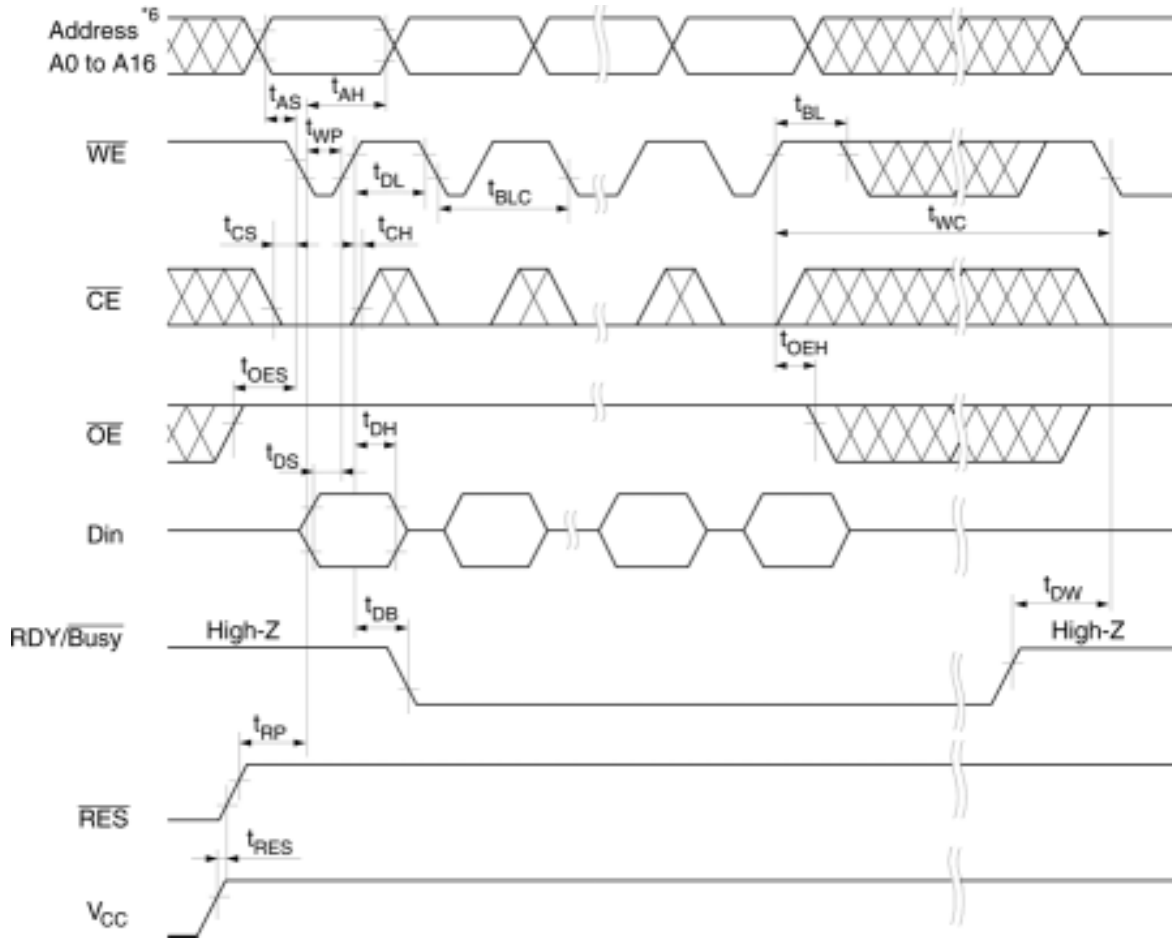


FIGURE 5. PAGE WRITE TIMING WAVEFORM(2) (\overline{CE} CONTROLLED)

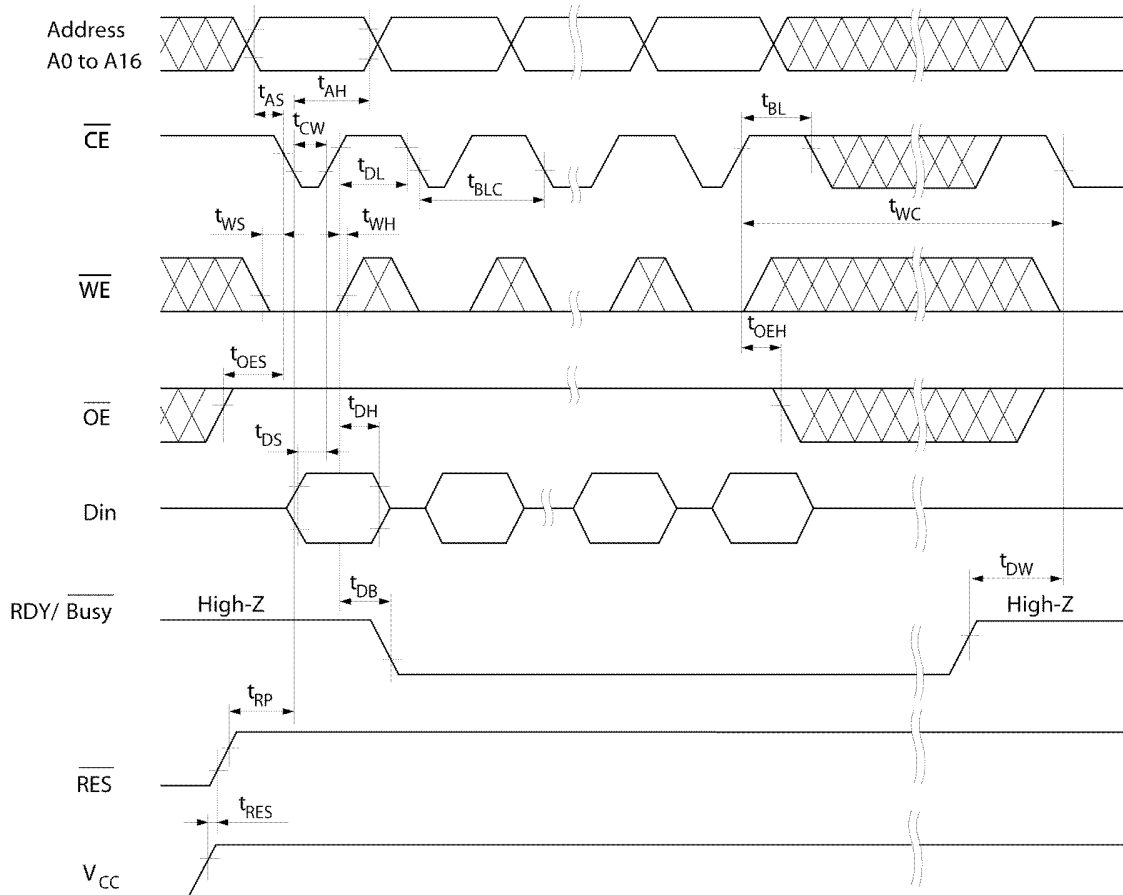


FIGURE 6. DATA POLLING TIMING WAVEFORM

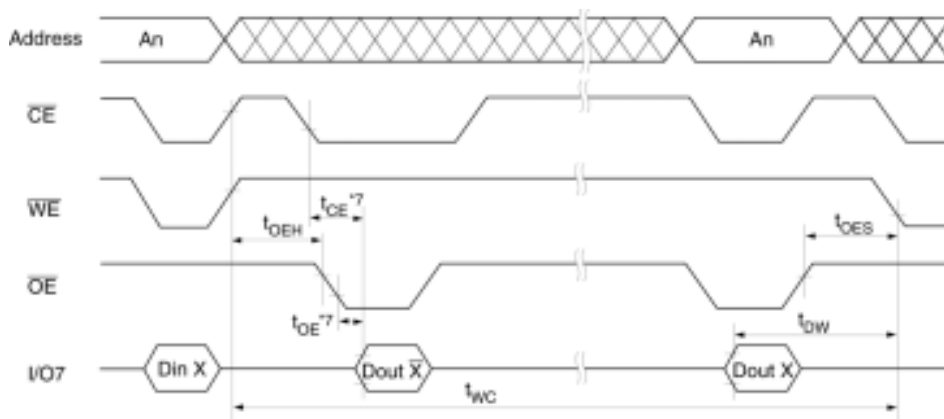


FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM(1) (IN PROTECTION MODE)

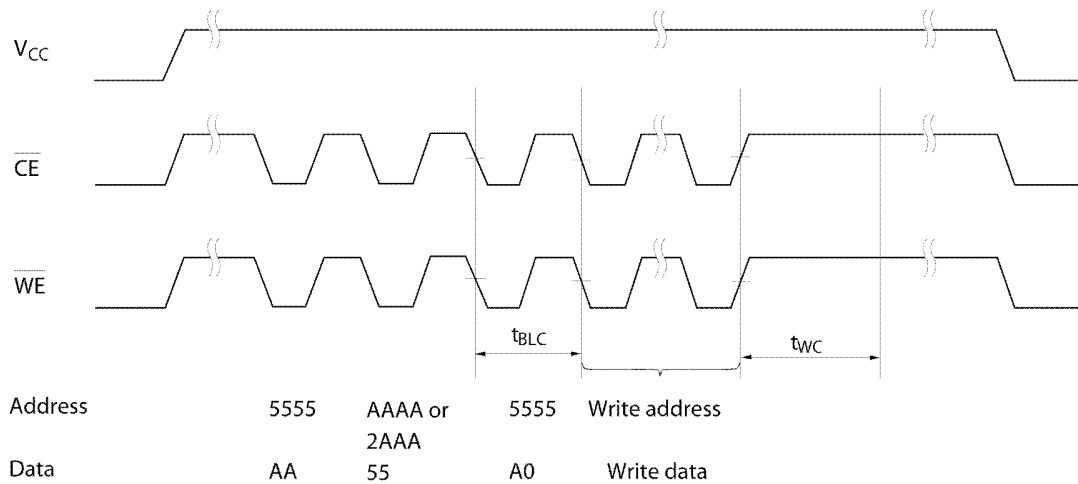
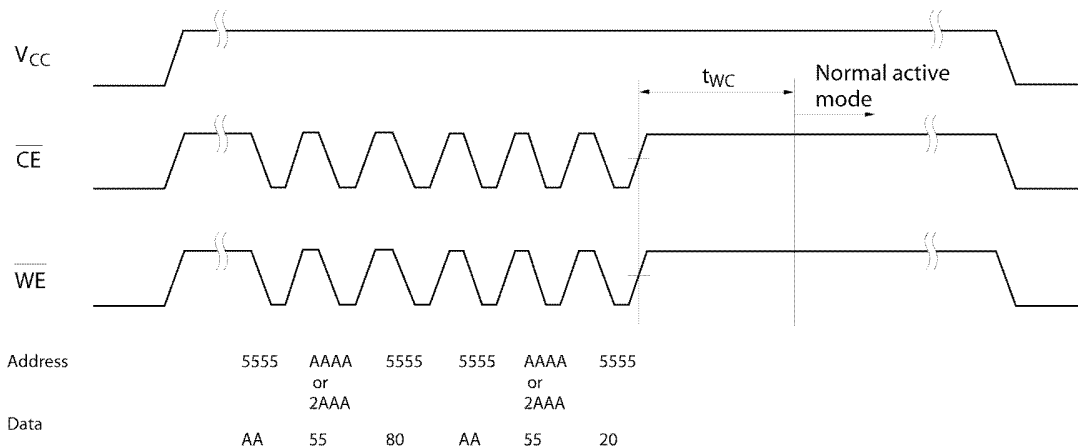


FIGURE 8. SOFTWARE DATA PROTECTION TIMING WAVEFORM(2) (IN NON-PROTECTION MODE)



Toggle Bit Waveform

EEPROM APPLICATION NOTES

This application note describes the programming procedures for each EEPROM module (four in each MCM) and details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows from 1 to 128 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window opens 30 μ s for the second byte. In the same manner each additional byte of data can be loaded within 30 μ s. In case \overline{CE} and \overline{WE} are kept high for 100 μ s after data input, the EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

\overline{WE} \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

\overline{Data} Polling

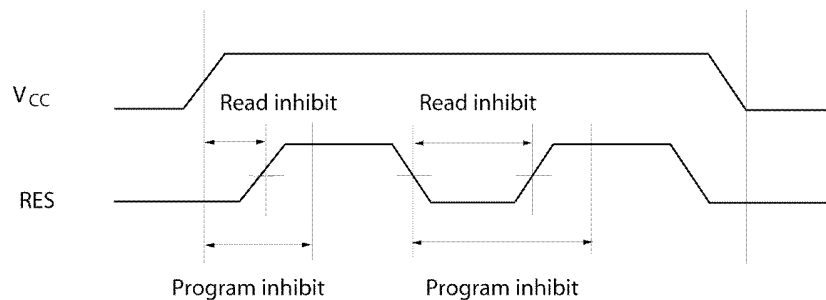
Data Polling function allows the status of the EEPROM to be determined. If the EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded output is from I/O 7 to indicate that the EEPROM is performing a write operation.

$\overline{RDY/Busy}$ Signal

$\overline{RDY/Busy}$ signal also allows a comparison operation to determine the status of the EEPROM. The $\overline{RDY/Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the $\overline{RDY/Busy}$ signal changes state to high impedance.

\overline{RES} Signal

When \overline{RES} is LOW, the EEPROM cannot be read and programmed. Therefore, data can be protected by keeping \overline{RES} low when V_{CC} is switched. \overline{RES} should be kept high during read and programming because it doesn't provide a latch function.

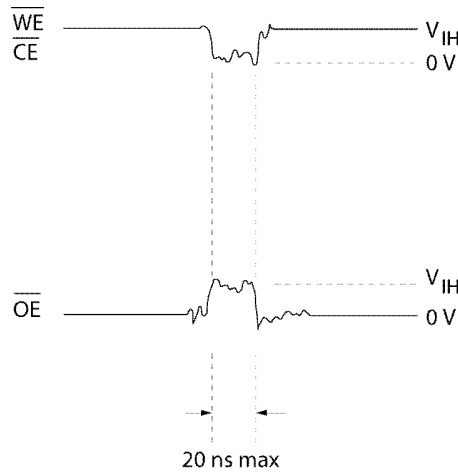


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

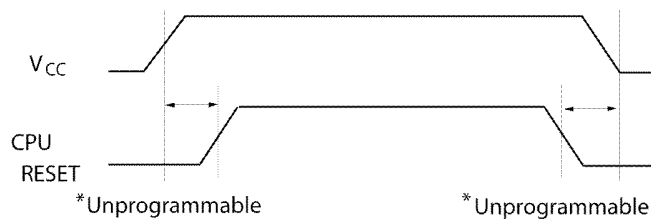
1. Data Protection against Noise of Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation.

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.

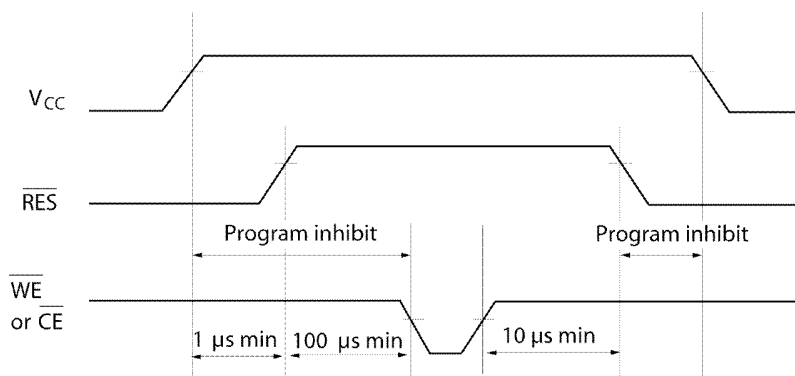


2. Data Protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to RES pin.

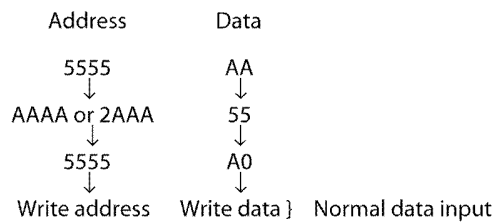


\overline{RES} should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when \overline{RES} becomes low, programming operation doesn't finish correctly in case that \overline{RES} falls low during programming operation. \overline{RES} should be kept high for 10 ms after the last data input.

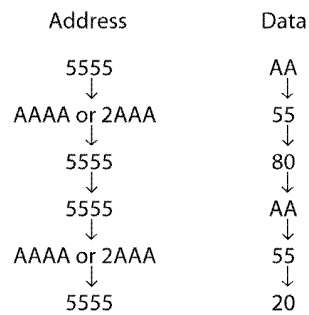


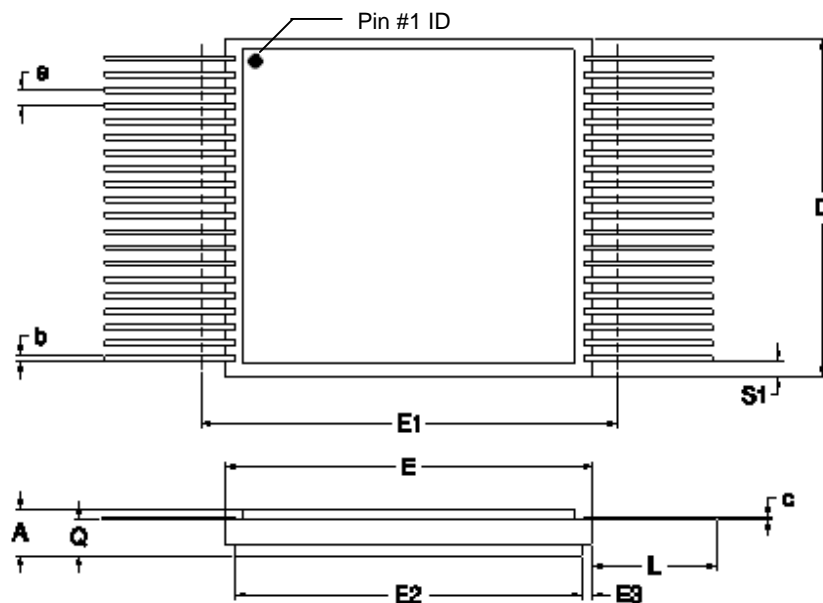
3. Software Data Protection

The software data protection function is to prevent unintentional programming caused by noise generated by external circuits. In software data protection mode, 3 bytes of data must be input before write data as follows. These bytes can switch the non-protection mode to the protection mode.



Software data protection mode can be canceled by inputting the following 6 bytes. Then, the EEPROM turns to the non-protection mode and can write data normally. However, when the data is input in the canceling cycle, the data cannot be written.





79C0408 RAD-PAK® AND XRAY-PAK™ PACKAGE DIMENSIONS

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.248	0.274	0.300
b	0.013	0.015	0.022
c	0.006	0.008	0.010
D	--	0.850	0.860
E	0.985	0.995	1.005
E1	--	--	1.025
E2	0.890	0.895	--
E3	0.000	0.050	--
e	0.040 BSC		
L	0.380	0.390	0.400
Q	0.214	0.245	0.270
S1	0.005	0.038	--
N	40		

F40-01

Note: All dimensions in inches

4 Megabit (512k x 8-bit) EEPROM MCM

79C0408

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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4 Megabit (512k x 8-bit) EEPROM MCM

79C0408

Product Ordering Options

