93AA46/56/66

1K/2K/4K 1.8V Microwire® Serial EEPROM

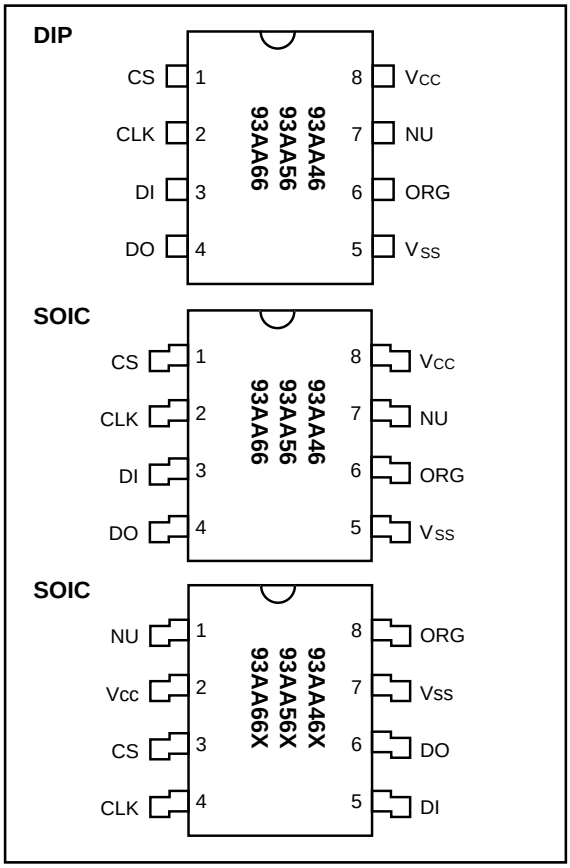
FEATURES

- Single supply with programming operation down to 1.8V
- Low power CMOS technology
  - 70 μA typical active READ current at 1.8V
  - 2 μA typical standby current at 1.8V
- ORG pin selectable memory configuration
  - 128 x 8- or 64 x 16-bit organization (93AA46)
  - 256 x 8- or 128 x 16-bit organization (93AA56)
  - 512 x 8 or 256 x 16 bit organization (93AA66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 10,000,000 ERASE/WRITE cycles guaranteed on 93AA56 and 93AA66
- 1,000,000 E/W cycles guaranteed on 93AA46
- Data retention > 200 years
- 8-pin PDIP/SOIC (SOIC in JEDEC and EIAJ standards)
- Temperature ranges supported
  - Commercial (C): 0°C to +70°C

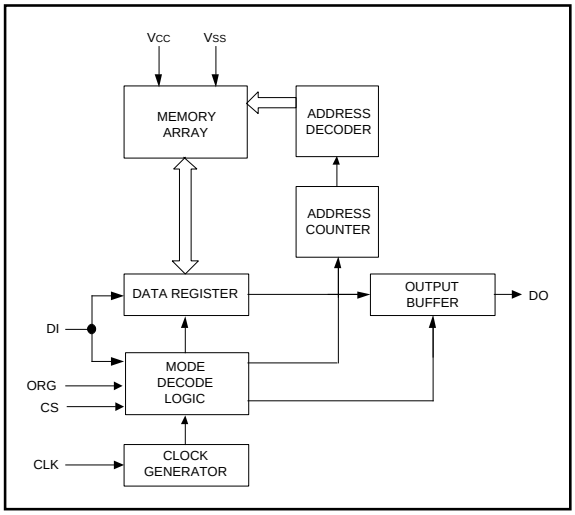
DESCRIPTION

The Microchip Technology Inc. 93AA46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93AA Series is available in standard 8-pin DIP and surface mount SOIC packages. The rotated pin-out 93AA46X/56X/66X are offered in the “SN” package only.

PACKAGE TYPES



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings

VCC 7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature.....-65˚C to +150˚C
Ambient temp. with power applied.....-65˚C to +125˚C
Soldering temperature of leads (10 seconds).....+300˚C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Configuration
NU	Not Utilized
VCC	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

			VCC = +1.8V to +5.5V		Commercial (C): Tamb = 0˚C to +70˚C	
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	—	VCC+1	V	VCC ≥ 2.7V
	VIH2	0.7 VCC	—	VCC+1	V	VCC < 2.7V
Low level input voltage	VIL1	-0.3	—	0.8	V	VCC ≥ 2.7V
	VIL2	-0.3	—	0.2 VCC	V	VCC < 2.7V
Low level output voltage	VOL1	—	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	—	0.2	V	IOL = 100µA; VCC = 1.8V
High level output voltage	VOH1	2.4	—	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	—	V	IOH = -100 µA; VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	—	7	pF	VIN/VOUT = 0V (Note 1 & 2) Tamb = +25˚C, FCLK = 1 MHz
Operating current	ICC write	—	—	3	mA	FCLK=2 MHz; VCC=5.5V (Note 2)
	ICC read	—	—	1	mA	FCLK = 2 MHz; VCC = 5.5V
				500	µA	FCLK = 1 MHz; VCC = 3.0V
			70		µA	FCLK = 1 MHz; VCC = 1.8V
Standby current	ICCS			100	µA	CLK = CS = 0V; VCC = 5.5V
				30	µA	CLK = CS = 0V; VCC = 3.0V
			2		µA	CLK = CS = 0V; VCC = 1.8V
Clock frequency	FCLK			2	MHz	VCC ≥ 4.5V
				1	MHz	VCC < 4.5V
Clock high time	TCKH	250			ns	
Clock low time	TCKL	250			ns	
Chip select setup time	TCSS	50			ns	Relative to CLK
Chip select hold time	TCSH	0			ns	Relative to CLK
Chip select low time	TCSL	250			ns	
Data input setup time	TDIS	100			ns	Relative to CLK
Data input hold time	TDIH	100			ns	Relative to CLK
Data output delay time	TPD			400	ns	CL = 100 pF
Data output disable time	TCZ			100	ns	CL = 100 pF (Note 2)
Status valid time	TSV			500	ns	CL = 100 pF
Program cycle time	TWC		4	10	ms	ERASE/WRITE mode
	TEC		8	15	ms	ERAL mode (Vcc = 5V ± 10%)
	TWL		16	30	ms	WRAL mode (Vcc = 5V ± 10%)
Endurance						
93AA46	—	1M	—	1M	—	25°C, Vcc = 5.0V, Block Mode
93AA56/66	—	10M	—	10M	—	(Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

TABLE 1-3: INSTRUCTION SET FOR 93AA46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

TABLE 1-4: INSTRUCTION SET FOR 93AA46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-5: INSTRUCTION SET FOR 93AA56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93AA56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

TABLE 1-7: INSTRUCTION SET FOR 93AA66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-8: INSTRUCTION SET FOR 93AA66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when VCC has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

2.4 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

2.5 Erase/Write Enable and Disable (EWEN,EWDS)

The 93AA46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.6 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word typical.

2.7 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word typical.

2.8 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire write cycle is complete.

The ERAL cycle takes (8 ms typical).

2.9 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

The WRAL cycle takes 16 ms typical.

FIGURE 2-1: SYNCHRONOUS DATA TIMING

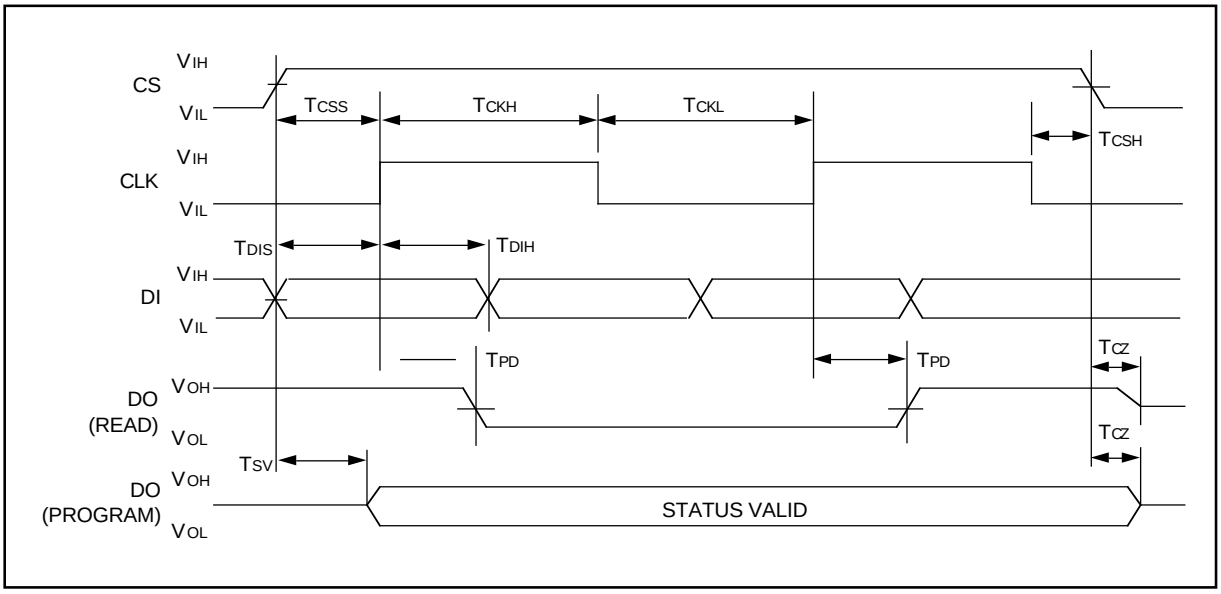
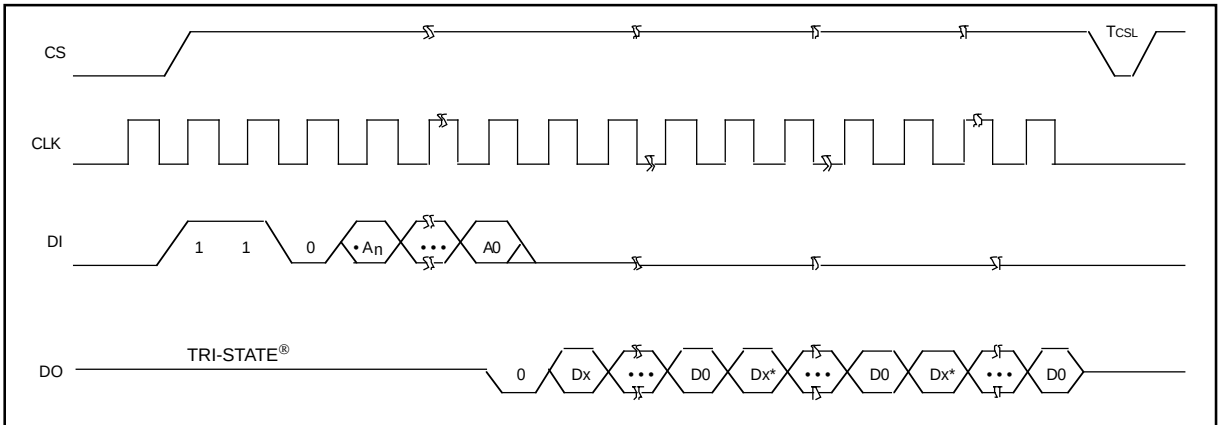


FIGURE 2-2: READ TIMING



Tri-State is a registered trademark of National Semiconductor Incorporated.

FIGURE 2-3: EWEN TIMING

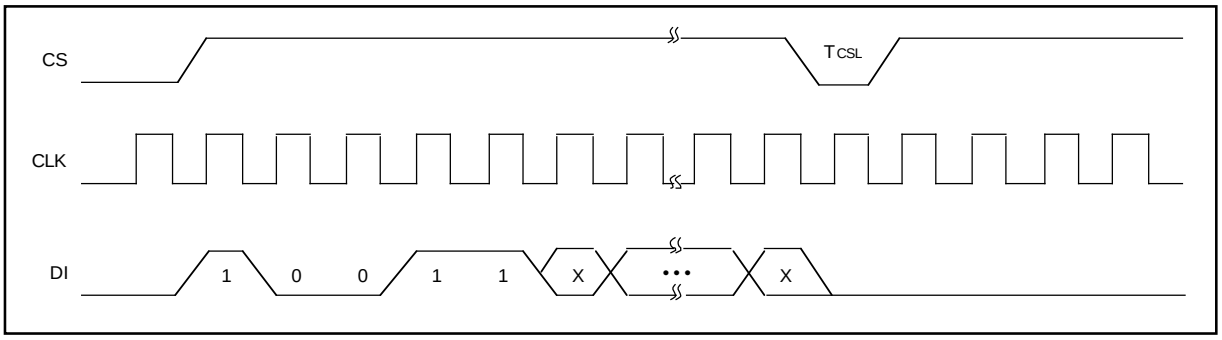


FIGURE 2-4: EWDS TIMING

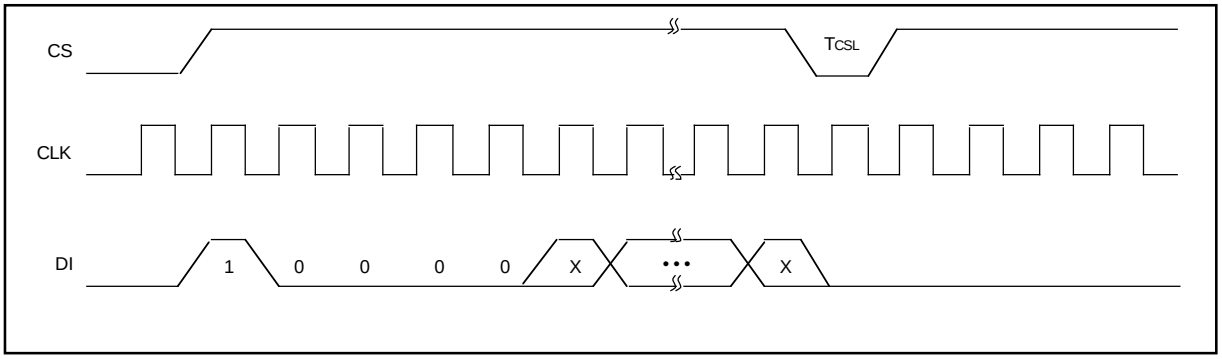


FIGURE 2-5: WRITE TIMING

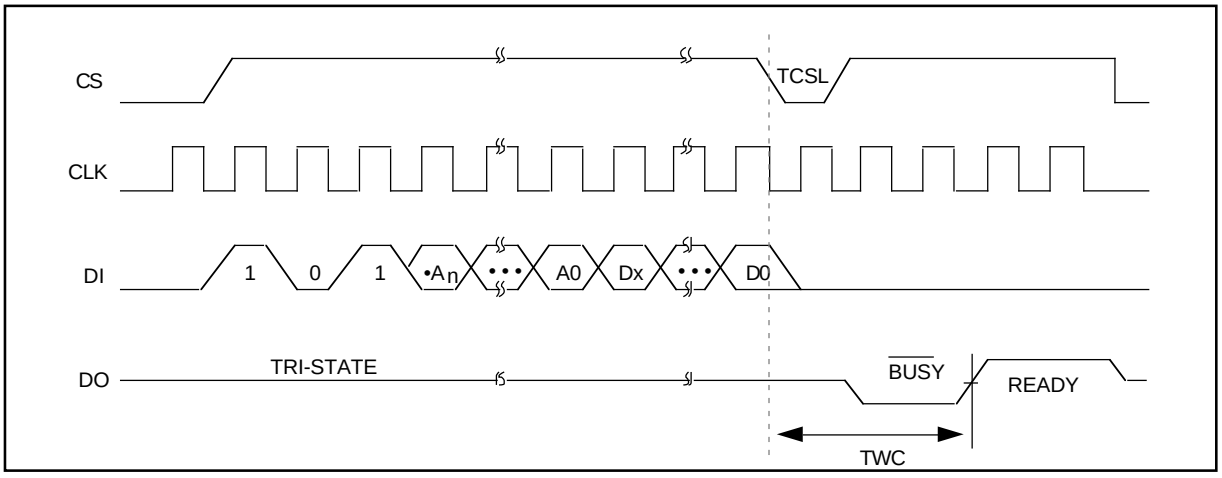
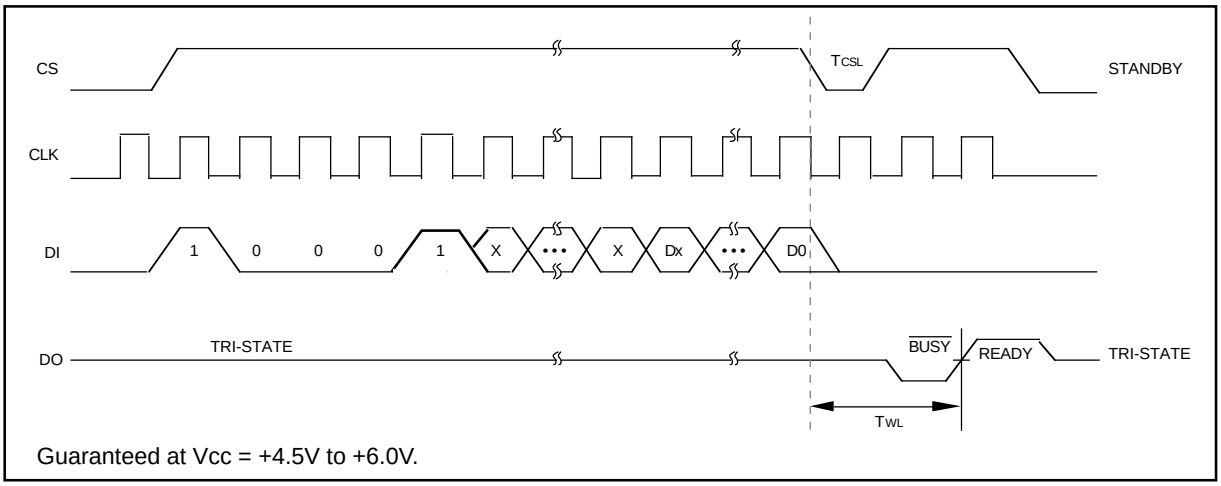


FIGURE 2-6: WRAL TIMING



Guaranteed at Vcc = +4.5V to +6.0V.

FIGURE 2-7: ERASE TIMING

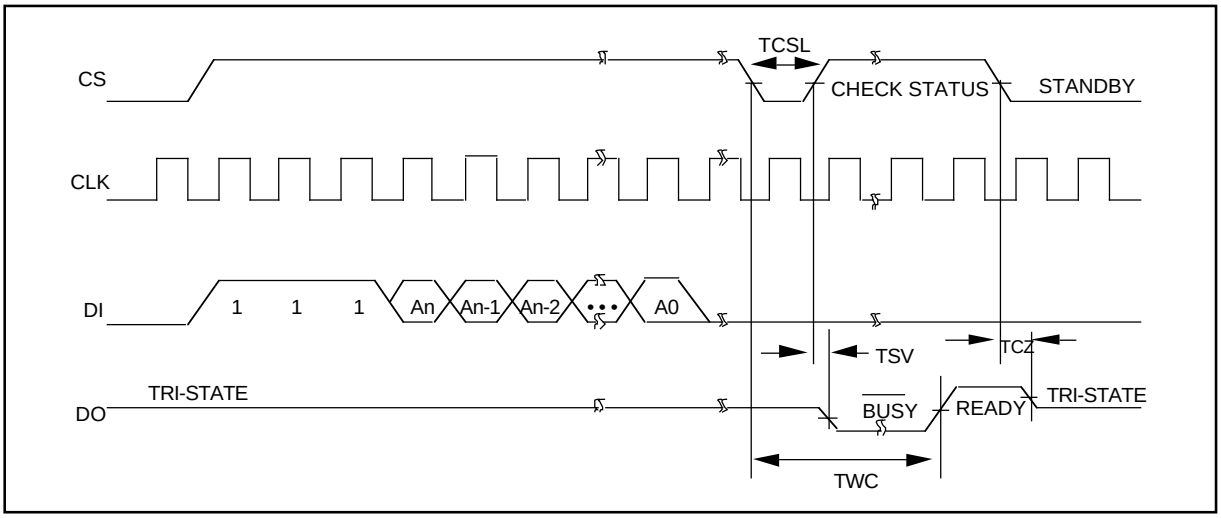
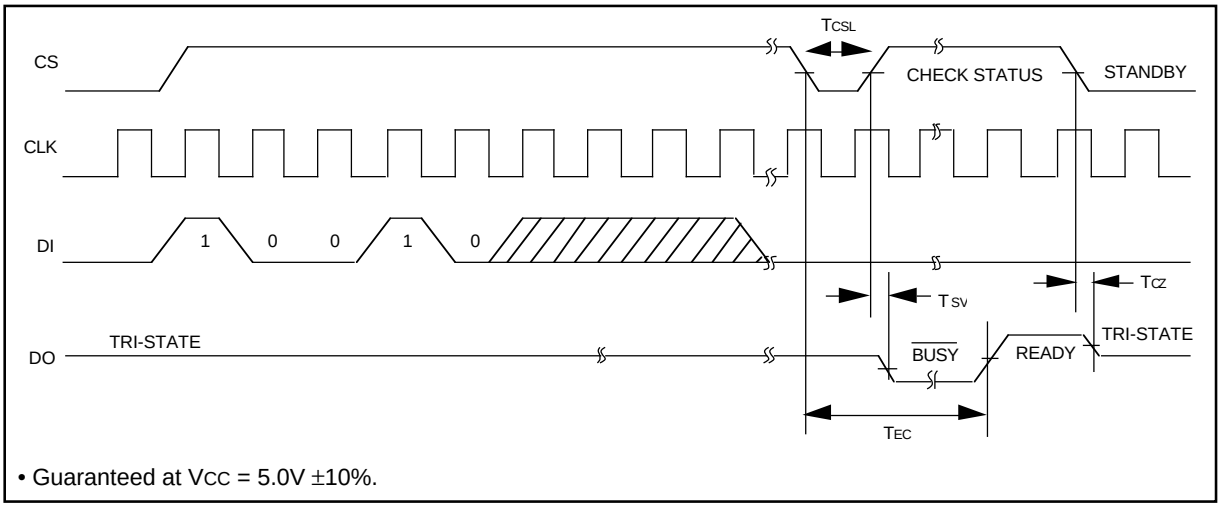


FIGURE 2-8: ERAL TIMING



• Guaranteed at VCC = 5.0V ±10%.

3.0 PIN DESCRIPTION

3.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AAXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a “Don't Care” if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note:	CS must go LOW between consecutive instructions.

3.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

3.5 Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to VCC or VSS.

NOTES:

NOTES:

93AA46/56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93AA46/56/66 - /P

Package:		P =	Plastic DIP (300 mil Body), 8-lead
		SN =	Plastic SOIC (150 mil Body), 8-lead
		SM =	Plastic SOIC (207 mil Body), 8-lead (93AA46/56/66)
Temperature Range:		Blank =	0°C to +70°C
Device:	93AA46/56/66		Microwire Serial EEPROM
	93AA46/56/66X		Microwire Serial EEPROM in alternate pinouts (SN package only)
	93AA46T/56T/66T		Microwire Serial EEPROM (Tape and Reel)
	93AA46XT/56XT/66XT		Microwire Serial EEPROM (Tape and Reel)

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