101-084

MICROCHIP

PIC17C75X

High-Performance 8-Bit CMOS EPROM Microcontrollers

Devices included in this data sheet:

- PIC17C752
- PIC17C756

Microcontroller Core Features:

- Only 58 single word instructions to learn
- All single cycle instructions (121 ns) except for program branches and table reads/writes which are two-cycle
- Operating speed
- ★ - DC - 33 MHz clock input
  - DC - 121 ns instruction cycle

Device	Memory	
	Program (x16)	Data (x8)
PIC17C752	8K	454
PIC17C756	16K	902

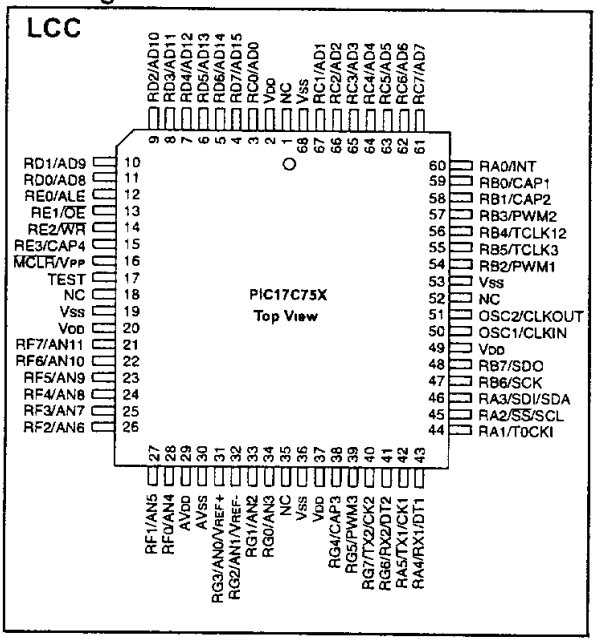
- ★ Hardware Multiplier
- Interrupt capability
- 16 level deep hardware stack
- Direct, indirect, and relative addressing modes
- Internal/external program memory execution
- Capable of addressing 64K x 16 program memory space

Peripheral Features:

- 50 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - RA2 and RA3 are open drain, high voltage (12V), high current (60 mA), I/O pins
- Four capture input pins
  - Captures are 16-bit, max resolution 121 ns
- Three PWM outputs
  - PWM resolution is 1- to 10-bits
- TMR0 16-bit timer/counter with 8-bit programmable prescaler
- TMR1 8-bit timer/counter
- TMR2 8-bit timer/counter
- TMR3 16-bit timer/counter
- Two Universal Synchronous Asynchronous Receiver Transmitters (USART/SCI)
  - Independant baud rate generators
- 10-bit, 12 channel analog-to-digital converter
- Synchronous Serial Port (SSP) with SPI™ and I^2C™ modes (including I^2C master mode)

Pin Diagrams

LCC



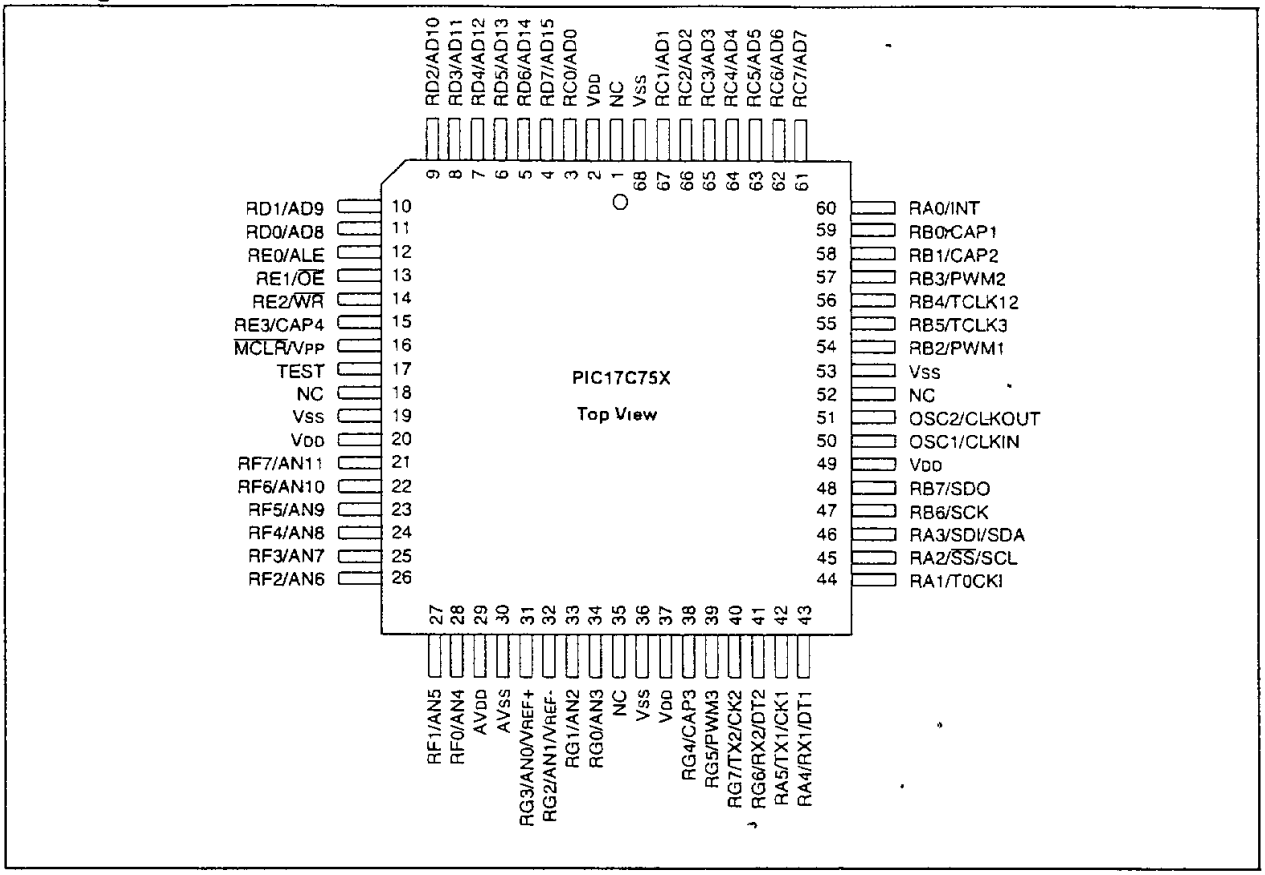
Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Brown-out Reset
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

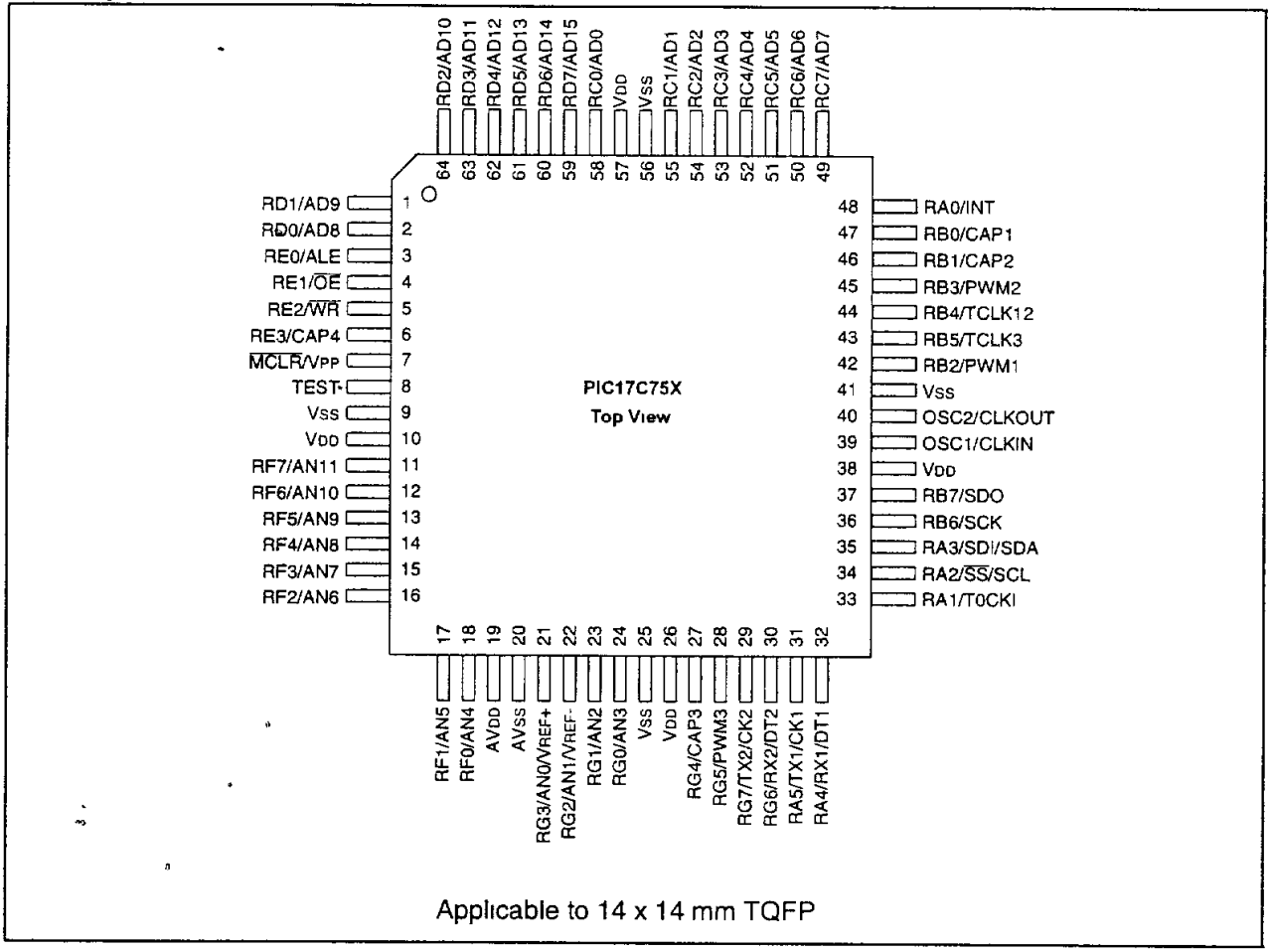
CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range (2.5V to 6.0V)
- Commercial and Industrial temperature ranges
- Low-power consumption
  - < 5 mA @ 5V, 4 MHz
  - 100 µA typical @ 4.5V, 32 kHz
  - < 1 µA typical standby current @ 5V

Pin Diagrams Cont.'d PIC17C75X IN 68-PIN LCC

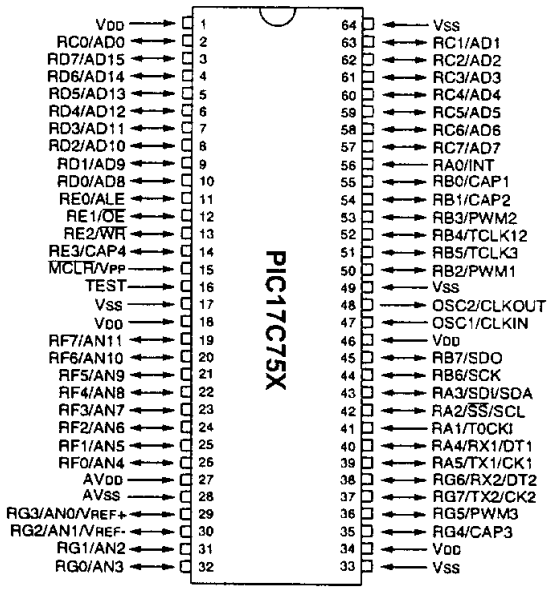


Pin Diagrams Cont.'d PIC17C75X IN 64-PIN TQFP



Applicable to 14 x 14 mm TQFP

Pin Diagrams Cont.'d PIC17C75X IN 64-PIN Y-SHRINK DIP



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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

1.0 OVERVIEW

This data sheet covers the PIC17C75X group of the PIC17CXXX family of microcontrollers The following devices are discussed in this data sheet.

- PIC17C752
- PIC17C756

The PIC17C75X devices are 68-Pin, EPROM-based members of the versatile PIC17CXXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers

All PIC16/17 microcontrollers employ an advanced RISC architecture The PIC17CXXX has enhanced core features, 16-level deep stack, and multiple internal and external interrupt sources The separate instruction and data buses of the Harvard architecture allow a 16-bit wide instruction word with a separate 8-bit wide data path The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles) A total of 58 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance For mathematical intensive applications all devices have a single cycle 8 x 8 Hardware Multiplier

PIC17CXXX microcontrollers typically achieve a 2 1 code compression and a 4 1 speed improvement over other 8-bit microcontrollers in their class

PIC17C75X devices have up to 902 bytes of RAM and 50 I/O pins In addition, the PIC17C75X adds several peripheral features useful in many high performance applications including

- Four timer/counters
- Four capture inputs
- Three PWM outputs
- Two independant Universal Synchronous Asynchronous Receiver Transmitters (USARTs)
- An A/D converter (12 channel, 10-bit resolution)
- A Synchronous Serial Port (SPI and I^2C w/ Master mode)

These special features reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption

There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LF oscillator is for low frequency crystals and minimizes power consumption, XT is a standard crystal, and the EC is for external clock input.

The SLEEP (power-down) mode offers additional power saving Wake-up from SLEEP can occur through several external and internal interrupts and device resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software malfunction

There are four configuration options for the device operational mode

- Microprocessor
- Microcontroller
- Extended microcontroller
- Protected microcontroller

The microprocessor and extended microcontroller modes allow up to 64K-words of external program memory

Brown-out Reset circuitry has also been added to the device This allows a device reset to occur if the device VDD falls below the Brown-out voltage trip point (BVDD) The chip will remain in Brown-out Reset until VDD rises above BVDD

Table 1-1 lists the features of the PIC17CXXX devices

A UV-erasable CERQUAD-packaged version (compatible with PLCC) is ideal for code development while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume

The PIC17C75X fits perfectly in applications that require extremely fast execution of complex software programs These include applications ranging from precise motor control and industrial process control to automotive, instrumentation, and telecom applications

The EPROM technology makes customization of application programs (with unique security codes, combinations, model numbers, parameter storage, etc) fast and convenient. Small footprint package options (including die sales) make the PIC17C75X ideal for applications with space limitations that require high performance

An In-circuit Serial Programming (ISP) feature allows

- Flexibility of programming the software code as one of the last steps of the manufacturing process

High speed execution, powerful peripheral features, flexible I/O, and low power consumption all at low cost make the PIC17C75X ideal for a wide range of embedded control applications

1.1 Family and Upward Compatibility

The PIC17CXXX family of microcontrollers have architectural enhancements over the PIC16C5X and PIC16CXX families These enhancements allow the device to be more efficient in software and hardware requirements Refer to Appendix A for a detailed list of enhancements and modifications Code written for PIC16C5X or PIC16CXX can be easily ported to PIC17CXXX devices (Appendix B).

1.2 Development Support

The PIC17CXXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a universal programmer, a "C" compiler, and fuzzy logic support tools For additional information see Section 19 0

TABLE 1-1: PIC17CXXX FAMILY OF DEVICES

Features		PIC17CR42	PIC17C42A	PIC17C43	PIC17CR43	PIC17C44	PIC17C752	PIC17C756
Maximum Frequency of Operation		33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Operating Voltage Range		2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	3.0 - 6.0V	3.0 - 6.0V
Program Memory (x16)	(EPROM)	-	16 K	4K	-	8K	8K	16K
	(ROM)	2K	-	-	4K	-	-	-
Data Memory (bytes)		232	232	454	454	454	454	902
Hardware Multiplier (8 x 8)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit postscaler)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		2	2	2	2	2	4	4
PWM outputs (up to 10-bit)		2	2	2	2	2	3	3
USART/SCI		1	1	1	1	1	2	2
A/D channels (10-bit)		-	-	-	-	-	12	12
SSP (SPI/I^2C w/Master mode)		-	-	-	-	-	Yes	Yes
Power-on Reset		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Interrupt Sources		11	11	11	11	11	18	18
Code Protect		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset		-	-	-	-	-	Yes	Yes
In-circuit Serial Programming		-	-	-	-	-	Yes	Yes
I/O Pins		33	33	33	33	33	50	50
I/O High Current Capability	Source	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA
	Sink	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)
Package Types		40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	64-pin DIP 68-pin LCC 68-pin TQFP	64-pin DIP 68-pin LCC 68-pin TQFP

Note 1 Pins RA2 and RA3 can sink up to 60 mA

2.0 DEVICE VARIETIES

Each device has a variety of frequency ranges and packaging options Depending on application and production requirements, the proper device option can be selected using the information in the PIC17C75X Product Selection System section at the end of this data sheet When placing orders, please use the "PIC17C75X Product Identification System" at the back of this data sheet to specify the correct part number When discussing the functionality of the device, memory technology and voltage range does not matter

There are three memory type options These are specified in the middle characters of the part number

1 **C**, as in PIC17**C**756 These devices have EPROM type memory
2 **CR**, as in PIC17**CR**756 These devices have ROM type memory
3 **F**, as in PIC17**F**756 These devices have Flash type memory

All these devices operate over the standard voltage range Devices are also offered which operate over an extended voltage range (and reduced frequency range) Table 2-1 shows all possible memory types and voltage range designators for a particular device These designators are in **bold** typeface

TABLE 2-1: DEVICE MEMORY VARIETIES

Memory Type	Voltage Range	
	Standard	Extended
EPROM	PIC17**C**XXX	PIC17**LC**XXX
ROM	PIC17**CR**XXX	PIC17**LCR**XXX
Flash	PIC17**F**XXX	PIC17**LF**XXX

Note: Not all memory technologies are available for a particular device.

2.1 UV Erasable Devices

The UV erasable version, offered in CERQUAD package, is optimal for prototype development and pilot programs

The UV erasable version can be erased and reprogrammed to any of the configuration modes Microchip's programming of the PIC17C75X Third party programmers also are available, refer to the *Third Party Guide* for a list of sources

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates

The OTP devices, packaged in plastic packages, permit the user to program them once In addition to the program memory, the configuration bits must be programmed

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory Certain code and prototype verification procedures apply before production shipments are available Please contact your local Microchip Technology sales office for more details

2.4 Serialized Quick-Turnaround Production (SQTP^{SM}) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers The serial numbers may be random, pseudo-random or sequential

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products

ROM devices do not allow serialization information in the program memory space

For information on submitting ROM code, please contact your regional sales office

Note:	Presently, NO ROM versions of the PIC17C75X devices are available.

2.6 Flash Memory Devices

These devices are electrically erasable and, therefore, can be offered in the low cost plastic package Being electrically erasable, these devices can be erased and reprogrammed in-circuit These devices are the same for prototype development, pilot programs, as well as production

Note:	Presently, NO Flash versions of the PIC17C75X devices are available.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17CXXX can be attributed to a number of architectural features commonly found in RISC microprocessors To begin with, the PIC17CXXX uses a modified Harvard architecture. This architecture has the program and data accessed from separate memories So, the device has a program memory bus and a data memory bus This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory (accesses over the same bus) Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word PIC17CXXX opcodes are 16-bits wide, enabling single word instructions The full 16-bit wide program memory bus fetches a 16-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions Consequently, all instructions execute in a single cycle (121 ns @ 33 MHz), except for program branches and two special instructions that transfer data between program and data memory

The PIC17CXXX can address up to 64K x 16 of program memory space

The **PIC17C752** integrates 8K x 16 of EPROM program memory on-chip

The **PIC17C756** integrates 16K x 16 EPROM program memory

Program execution can be internal only (microcontroller or protected microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode) Extended microcontroller mode does not allow code protection

The PIC17CXXX can directly or indirectly address its register files or data memory All special function registers, including the Program Counter (PC) and Working Register (WREG), are mapped in the data memory The PIC17CXXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17CXXX simple yet efficient. In addition, the learning curve is reduced significantly

One of the PIC17CXXX family architectural enhancements from the PIC16CXX family allows two file registers to be used in some two operand instructions. This allows data to be moved directly between two registers without going through the WREG register Thus increasing performance and decreasing program memory usage

The PIC17CXXX devices contain an 8-bit ALU and working register The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations Unless otherwise mentioned, arithmetic operations are two's complement in nature

The WREG register is an 8-bit working register used for ALU operations

All PIC17C75X devices have an 8 x 8 hardware multiplier This multiplier generates a 16-bit result in a single cycle

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the ALUSTA register The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction See the SUBLW and SUBWF instructions for examples

Although the ALU does not perform signed arithmetic, the Overflow bit (OV) can be used to implement signed math Signed arithmetic is comprised of a magnitude and a sign bit The overflow bit indicates if the magnitude overflows and causes the sign bit to change state That is if the result of the signed operation is greater then 128 (7Fh) or less then -127 (FFh) Signed math can have greater than 7-bit values (magnitude), if more than one byte is used The use of the overflow bit only operates on bit6 (MSb of magnitude) and bit7 (sign bit) of the value in the ALU That is, the overflow bit is not useful if trying to implement signed math where the magnitude, for example, is 11-bits If the signed math values are greater than 7-bits (15-, 24- or 31-bit), the algorithm must ensure that the low order bytes ignore the overflow status bit

Care should be taken when adding and subtracting signed numbers to ensure that the correct operation is executed. Example 3-1 shows an item that must be taken into account when doing signed arithmetic on an ALU which operates as an unsigned machine.

EXAMPLE 3-1: SIGNED MATH

Hex Value	Signed Value Math	Unsigned Value Math
FFh	-127	255
+ 01h	+ 1	+ 1
= ?	= -126 (FEh)	= 0 (00h), Carry bit = 1

Signed math requires the result to be FEh (-126) This would be accomplished by subtracting one as opposed to adding one

A simplified block diagram is shown in Figure 3-1 The descriptions of the device pins are listed in Table 3-1

FIGURE 3-1: PIC17C75X BLOCK DIAGRAM

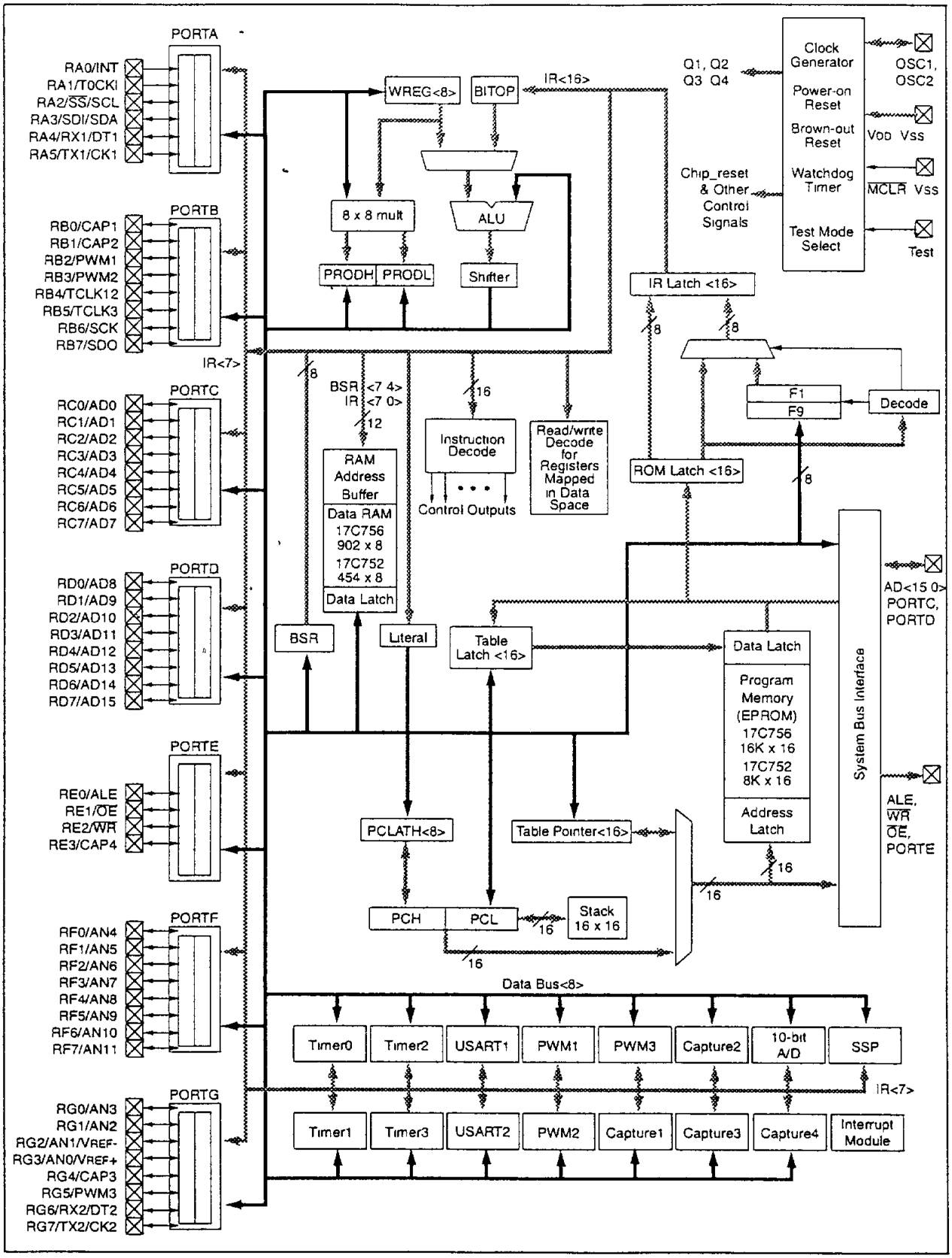


TABLE 3-1: PINOUT DESCRIPTIONS

Name	DIP No.	PLCC No.	TQFP No	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	47	50	39	I	ST	Oscillator input in crystal/resonator or RC oscillator mode External clock input in external clock mode
OSC2/CLKOUT	48	51	40	O	—	Oscillator output Connects to crystal or resonator in crystal oscillator mode In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency (FOSC/4) of OSC1 and denotes the instruction cycle rate
$\overline{MCLR}$/VPP	15	16	7	I/P	ST	Master clear (reset) input or Programming Voltage (VPP) input This is the active low reset input to the chip
						PORTA is a bi-directional I/O Port except for RA0 and RA1 which are input only
RA0/INT	56	60	48	I	ST	RA0 can also be selected as an external interrupt input Interrupt can be configured to be on positive or negative edge
RA1/T0CKI	41	44	33	I	ST	RA1 can also be selected as an external interrupt input, and the interrupt can be configured to be on positive or negative edge RA1 can also be selected to be the clock input to the Timer0 timer/counter
RA2/$\overline{SS}$/SCL	42	45	34	I/O	ST	RA2 can also be used as the slave select input for the SPI or the clock input for the I^2C bus High voltage, high current, open drain input/output port pin
RA3/SDI/SDA	43	46	35	I/O	ST	RA3 can also be used as the data input for the SPI or the data for the I^2C bus High voltage, high current, open drain input/output port pin
RA4/RX1/DT1	40	43	32	I/O †	ST	RA4 can also be selected as the USART1 (SCI) Asynchronous Receive or USART1 (SCI) Synchronous Data
RA5/TX1/CK1	39	42	31	I/O †	ST	RA5 can also be selected as the USART1 (SCI) Asynchronous Transmit or USART1 (SCI) Synchronous Clock
						PORTB is a bi-directional I/O Port with software configurable weak pull-ups
RB0/CAP1	55	59	47	I/O	ST	RB0 can also be the Capture1 input pin
RB1/CAP2	54	58	46	I/O	ST	RB1 can also be the Capture2 input pin
RB2/PWM1	50	54	42	I/O	ST	RB2 can also be the PWM1 output pin
RB3/PWM2	53	57	45	I/O	ST	RB3 can also be the PWM2 output pin
RB4/TCLK12	52	56	44	I/O	ST	RB4 can also be the external clock input to Timer1 and Timer2.
RB5/TCLK3	51	55	43	I/O	ST	RB5 can also be the external clock input to Timer3
RB6/SCK	44	47	36	I/O	ST	RB6 can also be used as the master/slave clock for the SPI
RB7/SDO	45	48	37	I/O	ST	RB7 can also be used as the data output for the SPI

Legend I = Input only, O = Output only, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

† The output is only available by the Peripheral operation

TABLE 3-1: PINOUT DESCRIPTIONS

Name	DIP No	PLCC No.	TQFP No	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O Port
RC0/AD0	2	3	58	I/O	TTL	This is also the least significant byte (LSB) of the 16-bit wide system bus in microprocessor mode or extended microcontroller mode In multiplexed system bus configuration, these pins are address output as well as data input or output
RC1/AD1	63	67	55	I/O	TTL	
RC2/AD2	62	66	54	I/O	TTL	
RC3/AD3	61	65	53	I/O	TTL	
RC4/AD4	60	64	52	I/O	TTL	
RC5/AD5	58	63	51	I/O	TTL	
RC6/AD6	58	62	50	I/O	TTL	
RC7/AD7	57	61	49	I/O	TTL	
						PORTD is a bi-directional I/O Port
RD0/AD8	10	11	2	I/O	TTL	This is also the most significant byte (MSB) of the 16-bit system bus in microprocessor mode or extended microprocessor mode or extended microcontroller mode In multiplexed system bus configuration these pins are address output as well as data input or output
RD1/AD9	9	10	1	I/O	TTL	
RD2/AD10	8	9	64	I/O	TTL	
RD3/AD11	7	8	63	I/O	TTL	
RD4/AD12	6	7	62	I/O	TTL	
RD5/AD13	5	6	61	I/O	TTL	
RD6/AD14	4	5	60	I/O	TTL	
RD7/AD15	3	4	59	I/O	TTL	
						PORTE is a bi-directional I/O Port
RE0/ALE	11	12	3	I/O	TTL	In microprocessor mode or extended microcontroller mode, RE0 is the Address Latch Enable (ALE) output Address should be latched on the falling edge of ALE output
RE1/$\overline{OE}$	12	13	4	I/O	TTL	In microprocessor or extended microcontroller mode, RE1 is the Output Enable ($\overline{OE}$) control output (active low)
RE2/$\overline{WR}$	13	14	5	I/O	TTL	In microprocessor or extended microcontroller mode, RE2 is the Write Enable ($\overline{WR}$) control output (active low)
RE3/CAP4	14	15	6	I/O	ST	RE3 can also be the Capture4 input pin
						PORTF is a bi-directional I/O Port
RF0/AN4	26	28	18	I/O	ST	RF0 can also be analog input 4
RF1/AN5	25	27	17	I/O	ST	RF1 can also be analog input 5
RF2/AN6	24	26	16	I/O	ST	RF2 can also be analog input 6
RF3/AN7	23	25	15	I/O	ST	RF3 can also be analog input 7
RF4/AN8	22	24	14	I/O	ST	RF4 can also be analog input 8
RF5/AN9	21	23	13	I/O	ST	RF5 can also be analog input 9
RF6/AN10	20	22	12	I/O	ST	RF6 can also be analog input 10
RF7/AN11	19	21	11	I/O	ST	RF7 can also be analog input 11

Legend I = Input only, O = Output only, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

† The output is only available by the Peripheral operation.

TABLE 3-1: PINOUT DESCRIPTIONS

Name	DIP No	PLCC No	TQFP No	I/O/P Type	Buffer Type	Description
						PORTG is a bi-directional I/O Port
RG0/AN3	32	34	24	I/O	ST	RG0 can also be analog input 3
RG1/AN2	31	33	23	I/O	ST	RG1 can also be analog input 2
RG2/AN1/VREF-	30	32	22	I/O	ST	RG2 can also be analog input 1, or the ground reference voltage
RG3/AN0/VREF+	29	31	21	I/O	ST	RG3 can also be analog input 0, or the positive reference voltage
RG4/CAP3	35	38	27	I/O	ST	RG4 can also be the Capture3 input pin
RG5/PWM3	36	39	28	I/O	ST	RG5 can also be the PWM3 output pin
RG6/RX2/DT2	38	41	30	I/O	ST	RG6 can also be selected as the USART2 (SCI) Asynchronous Receive or USART2 (SCI) Synchronous Data
RG7/TX2/CK2	37	40	29	I/O	ST	RG7 can also be selected as the USART2 (SCI) Asynchronous Transmit or USART2 (SCI) Synchronous Clock
TEST	16	17	8	I	ST	Test mode selection control input Always tie to VSS for normal operation
VSS	17, 33, 49, 64	19, 36,53, 68	9, 25, 41, 56	P		Ground reference for logic and I/O pins
VDD	1, 18, 34, 46	2, 20, 37, 49,	10, 26, 38, 57	P		Positive supply for logic and I/O pins
AVSS	28	30	20	P		Ground reference for A/D converter This pin **MUST** be at the same potential as VSS
AVDD	27	29	19	P		Positive supply for A/D converter This pin **MUST** be at the same potential as VDD
NC	-	1, 18, 35, 52	-			No Connect Leave these pins unconnected

Legend: I = Input only, O = Output only, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input.

† The output is only available by the Peripheral operation.

NOTES:

4.0 ON-CHIP OSCILLATOR CIRCUIT

The internal oscillator circuit is used to generate the device clock Four device clock periods generate an internal instruction clock (TCY) There are four modes that the oscillator can operate in These are selected by the device configuration bits during device programming These modes are

- LF Low Frequency (FOSC <= 2 MHz)
- XT Standard Crystal/Resonator Frequency (2 MHz <= FOSC <= 33 MHz)
- EC External Clock Input (Default oscillator configuration)
- RC External Resistor/Capacitor (FOSC <= 4 MHz)

There are two timers that offer necessary delays on power-up One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode The user can wake from SLEEP through external reset, Watchdog Timer Reset or through an interrupt

Several oscillator options are made available to allow the part to fit the application The RC oscillator option saves system cost while the LF crystal option saves power Configuration bits are used to select various options.

4.1 Oscillator Configurations

4 1 1 OSCILLATOR TYPES

The PIC17CXXX can be operated in four different oscillator modes The user can program two configuration bits (FOSC1 FOSC0) to select one of these four modes

- LF Low Power Crystal
- XT Crystal/Resonator
- EC External Clock Input
- RC Resistor/Capacitor

The main difference between the LF and XT modes is the gain of the internal inverter of the oscillator circuit which allows the different frequency ranges

For more details on the device configuration bits, see Section 17.0

4 1 2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LF modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-2) The PIC17CXXX oscillator design requires the use of a parallel cut crystal Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications

For frequencies above 20 MHz, it is common for the crystal to be an overtone mode crystal Use of overtone mode crystals require a tank circuit to attenuate the gain at the fundamental frequency Figure 4-3 shows an example circuit

4 1 2 1 OSCILLATOR / RESONATOR START-UP

As the device voltage increases from Vss, the oscillator will start its oscillations The time required for the oscillator to start oscillating depends on many factors These include

- Crystal / resonator frequency
- Capacitor values used (C1 and C2)
- Device VDD rise time
- System temperature
- Series resistor value (and type) if used
- Oscillator mode selection of device (which selects the gain of the internal oscillator inverter)

Figure 4-1 shows an example of a typical oscillator / resonator start-up. The peak-to-peak voltage of the oscillator waveform can be quite low (less than 50% of device VDD) when the waveform is centered at VDD/2 (refer to parameter number D033 and D043 in the electrical specification section)

FIGURE 4-1: OSCILLATOR / RESONATOR START-UP CHARACTERISTICS

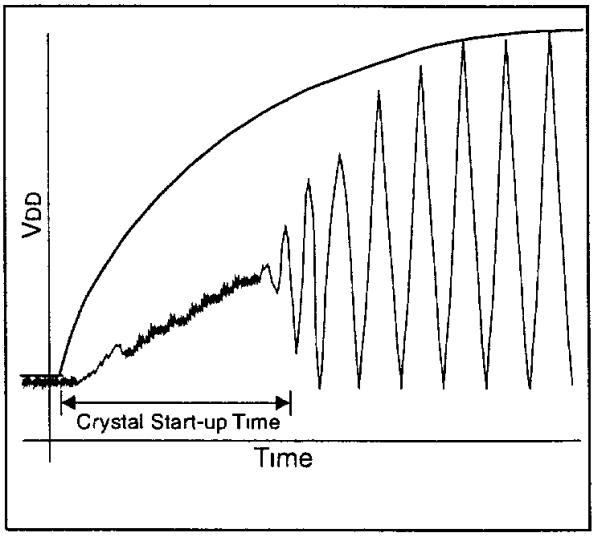
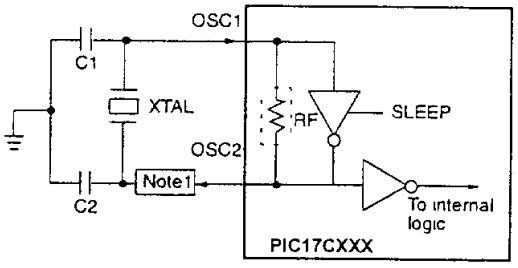


FIGURE 4-2: CRYSTAL OR CERAMIC RESONATOR OPERATION (XT OR LF OSC CONFIGURATION)



See Table 4-1 and Table 4-2 for recommended values of C1 and C2

Note 1 A series resistor (Rs) may be required for AT strip cut crystals

TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2 (1)
LF	455 kHz 2 0 MHz	15 - 68 pF 10 - 33 pF
XT	4 0 MHz 8.0 MHz 16 0 MHz	22 - 68 pF 33 - 100 pF 33 - 100 pF

Higher capacitance increases the stability of the oscillator but also increases the start-up time These values are for design guidance only Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components

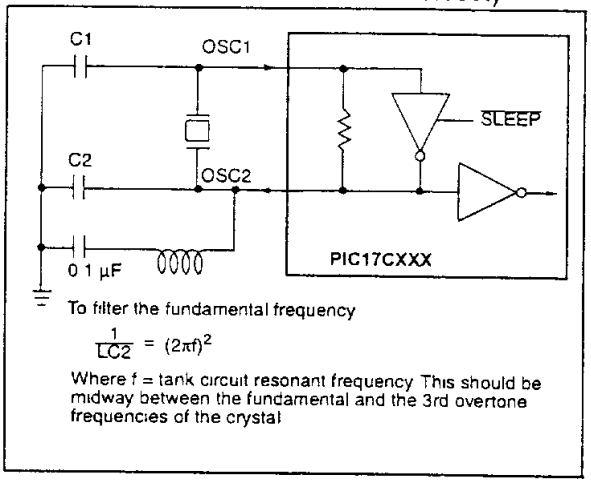
Note 1 These values include all board capacitances on this pin Actual capacitor value depends on board capacitance

Resonators Used:

455 kHz	Panasonic EFO-A455K04B	± 0 3%
2 0 MHz	Murata Erie CSA2 00MG	± 0 5%
4 0 MHz	Murata Erie CSA4 00MG	± 0 5%
8 0 MHz	Murata Erie CSA8 00MT	± 0 5%
16 0 MHz	Murata Erie CSA16 00MX	± 0 5%

Resonators used did not have built-in capacitors

FIGURE 4-3: CRYSTAL OPERATION, OVERTONE CRYSTALS (XT OSC CONFIGURATION)



To filter the fundamental frequency

$$\frac{1}{LC2} = (2\pi f)^2$$

Where f = tank circuit resonant frequency This should be midway between the fundamental and the 3rd overtone frequencies of the crystal

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1 (3)	C2 (3)
LF	32 kHz(1) 1 MHz 2 MHz	100-150 pF 10-33 pF 10-33 pF	100-150 pF 10-33 pF 10-33 pF
XT	2 MHz 4 MHz 8 MHz (2) 16 MHz 25 MHz 32 MHz (3)	47-100 pF 15-68 pF 15-47 pF TBD 15-47 pF 10	47-100 pF 15-68 pF 15-47 pF TBD 15-47 pF 10

Higher capacitance increases the stability of the oscillator but also increases the start-up time and the oscillator current These values are for design guidance only RS may be required in XT mode to avoid overdriving the crystals with low drive level specification Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values for external components

Note 1 For VDD > 4 5V, C1 = C2 ≈ 30 pF is recommended

2 RS of 330Ω is required for a capacitor combination of 15/15 pF

3 These values include all board capacitances on this pin. Actual capacitor value depends on board capacitance

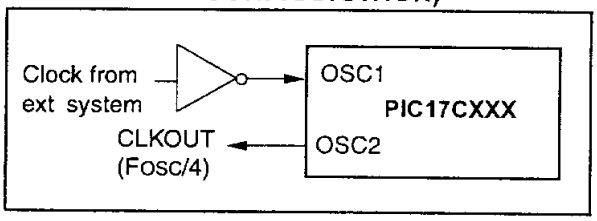
Crystals Used

32 768 kHz	Epson C-001R32 768K-A	± 20 PPM
1 0 MHz	ECS-10-13-1	± 50 PPM
2 0 MHz	ECS-20-20-1	± 50 PPM
4 0 MHz	ECS-40-20-1	± 50 PPM
8 0 MHz	ECS ECS-80-S-4 ECS-80-18-1	± 50 PPM
16 0 MHz	ECS-160-20-1	TBD
25 MHz	CTS CTS25M	± 50 PPM
32 MHz	CRYSTEK HF-2	± 50 PPM

4 1 3 EXTERNAL CLOCK OSCILLATOR

In the EC oscillator mode, the OSC1 input can be driven by CMOS drivers In this mode, the OSC1/CLKIN pin is hi-impedance and the OSC2/CLKOUT pin is the CLKOUT output (4 TOSC)

FIGURE 4-4: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)



4 1 4 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built Prepackaged oscillators provide a wide operating range and better stability A well-designed crystal oscillator will provide good performance with TTL gates Two types of crystal oscillator circuits can be used. one with series resonance, or one with parallel resonance

Figure 4-5 shows implementation of a parallel resonant oscillator circuit The circuit is designed to use the fundamental frequency of the crystal The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires The 4 7 kΩ resistor provides the negative feedback for stability The 10 kΩ potentiometer biases the 74AS04 in the linear region This could be used for external oscillator designs

FIGURE 4-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

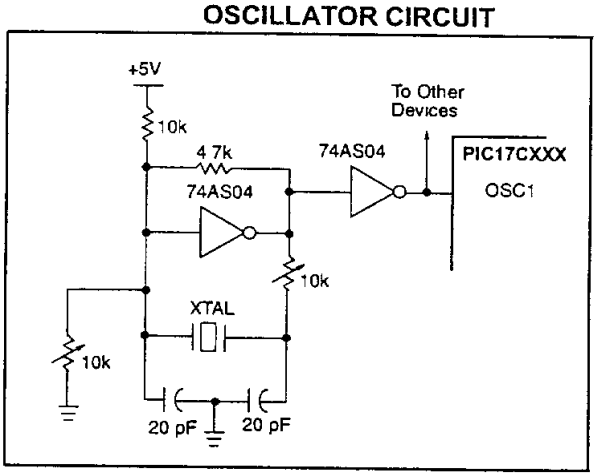
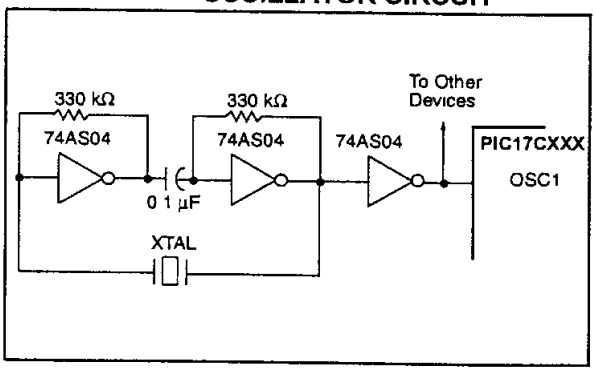


Figure 4-6 shows a series resonant oscillator circuit This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 4-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



4.1.5 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 4-7 shows how the R/C combination is connected to the PIC17CXXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

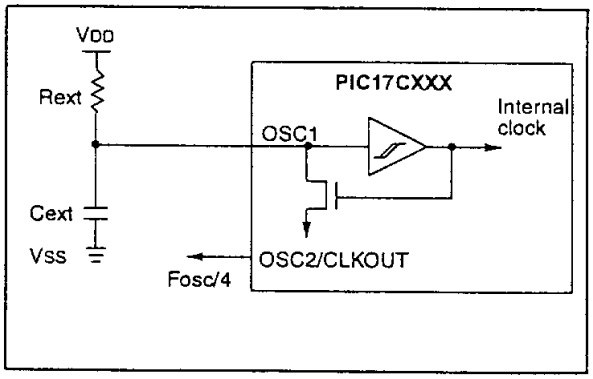
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 21.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 21.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 4-8 for waveform).

FIGURE 4-7: RC OSCILLATOR MODE



4.1.5.1 RC START-UP

As the device voltage increases, the RC will immediately start its oscillations once the pin voltage levels meet the input threshold specifications (parameter number D032 and D042 in the electrical specification section). The time required for the RC to start oscillating depends on many factors. These include:

- Resistor value used
- Capacitor value used
- Device VDD rise time
- System temperature

4.2 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3, and Q4 Internally, the program counter (PC) is incremented every Q1, and the instruction is fetched from the program memory and latched into the instruction register in Q4 The instruction is decoded and executed during the following Q1 through Q4 The clocks and instruction execution flow are shown in Figure 4-8.

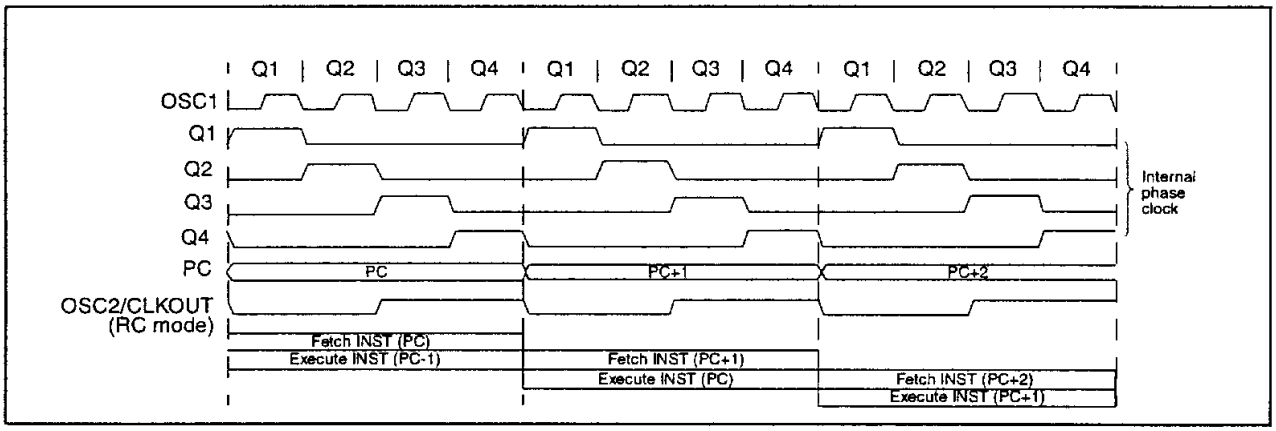
4.3 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4) The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle However, due to the pipelining, each instruction effectively executes in one cycle If an instruction causes the program counter to change (e g GOTO) then two cycles are required to complete the instruction (Example 4-1)

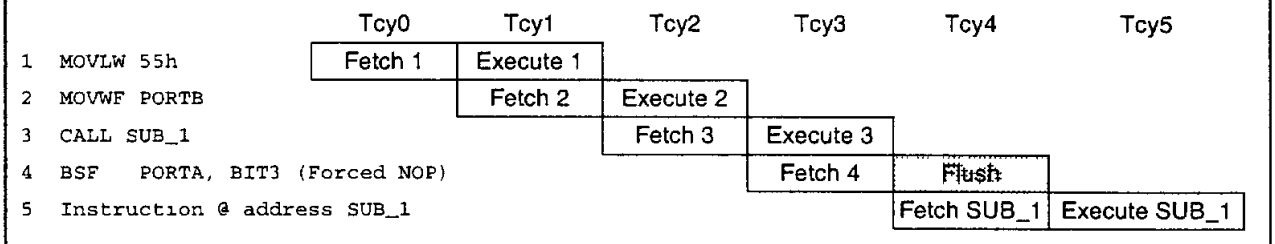
A fetch cycle begins with the program counter incrementing in Q1

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1 This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles Data memory is read during Q2 (operand read) and written during Q4 (destination write)

FIGURE 4-8: CLOCK/INSTRUCTION CYCLE



EXAMPLE 4-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed

NOTES:

5.0 RESET

The PIC17CXXX differentiates between various kinds of reset

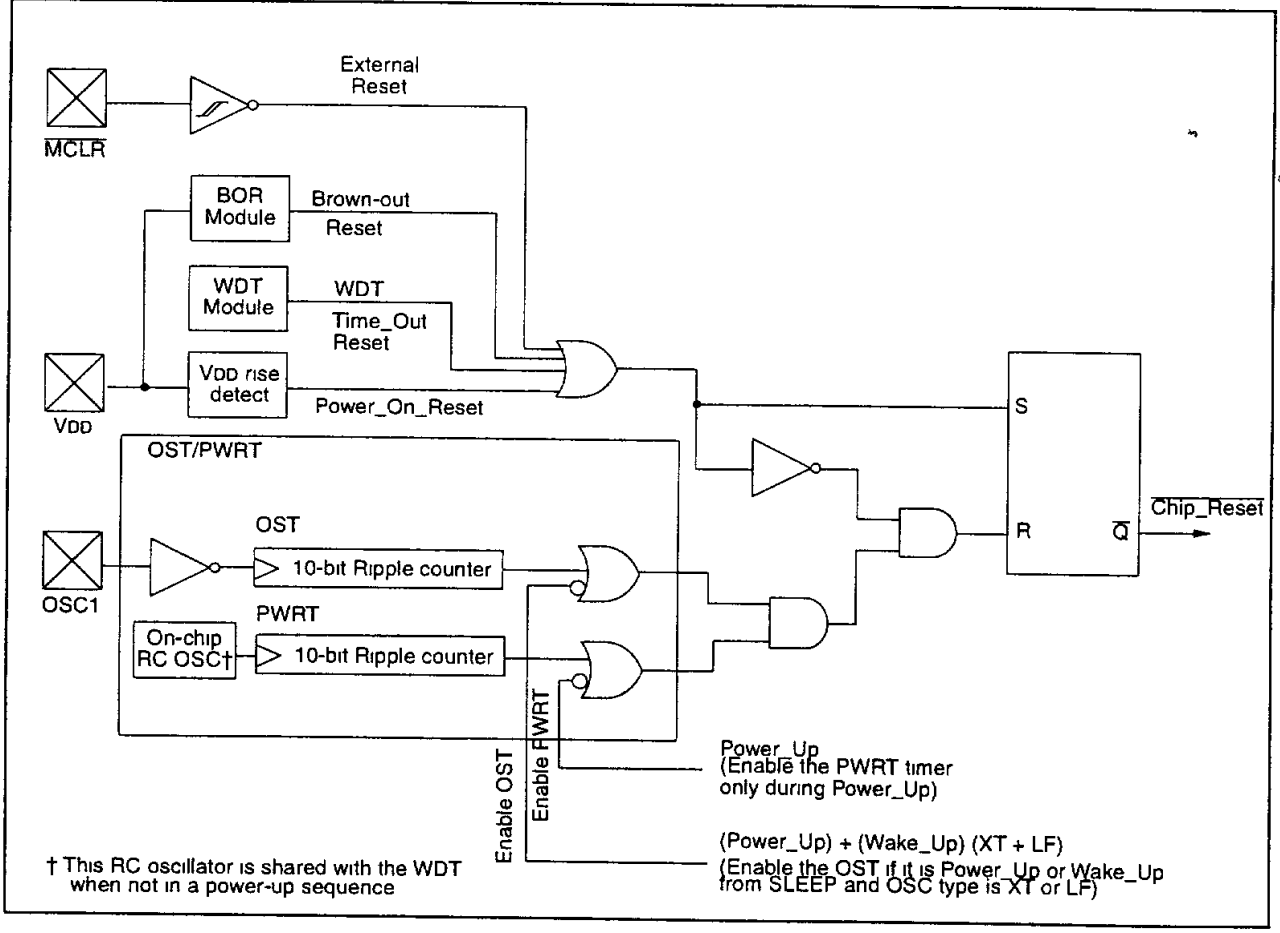
- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- Brown-out Reset
- WDT Reset (normal operation)

Some registers are not affected in any reset condition, their status is unknown on POR and unchanged in any other reset Most other registers are forced to a "reset state" on Power-on Reset (POR), Brown-out Reset (BOR), on $\overline{MCLR}$ or WDT Reset and on $\overline{MCLR}$ reset during SLEEP A WDT Reset during SLEEP, is viewed as the resumption of normal operation The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 5-3 These bits are used in software to determine the nature of the reset See Table 5-4 for a full description of reset states of all registers

Note:	While the device is in a reset state, the internal phase clock is held in the Q1 state. Any processor mode that allows external execution will force the RE0/ALE pin as a low output and the RE1/$\overline{OE}$ and RE2/$\overline{WR}$ pins as high outputs.

A simplified block diagram of the on-chip reset circuit is shown in Figure 5-1

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.1 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST), and Brown-out Reset (BOR)

5 1 1 POWER-ON RESET (POR)

The Power-on Reset circuit holds the device in reset until VDD is above the trip point (in the range of 1 4V - 2 3V) The devices produce an internal reset for both rising and falling VDD To take advantage of the POR, just tie the $\overline{MCLR}$/VPP pin directly (or through a resistor) to VDD This will eliminate external RC components usually needed to create Power-on Reset A minimum rise time for VDD is required See Electrical Specifications for details

Figure 5-2 and Figure 5-3 show two possible POR circuits

FIGURE 5-2: USING ON-CHIP POR

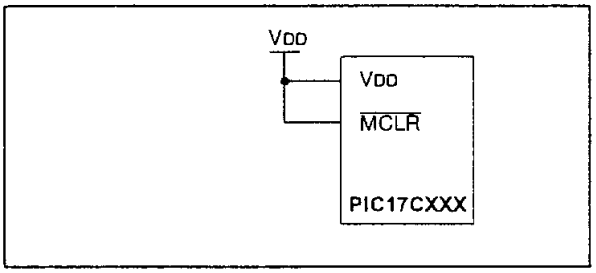
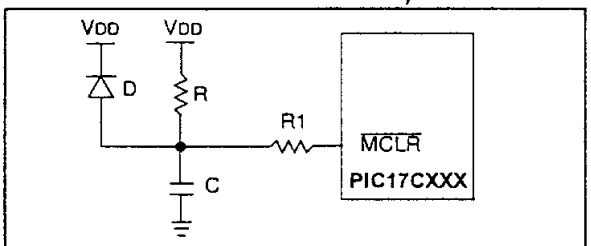


FIGURE 5-3: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1 An external Power-on Reset circuit is required only if VDD power-up time is too slow The diode D helps discharge the capacitor quickly when VDD powers down.

2 R < 40 kΩ is recommended to ensure that the voltage drop across R does not exceed 0 2V (max leakage current spec on the $\overline{MCLR}$/VPP pin is 5 µA) A larger voltage drop will degrade VIH level on the $\overline{MCLR}$/VPP pin

3 R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS)

5 1 2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 96 ms time-out (nominal) on power-up This occurs from the rising edge of the POR signal and after the first rising edge of $\overline{MCLR}$ (detected high) The Power-up Timer operates on an internal RC oscillator The chip is kept in RESET as long as the PWRT is active In most cases the PWRT delay allows VDD to rise to an acceptable level

The power-up time delay will vary from chip to chip and with VDD and temperature. See DC parameters for details

5 1 3 OSCILLATOR START-UP TIMER (OST)

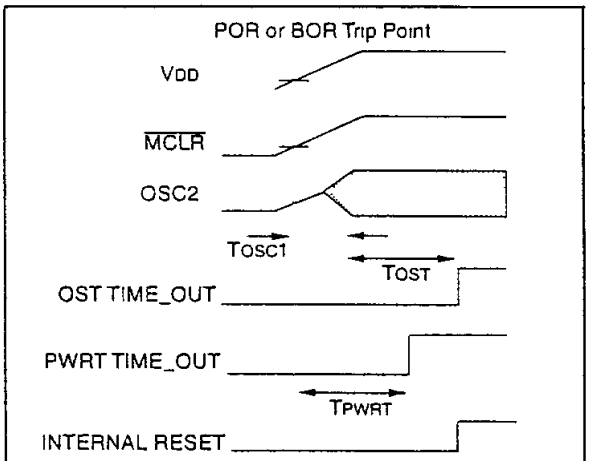
The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (1024TOSC) delay after $\overline{MCLR}$ is detected high or a wake-up from SLEEP event occurs

The OST time-out is invoked only for XT and LF oscillator modes on a Power-on Reset or a Wake-up from SLEEP.

The OST counts the oscillator pulses on the OSC1/CLKIN pin The counter only starts incrementing after the amplitude of the signal reaches the oscillator input thresholds This delay allows the crystal oscillator or resonator to stabilize before the device exits reset The length of the time-out is a function of the crystal/resonator frequency

Figure 5-4 shows the operation of the OST circuit In this figure the oscillator is of such a low frequency that OST time out occurs after the power-up timer time-out

FIGURE 5-4: OSCILLATOR START-UP TIME



This figure shows in greater detail the timings involved with the oscillator start-up timer In this example the low frequency crystal start-up time is larger than power-up time (TPWRT)

Tosc1 = time for the crystal oscillator to react to an oscillation level detectable by the Oscillator Start-up Timer (ost)

TOST = 1024TOSC

5 1 4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows First the internal POR signal goes high when the POR trip point is reached If $\overline{MCLR}$ is high, then both the OST and PWRT timers start In general the PWRT time-out is longer, except with low frequency crystals/resonators The total time-out also varies based on oscillator configuration Table 5-1 shows the times that are associated with the oscillator configuration Figure 5-5 and Figure 5-6 display these time-out sequences

If the device voltage is not within electrical specification at the end of a time-out, the $\overline{MCLR}$/VPP pin must be held low until the voltage is within the device specification The use of an external RC delay is sufficient for many of these applications

The time-out sequence begins from the first rising edge of $\overline{MCLR}$

Table 5-3 shows the reset conditions for some special registers, while Table 5-4 shows the initialization conditions for all the registers

TABLE 5-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up	Wake up from SLEEP	$\overline{MCLR}$ Reset	BOR
XT, LF	Greater of 96 ms or 1024Tosc	1024Tosc	—	—
EC, RC	Greater of 96 ms or 1024Tosc	—	—	—

TABLE 5-2: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$ (1)	$\overline{TO}$	$\overline{PD}$	Event
0	0	1	1	Power-on Reset
1	1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP
1	1	0	1	WDT Reset during normal operation
1	1	0	0	WDT Wake-up during SLEEP
1	1	1	1	$\overline{MCLR}$ Reset during normal operation
1	0	x	x	Brown-out Reset
0	0	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	0	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
x	x	1	1	CLRWDT instruction executed

Note 1 When BOR is enabled, else the $\overline{BOR}$ status bit is unknown

TABLE 5-3: RESET CONDITION FOR THE PROGRAM COUNTER AND THE CPUSTA REGISTER

Event		PCH PCL	CPUSTA (4)	OST Active
Power-on Reset		0000h	--11 1100	Yes
Brown-out Reset		0000h	--11 1101	No
$\overline{MCLR}$ Reset during normal operation		0000h	--11 1111	No
$\overline{MCLR}$ Reset during SLEEP		0000h	--11 1011	Yes (2)
WDT Reset during normal operation		0000h	--11 0111	No
WDT Wake-up during SLEEP (3)		0000h	--11 0011	Yes (2)
Interrupt wake-up from SLEEP	GLINTD is set	PC + 1	--11 1011	Yes (2)
	GLINTD is clear	PC + 1 (1)	--10 1011	Yes (2)

Legend u = unchanged, x = unknown, - = unimplemented read as '0'

Note 1 On wake-up, this instruction is executed The instruction at the appropriate interrupt vector is fetched and then executed

2 The OST is only active when the Oscillator is configured for XT or LF modes

3 The Program Counter = 0, that is, the device branches to the reset vector This is different from the mid-range devices

4 When $\overline{BOR}$ is enabled, else the $\overline{BOR}$ status bit is unknown

In Figure 5-5, Figure 5-6 and Figure 5-7, TPWRT > TOST, as would be the case in higher frequency crystals. For lower frequency crystals, (i e , 32 kHz) TOST would be greater

FIGURE 5-5. TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

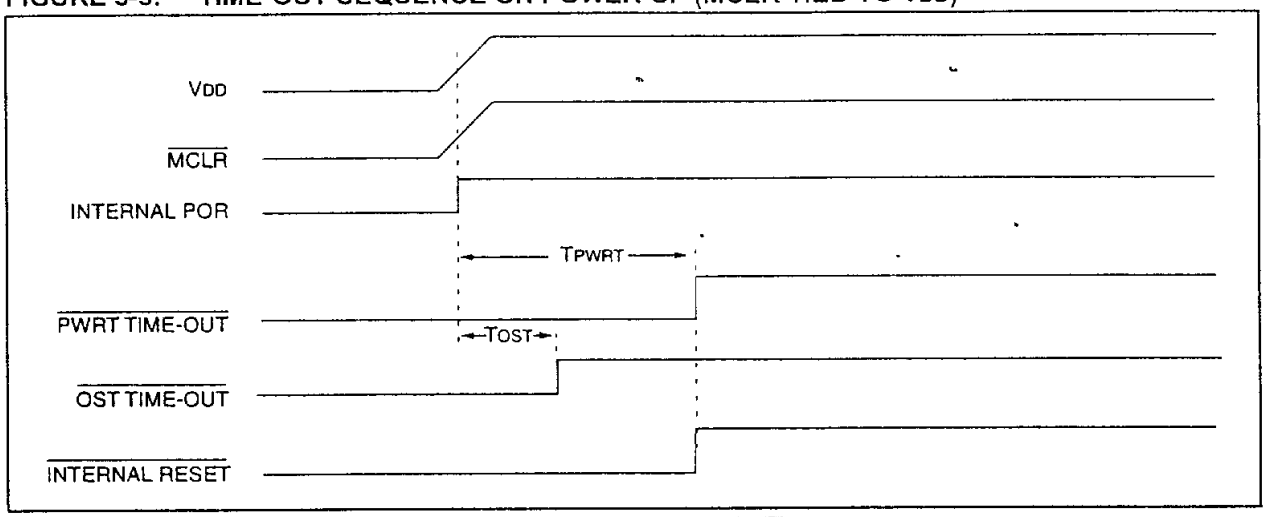


FIGURE 5-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)

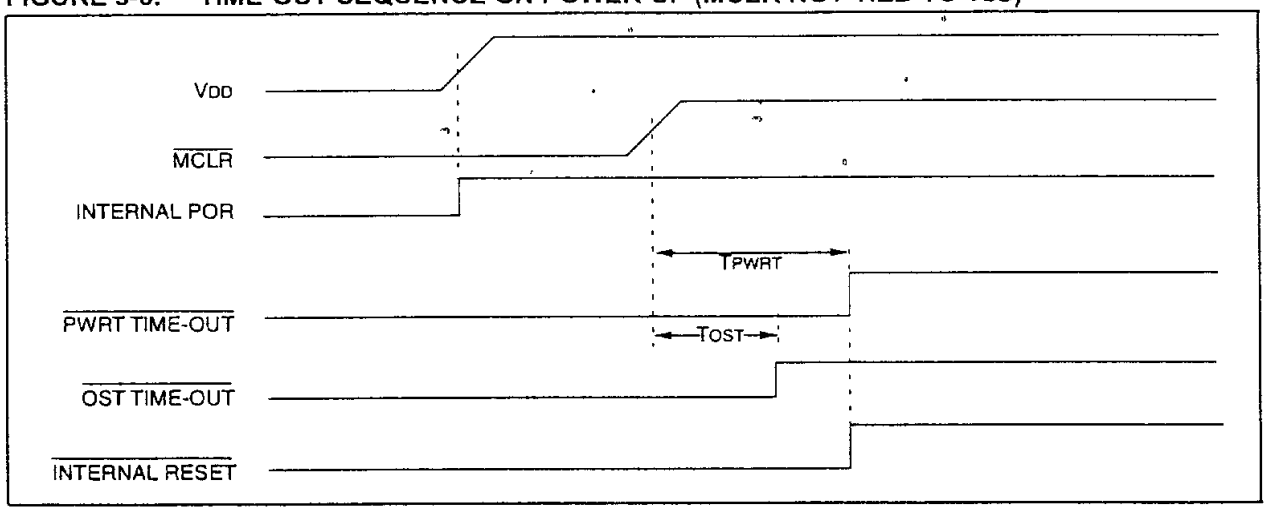


FIGURE 5-7: SLOW RISE TIME ($\overline{MCLR}$ TIED TO VDD)

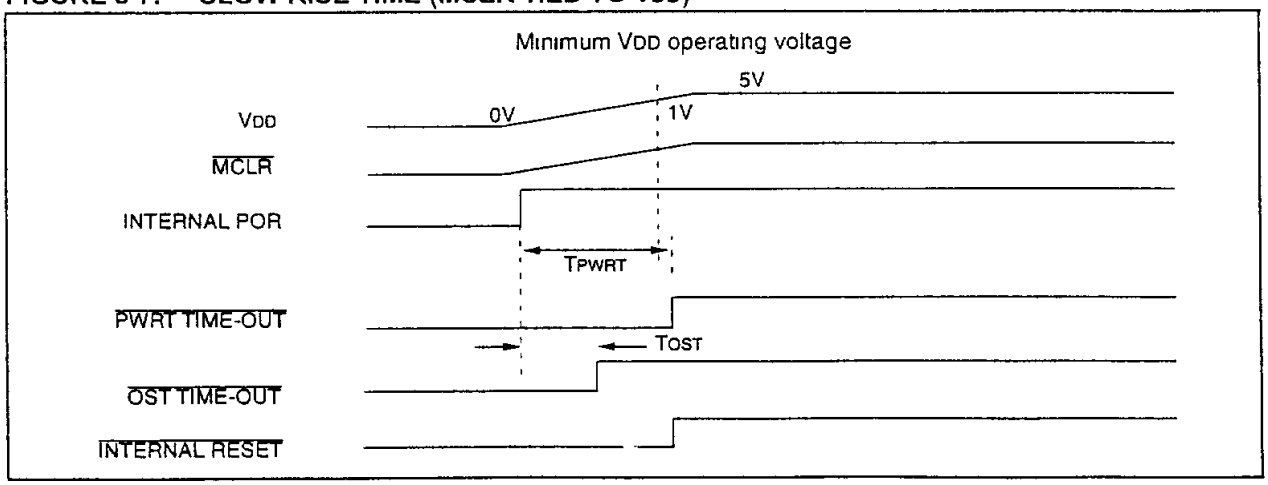


TABLE 5-4: INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS

Register	Address	Power-on Reset Brown-out Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through interrupt
Unbanked				
INDF0	00h	N A	N A	N A
FSR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1(2)
PCLATH	03h	0000 0000	0000 0000	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
T0STA	05h	0000 000-	0000 000-	0000 000-
CPUSTA(3)	06h	--11 1100(4)	--11 qquu(4)	--uu qquu(4)
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu(1)
INDF1	08h	N A	N.A	N.A.
FSR1	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	0Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH	0Eh	0000 0000	0000 0000	uuuu uuuu
BSR	0Fh	0000 0000	Q000 0000	uuuu uuuu
Bank 0				
PORTA	10h	0-xx xxxx	0-uu uuuu	u-uu uuuu
DDRB	11h	1111 1111	1111 1111	uuuu uuuu
PORTB	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCSTA1	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG1	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	15h	0000 --1x	0000 --1u	uuuu --uu
TXREG1	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SPBRG1	17h	xxxx xxxx	uuuu uuuu	uuuu uuuu
Bank 1				
DDRC	10h	1111 1111	1111 1111	uuuu uuuu
PORTC	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
DDRD	12h	1111 1111	1111 1111	uuuu uuuu
PORTD	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
DDRE	14h	---- 1111	---- 1111	---- uuuu
PORTE	15h	---- xxxx	---- uuuu	---- uuuu
PIR1	16h	x000 0010	u000 0010	uuuu uuuu(1)
PIE1	17h	0000 0000	0000 0000	uuuu uuuu

Legend u = unchanged, x = unknown, - = unimplemented read as '0', q = value depends on condition.

Note 1. One or more bits in INTSTA, PIR1, PIR2 will be affected (to cause wake-up)

2 When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector

3 See Table 5-3 for reset value of specific condition

4 If Brown-out is enabled, else the $\overline{BOR}$ bit is unknown.