



# MX23C1611

## 5 Volt 16-Mbit (2M x 8/1M x 16) Mask ROM with Page Mode

### FEATURES

- Bit organization
  - 2M x 8 (byte mode)
  - 1M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
  - Page access: 50ns (max.)
- Page Size
  - 8 double words per page
- Current
  - Operating: 60mA
  - Standby: 100uA
- Supply voltage
  - 5V±10%
- Package
  - 44 pin SOP (500mil)
  - 42 pin PDIP (600mm)
  - 48 pin TSOP (20mm x 12mm)

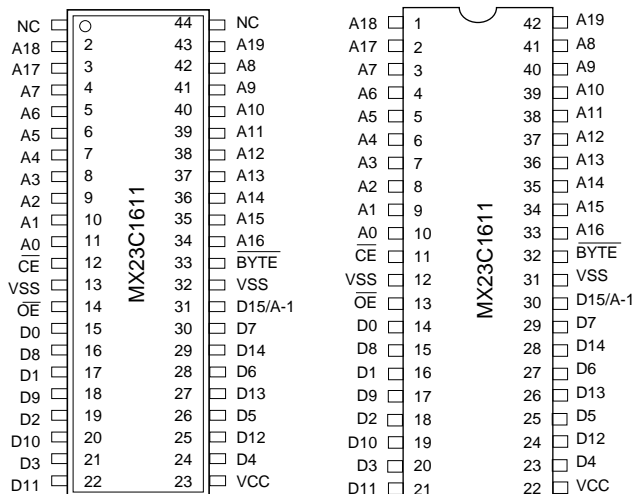
### ORDER INFORMATION

Part No.	Access Page Access Package		
	Time	Time	
MX23C1611MC-10	100ns	50ns	44 pin SOP
MX23C1611MC-12	120ns	60ns	44 pin SOP
MX23C1611PC-10	100ns	50ns	42 pin PDIP
MX23C1611PC-12	120ns	60ns	42 pin PDIP
MX23C1611TC-10	100ns	50ns	48 pin TSOP
MX23C1611TC-12	120ns	60ns	48 pin TSOP

### PIN CONFIGURATION

#### 44 SOP

#### 42 PDIP



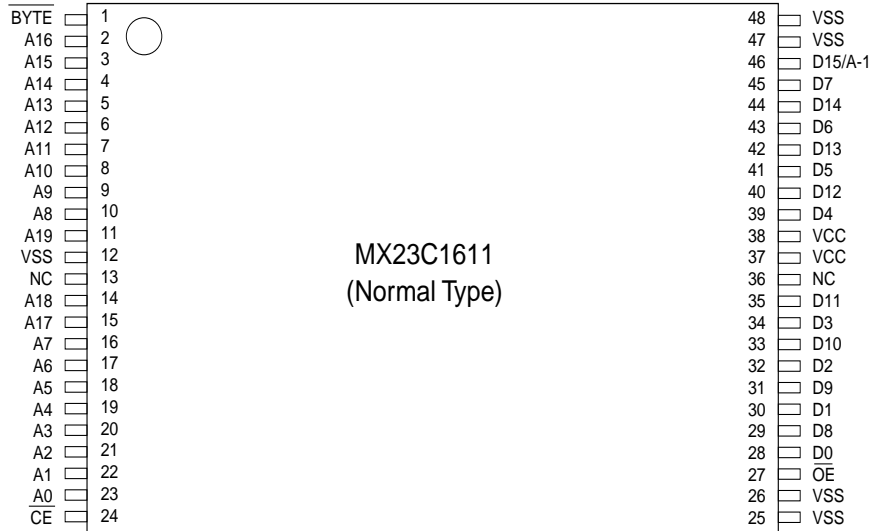
### PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
CE	Chip Enable Input
OE	Output Enable Input
Byte	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

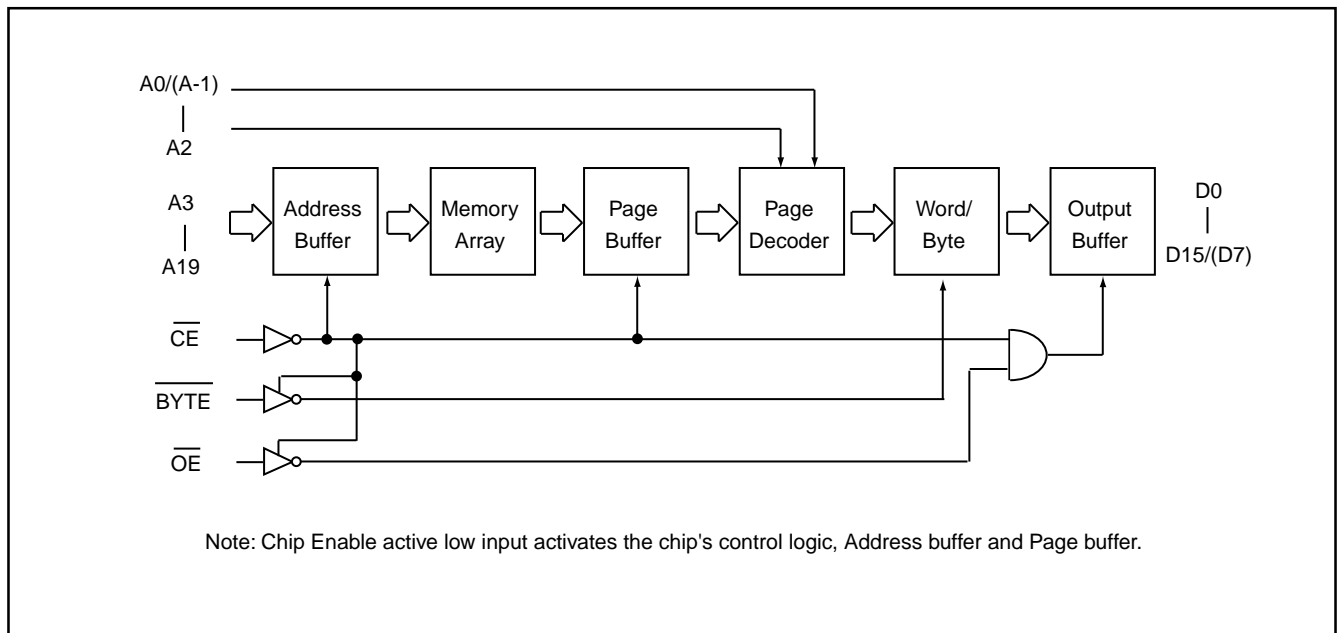
### MODE SELECTION

CE	OE	Byte	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

## 48 TSOP (Normal Type)



## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	-40°C to 85°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE} = V_{IH}$
Standby Current (cmos)	ISTB2	-	100uA	$\overline{CE} > V_{CC} - 0.2V$
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

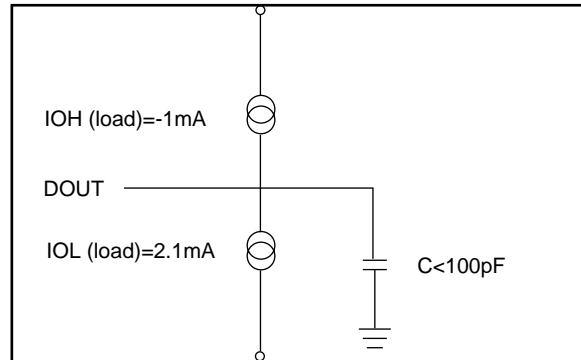
**AC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	23C1611-10		23C1611-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	100ns	-	120ns
Page Mode Access Time	tPA	-	50ns	-	60ns
Output Enable Time	tOE	-	50ns	-	60ns
Output Hold After Address	tOH	10ns	-	10ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from  $\overline{OE}$  or  $\overline{CE}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



Note:

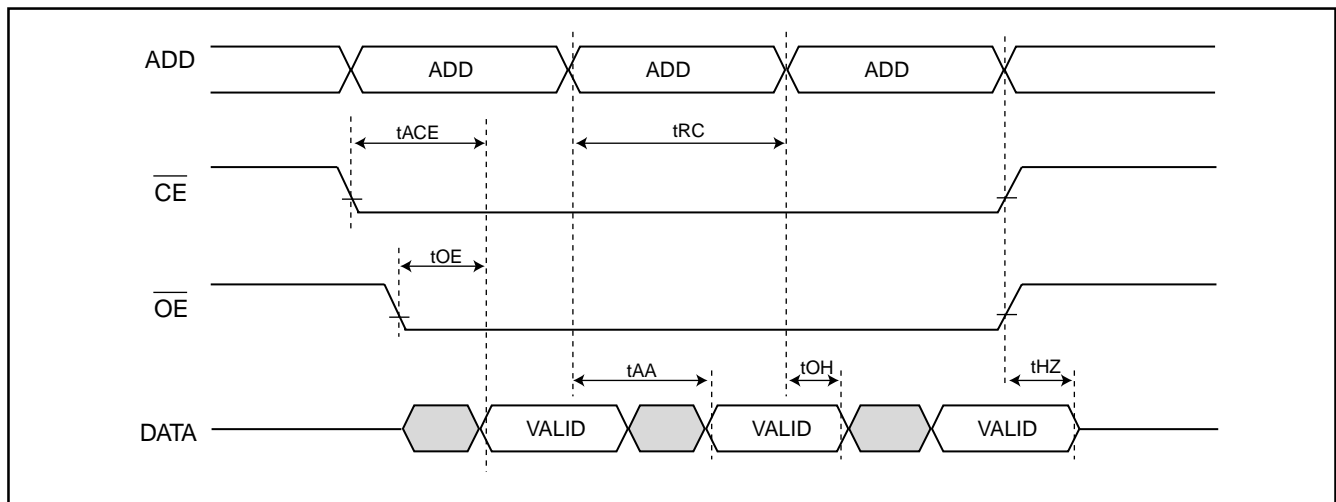
No output loading is present in tester load board.

Active loading is used and under software programming control.

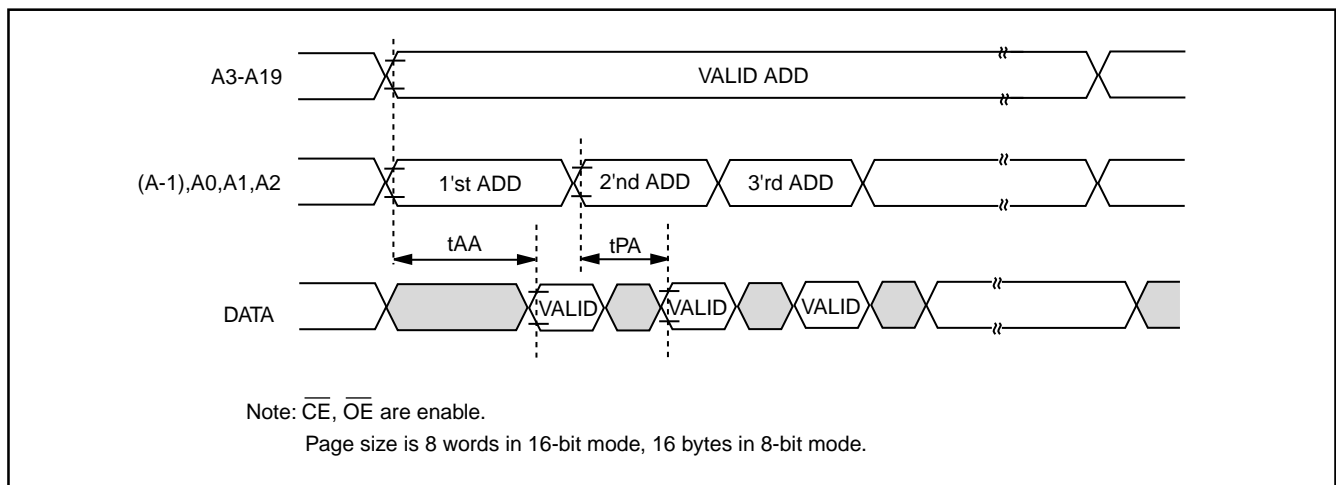
Output loading capacitance includes load board's and all stray capacitance.

## TIMING DIAGRAM

### RANDOM READ

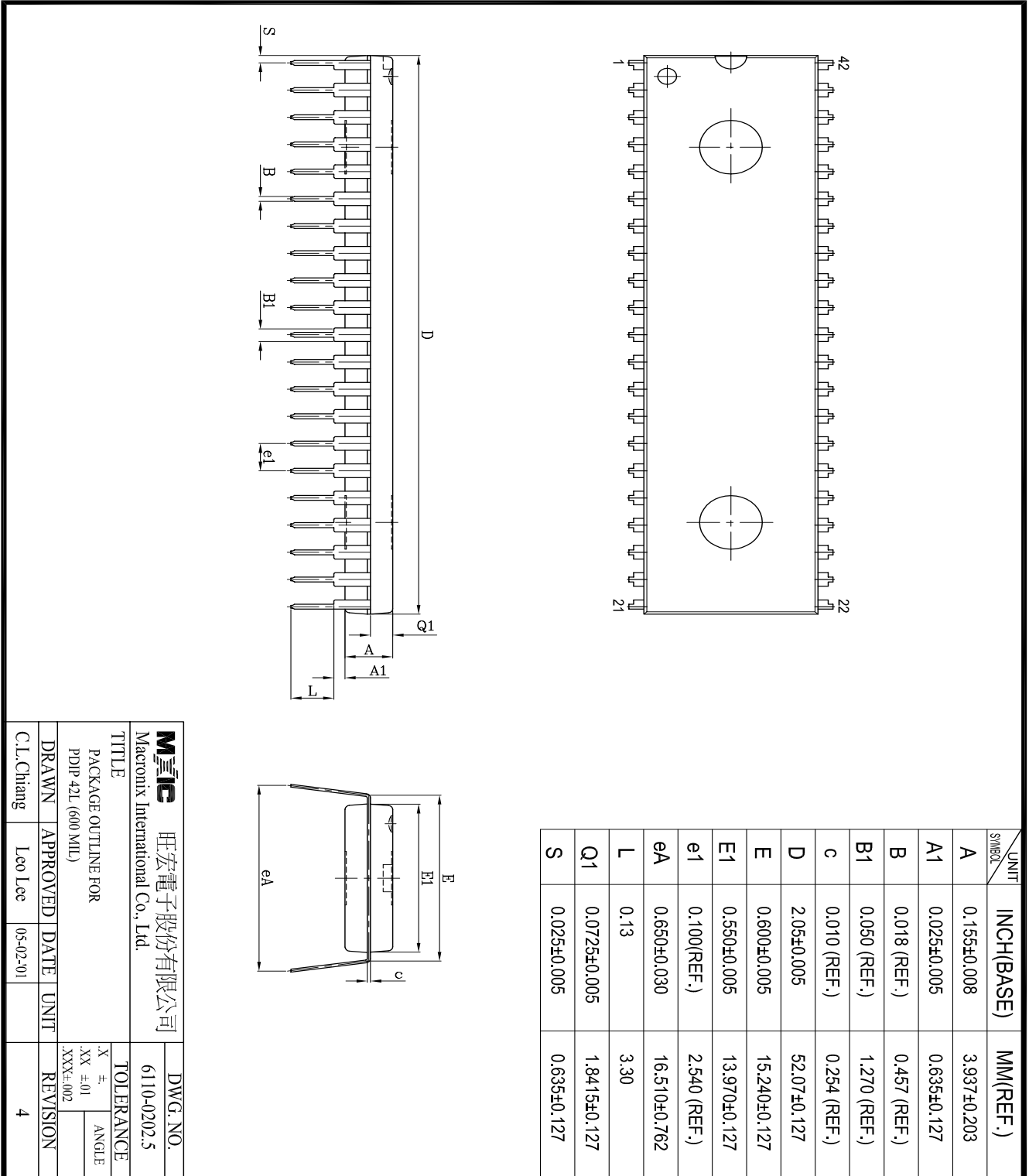


### PAGE READ



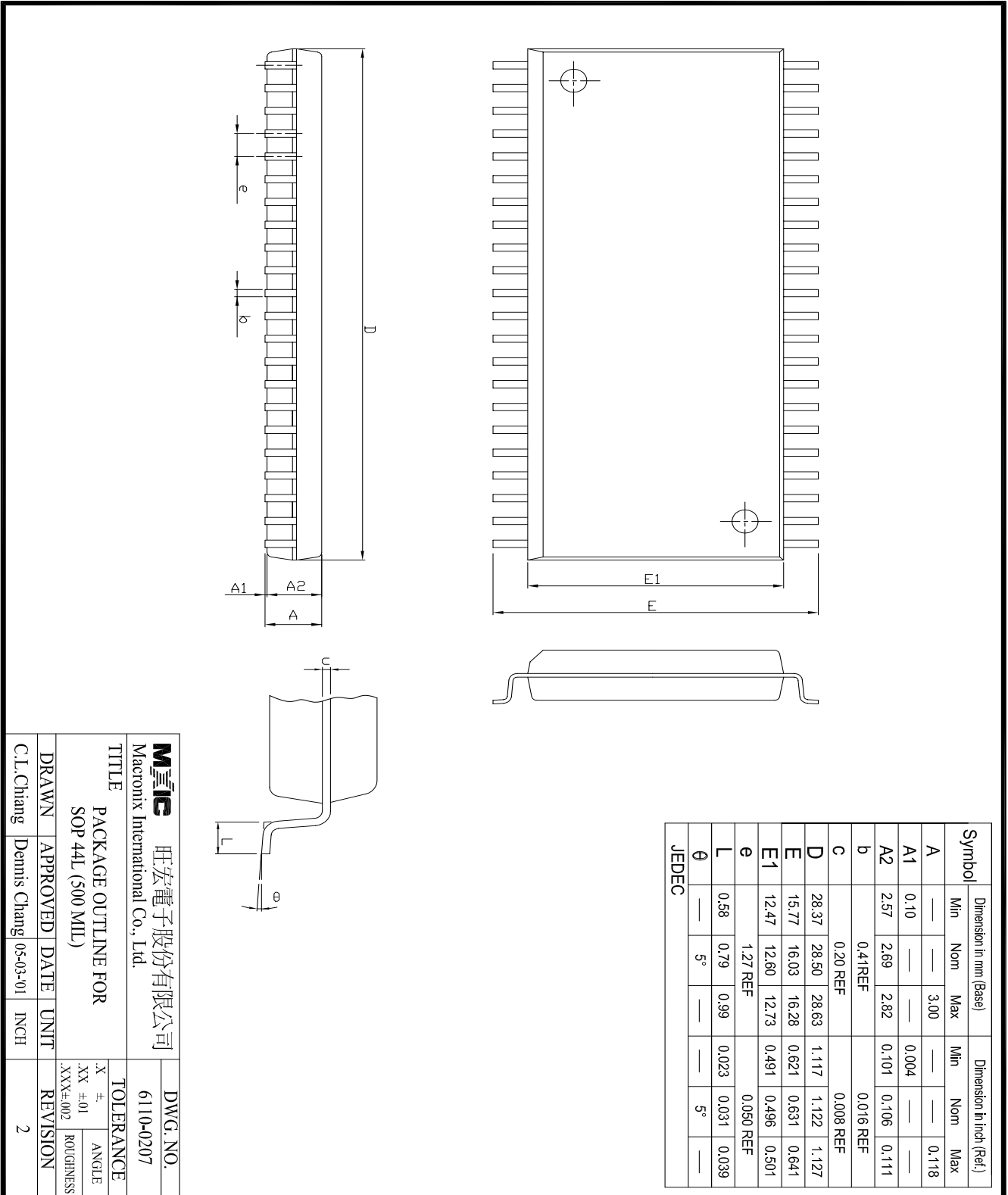
## PACKAGE INFORMATION

### 42-PIN PLASTIC DIP(600 mil)

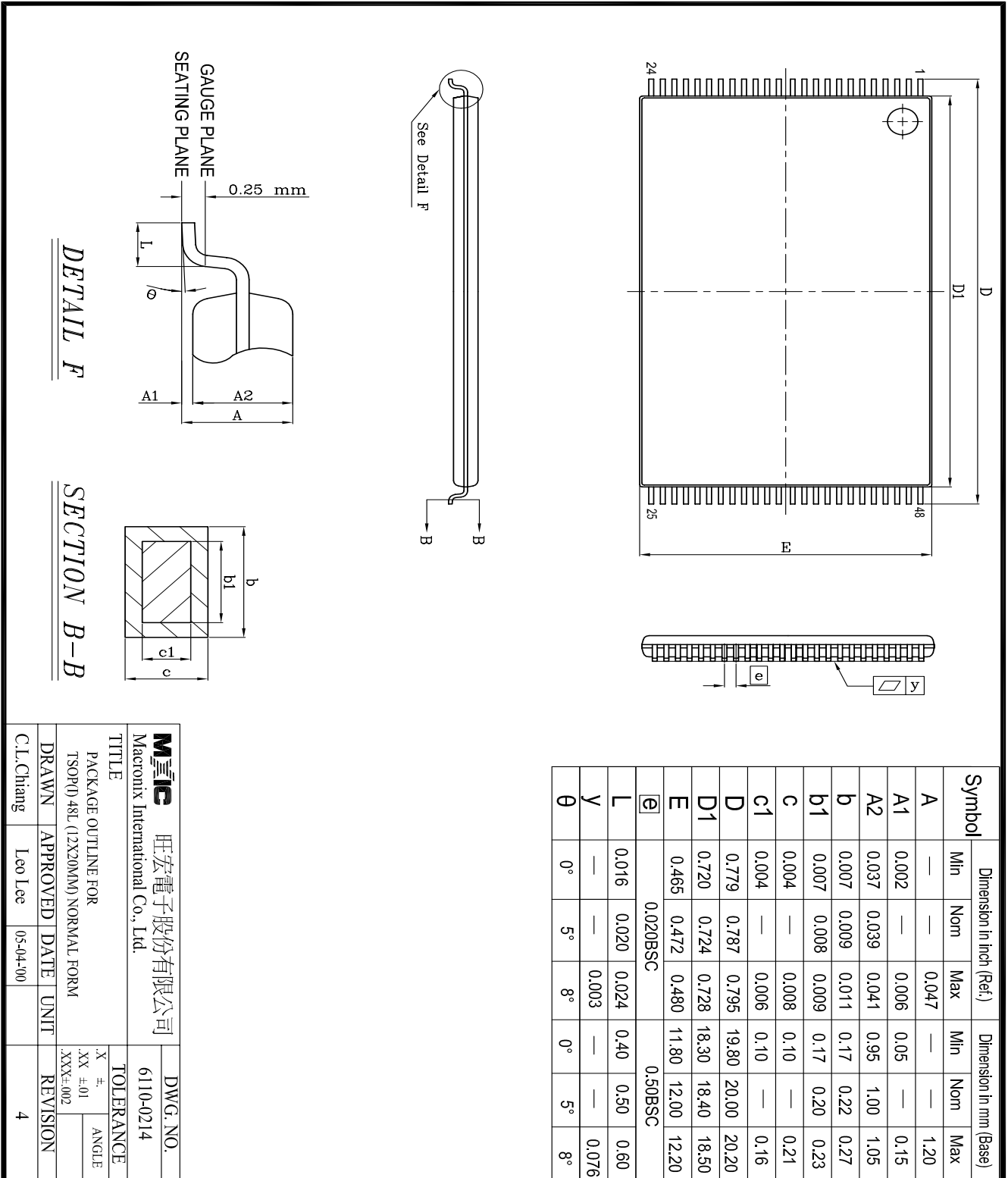


<b>Mxic</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO.	61110-0202.5
TITLE PACKAGE OUTLINE FOR PDIP 42L (600 MIL)		TOLERANCE	.X ±. XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE	UNIT
C.L.Chang	Leo Lee	05-02-01	4

## 44-PIN PLASTIC SOP



## 48-PINTSOP



**DETAIL F**

**SECTION B-B**

<b>MAGIC</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0214	
TITLE PACKAGE OUTLINE FOR TSOP(D) 48L (12X20MM) NORMAL FORM			
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-04-00	
TOLERANCE		REVISION	
.X ±.01		4	
.XX ±.01			
.XXX ±.002			
ANGLE			



**Revision History**

<b>Revision</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.8	tACE--->1000ns changes to tACE--->100ns	P3	JUL/20/1998
1.9	AC Characteristics: tOH 10ns --> 0ns	P3	FEB/01/1999
2.0	Typing error correction	P1	JAN/18/2000
2.1	Modify Package Information	P5~7	JUL/18/2001





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