MX23L1610

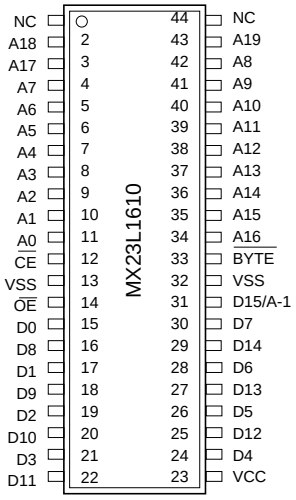
3.3 Volt 16-Mbit (2M x 8 / 1M x 16) Mask ROM

FEATURES

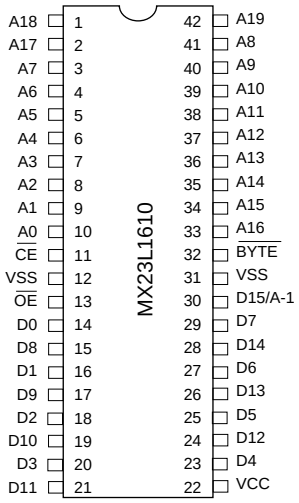
- Bit organization
  - 2M x 8 (byte mode)
  - 1M x 16 (word mode)
- Fast access time
  - 70ns (max.)@3.3V±10%
- Current
  - Operating:25mA
  - Standby:15uA
- Supply voltage
  - 3.0V ~ 3.6V
- Package
  - 44 pin SOP (500mil)
  - 42 pin DIP (600mil)
  - 48 pin TSOP (12mm x 20mm)
  - 44 pin TSOP (Type II)

PIN CONFIGURATION

44 SOP/44 TSOP



42 PDIP



ORDER INFORMATION

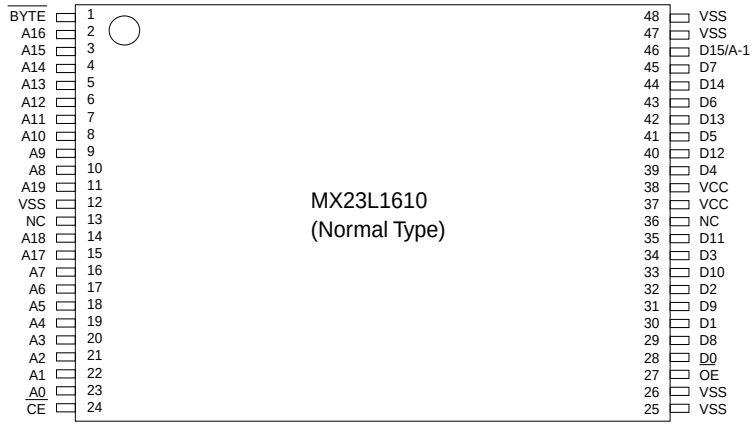
Part No.	Access	Package
MX23L1610MC-70	70ns	44 pin SOP
MX23L1610MC-90	90ns	44 pin SOP
MX23L1610MC-10	100ns	44 pin SOP
MX23L1610MC-12	120ns	44 pin SOP
MX23L1610MC-15	150ns	44 pin SOP
MX23L1610PC-10	100ns	42 pin PDIP
MX23L1610PC-12	120ns	42 pin PDIP
MX23L1610PC-15	150ns	42 pin PDIP
MX23L1610TC-70	70ns	48 pin TSOP
MX23L1610TC-90	90ns	48 pin TSOP
MX23L1610TC-10	100ns	48 pin TSOP
MX23L1610TC-12	120ns	48 pin TSOP
MX23L1610TC-15	150ns	48 pin TSOP
MX23L1610RC-10	100ns	48 pin TSOP (Reverse type)
MX23L1610RC-90	90ns	48 pin TSOP (Reverse type)
MX23L1610RC-12	120ns	48 pin TSOP (Reverse type)
MX23L1610RC-15	150ns	48 pin TSOP (Reverse type)
MX23L1610TI-12*	120ns	48 pin TSOP
MX23L1610YC-10	100ns	44 pin TSOP
MX23L1610YC-12	120ns	44 pin TSOP
MX23L1610YC-15	150ns	44 pin TSOP

*Note:Temperature: -40~85° C

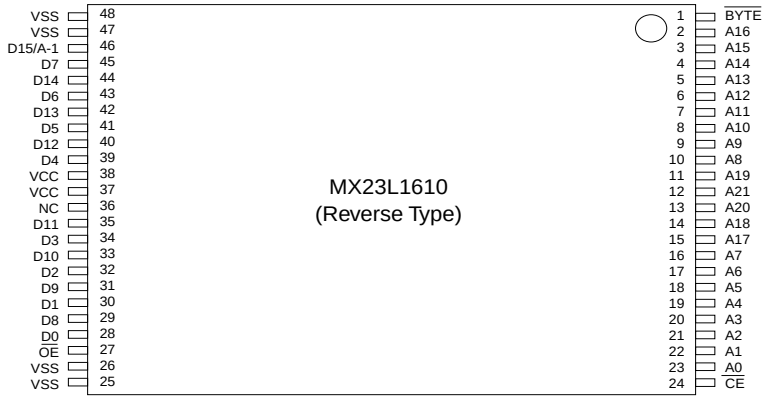
PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{Byte}$	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

48 TSOP (Normal Type)



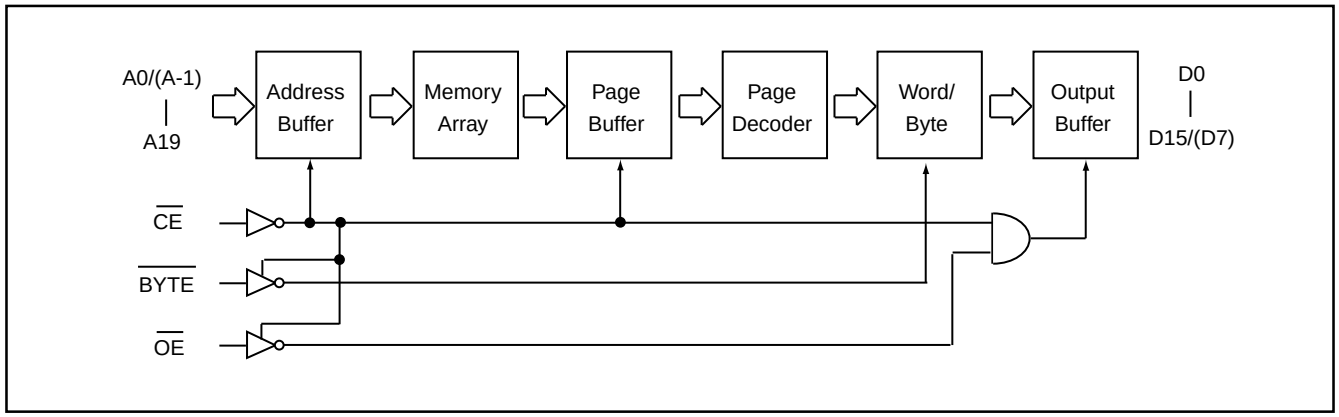
48 TSOP (Reverse Type)



MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 4.3V
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V*	MAX. number:VCC+0.3V is under normal operation mode, and VCC+0.7V is under non-operating mode
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	25mA	tRC = 120ns, all output open
Standby Current (TTL)	ISTB1	-	0.5mA	$\overline{CE}$ = VIH
Standby Current (cmos)	ISTB2	-	15uA	$\overline{CE}$>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

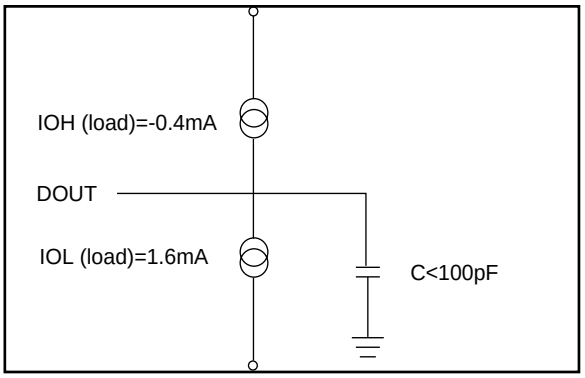
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	23L1610-70		23L1610-90		23L1610-10		23L1610-12		23L1610-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	35ns	-	45ns	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

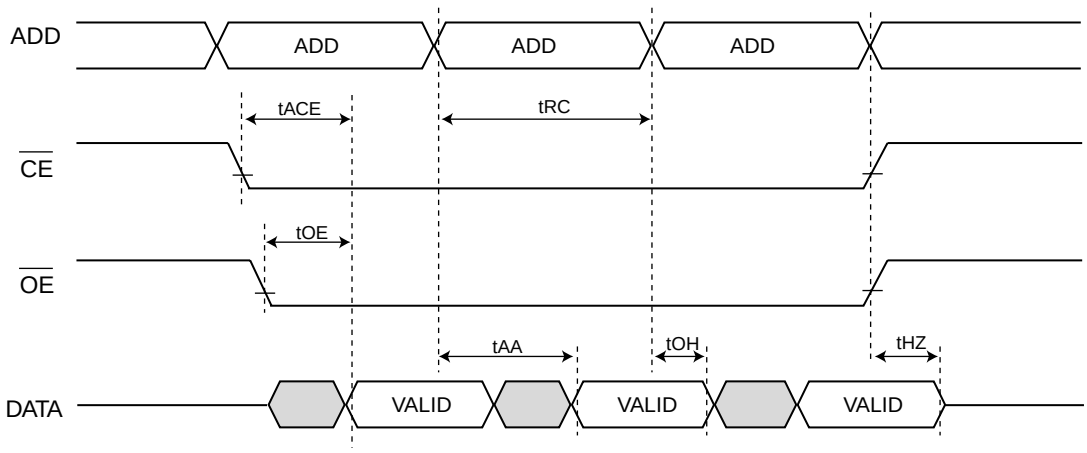
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note:
No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

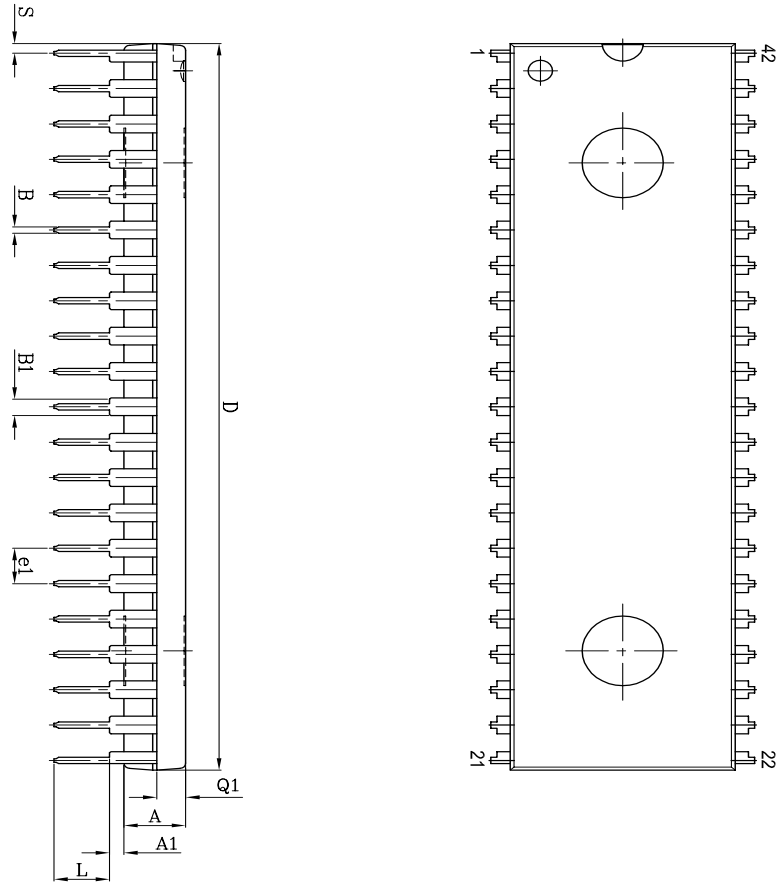
RANDOM READ



Note:$\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

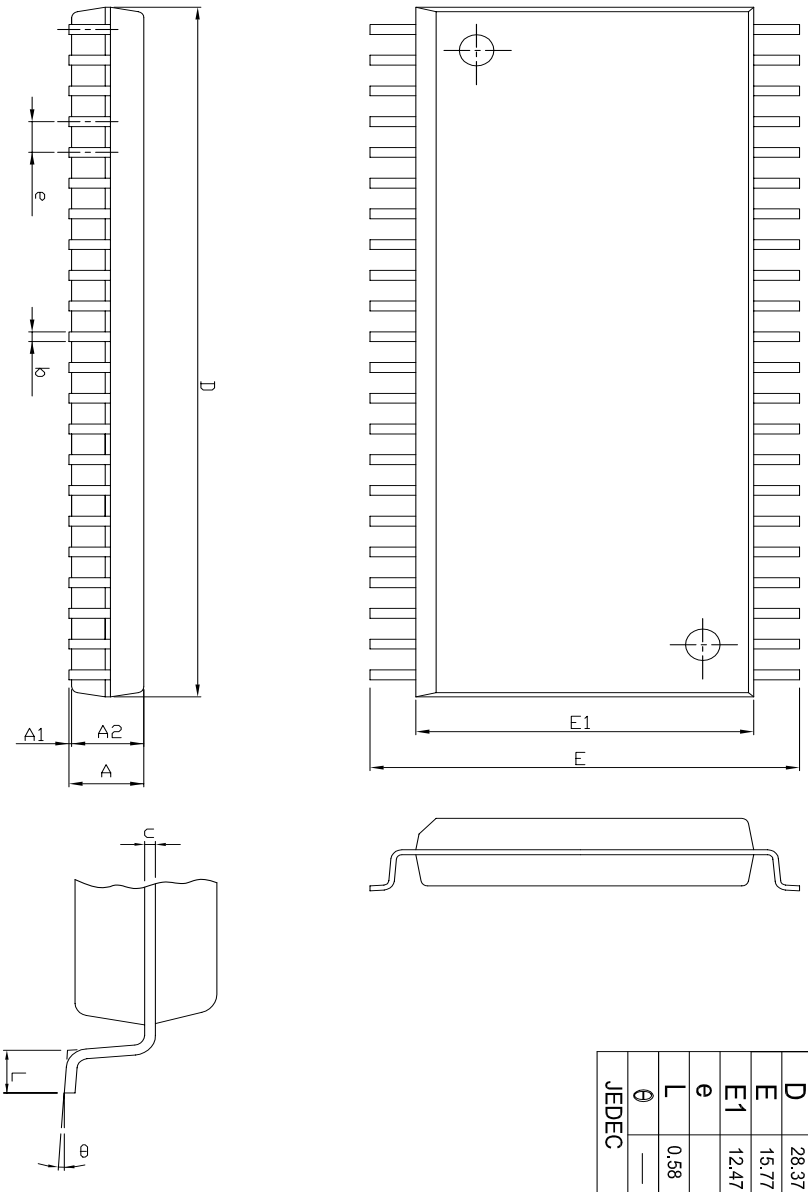
42-PIN PLASTIC DIP(600 mil)



SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.025±0.005	0.635±0.127

旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO.
TITLE			6110-0202.5
PACKAGE OUTLINE FOR PDIP 42L (600 MIL)			TOLERANCE .X ± .1 .XX ± .01 .XXX± .002 ANGLE
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-02-'01	REVISION
			4

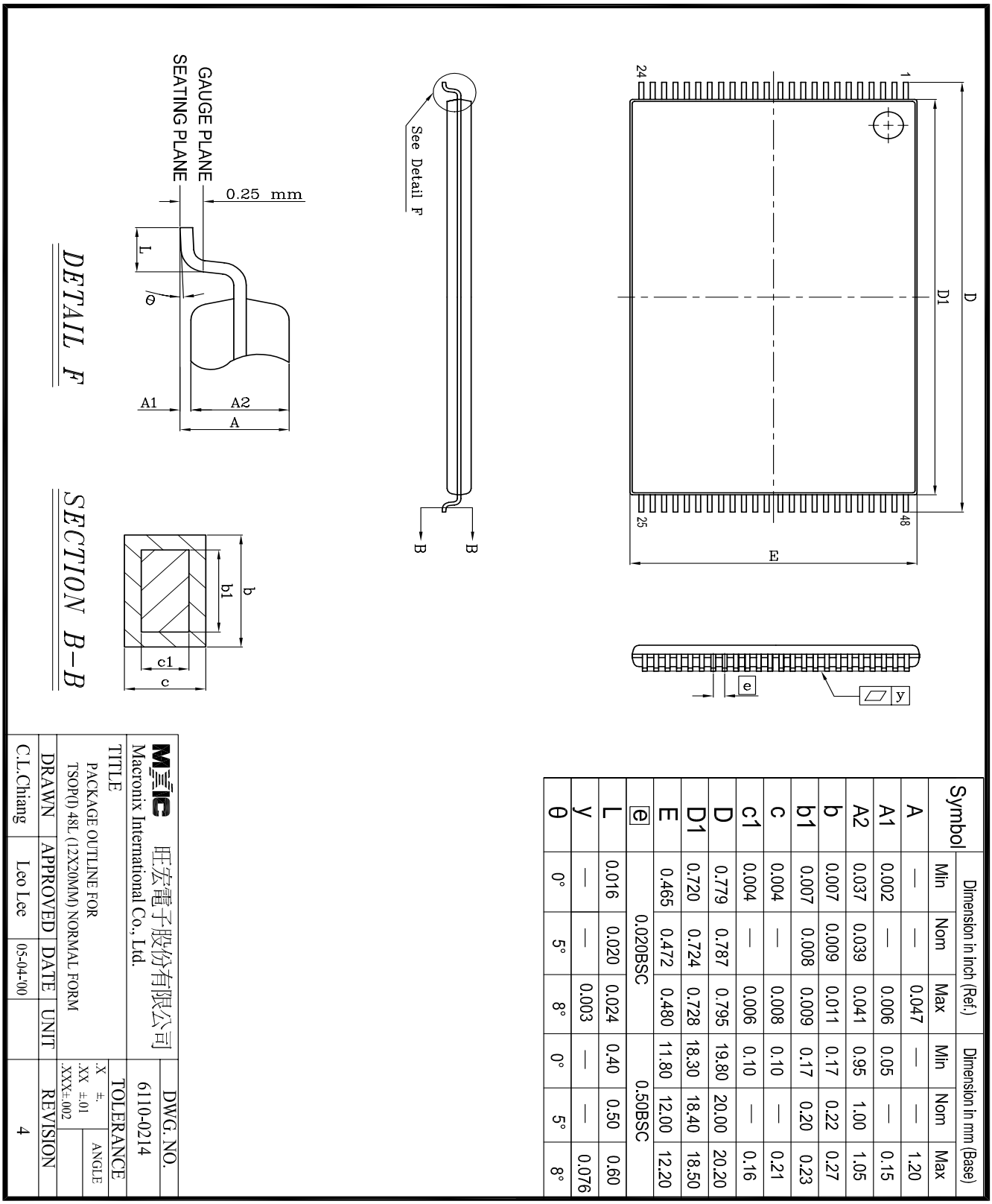
44-PIN PLASTIC SOP



Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b		0.41REF			0.016 REF	
c		0.20 REF			0.008 REF	
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e		1.27 REF			0.050 REF	
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—
JEDEC						

MXIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0207
TITLE	PACKAGE OUTLINE FOR SOP 44L (500 MIL)		TOLERANCE
		UNIT	.X ± .XX ±.01 ANGLE
			.XXX±.002 ROUGHNESS
DRAWN	APPROVED	DATE	REVISION
C.L.Chiang	Dennis Chang	05-03-01	2
		INCH	

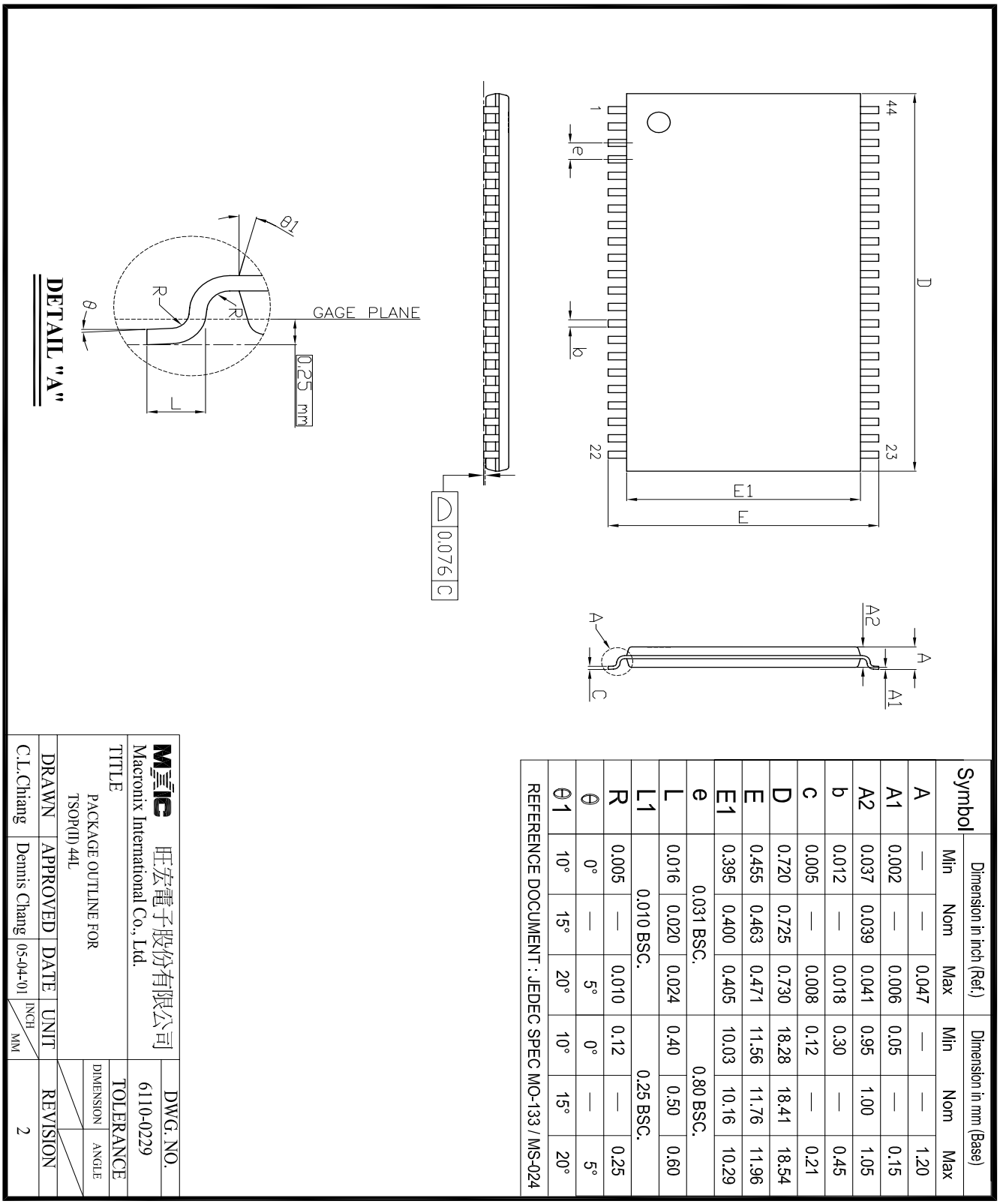
48-PIN PLASTIC TSOP



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
c	0.004	—	0.008	0.10	—	0.21
c1	0.004	—	0.006	0.10	—	0.16
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	0.465	0.472	0.480	11.80	12.00	12.20
e		0.020BSC			0.50BSC	
L	0.016	0.020	0.024	0.40	0.50	0.60
y	—	—	0.003	—	—	0.076
θ	0°	5°	8°	0°	5°	8°

MIC 旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0214
TITLE PACKAGE OUTLINE FOR TSOP(I) 48L (12X20MM) NORMAL FORM			TOLERANCE .X ±. ANGLE .XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-04-'00	
			REVISION 4

44-PIN TSOP (Type II)



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	—	0.018	0.30	—	0.45
c	0.005	—	0.008	0.12	—	0.21
D	0.720	0.725	0.730	18.28	18.41	18.54
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e		0.031 BSC.			0.80 BSC.	
L	0.016	0.020	0.024	0.40	0.50	0.60
L1		0.010 BSC.			0.25 BSC.	
R	0.005	—	0.010	0.12	—	0.25
θ	0°	—	5°	0°	—	5°
θ1	10°	15°	20°	10°	15°	20°

REFERENCE DOCUMENT : JEDEC SPEC MO-133 / MS-024

MIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0229
TITLE			TOLERANCE
PACKAGE OUTLINE FOR TSOP(II) 44L		DIMENSION	ANGLE
			REVISION
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-04-'01	INCH / MM
			2

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.9	1. Package Type:Add 42-PDIP package type. 2. DC Characteristics:The input low voltage VIL Max. value is changed as 0.2xVCC instead of 0.8V. 3. AC Characteristics:The output high Z delay is changed as 20ns instead of 70ns. 4. Add 105ns speed grade. 5. Add 100ns speed grade @3.3V±5% 6. AC Test Conditions:The output timing level is changed as 1.4V instead of 0.8V and 2.0V.		JUN/11/1998
2.0	AC CHARACTERISTICS tOH 10ns-->0ns	P4	FEB/01/1999
2.1	Typing error correction	P1	JAN/18/2000
2.2	1.Added 44-pin TSOP (Type II) Package 2.Modify Package Information	P1,8 P5~7	JUL/18/2001
2.3	1.Add 90ns speed grade 2.Delete 105ns speed grade	P1,3 P1,3	JUL/31/2001
2.4	1.Added 70ns speed grade	P1,3	AUG/14/2001
2.5	Change VOH(MIN.):2.3V-->2.4V; VIH(MIN.):2.1V-->2.2V	P3	AUG/15/2001

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