



MX23L8100

8M-BIT MASK ROM(8/16 BIT OUTPUT)

FEATURES

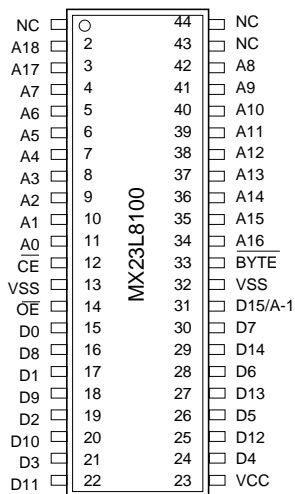
- Bit organization
 - 1M x 8 (byte mode)
 - 512K x 16 (word mode)
- Fast access time
 - Random access: 100ns (max.)
- Current
 - Operating: 20mA
 - Standby: 5uA
- Supply voltage
 - 3.3V±10%
- Package
 - 44 pin SOP (500mil)
 - 42 pin PDIP (600mil)
 - 48 pin TSOP (type 1)
 - 44 pin TSOP (type 2)

ORDER INFORMATION

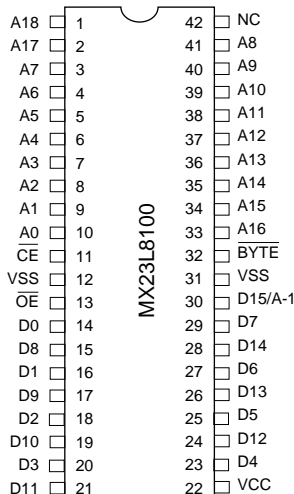
Part No.	Access Time	Package
MX23L8100MC-10	100ns	44 pin SOP
MX23L8100MC-12	120ns	44 pin SOP
MX23L8100MC-15	150ns	44 pin SOP
MX23L8100PC-10	100ns	42 pin PDIP
MX23L8100PC-12	120ns	42 pin PDIP
MX23L8100PC-15	150ns	42 pin PDIP
MX23L8100TC-10	100ns	48 pin TSOP*
MX23L8100TC-12	120ns	48 pin TSOP
MX23L8100TC-15	150ns	48 pin TSOP
MX23L8100RC-10	100ns	48 pin RTSOP*
MX23L8100RC-12	120ns	48 pin RTSOP
MX23L8100RC-15	150ns	48 pin RTSOP
MX23L8100YC-10	100ns	44 pin TSOP
MX23L8100YC-12	120ns	44 pin TSOP
MX23L8100TI-10	100ns	48 pin TSOP*

PIN CONFIGURATION

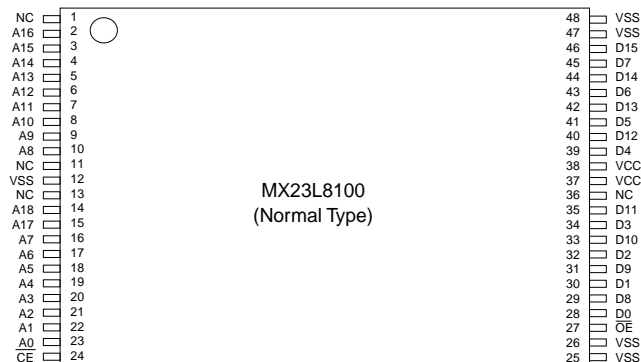
44 SOP/44TSOP



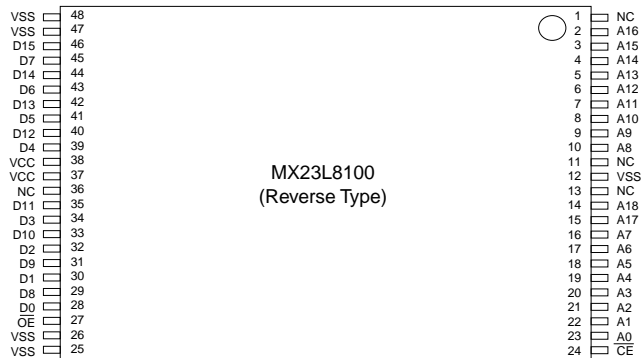
42 PDIP



48 TSOP (for word mode only)



48 Reverse TSOP (for word mode only)



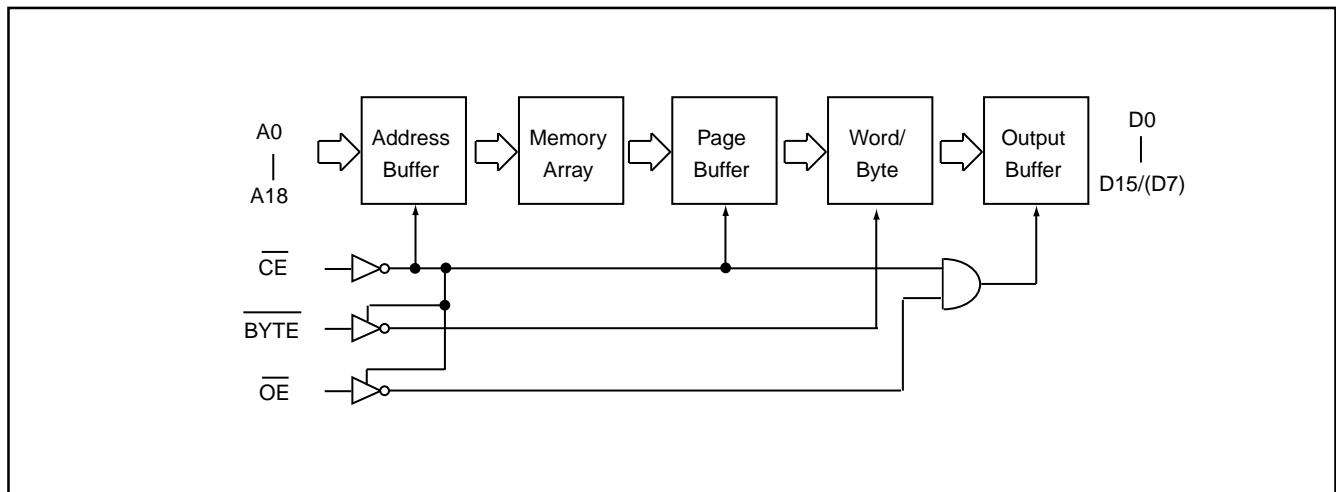
PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15(Word Mode)/LSB Address (Byte Mode)
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{Byte}	Word/Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

\overline{CE}	\overline{OE}	\overline{Byte}	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	T _{opr}	0°C to 70°C
Storage Temperature	T _{stg}	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	24V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	20mA	f=10MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	\overline{CE} =VIH
Standby Current (CMOS)	ISTB2	-	5uA	\overline{CE} > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

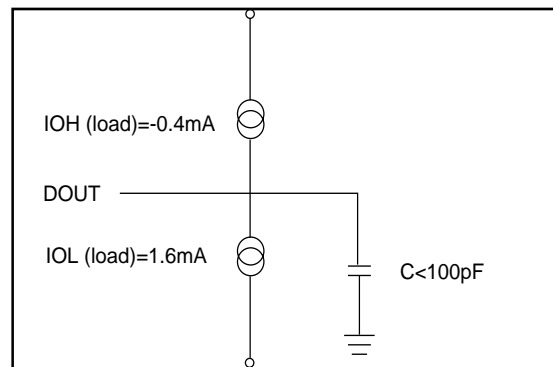
AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	23L8100-10		23L8100-12		23L8100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

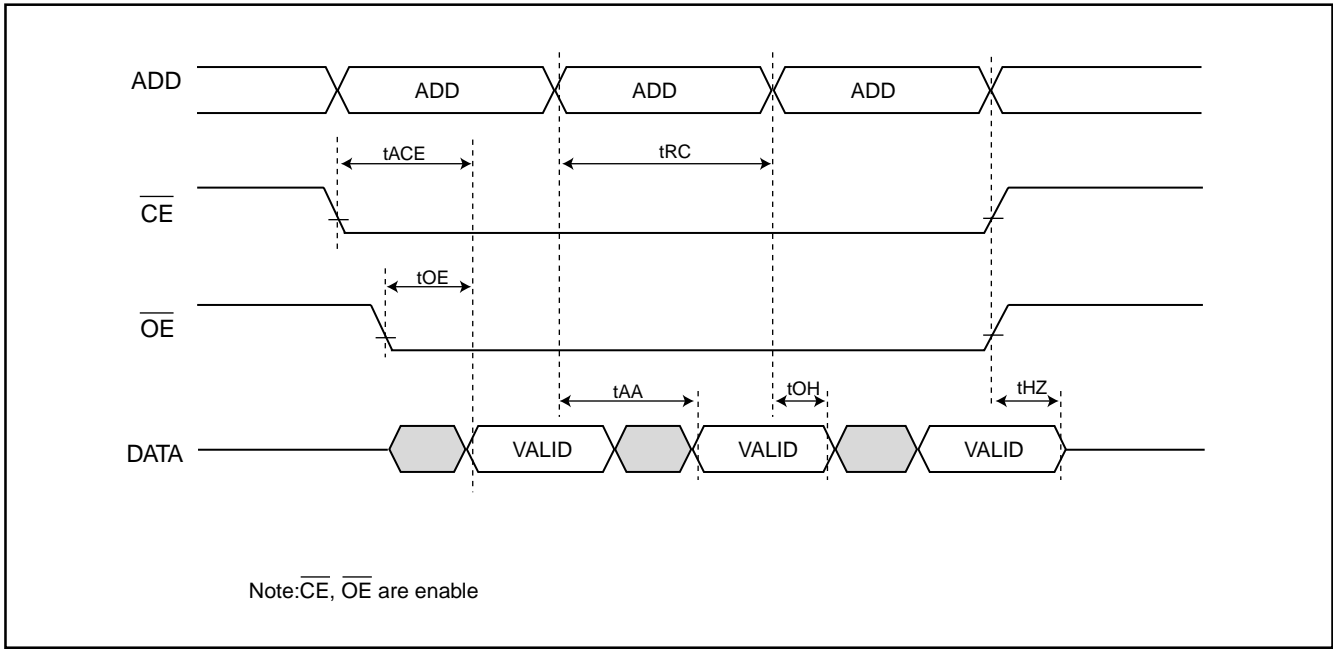
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note: No output loading is present in tester load board.

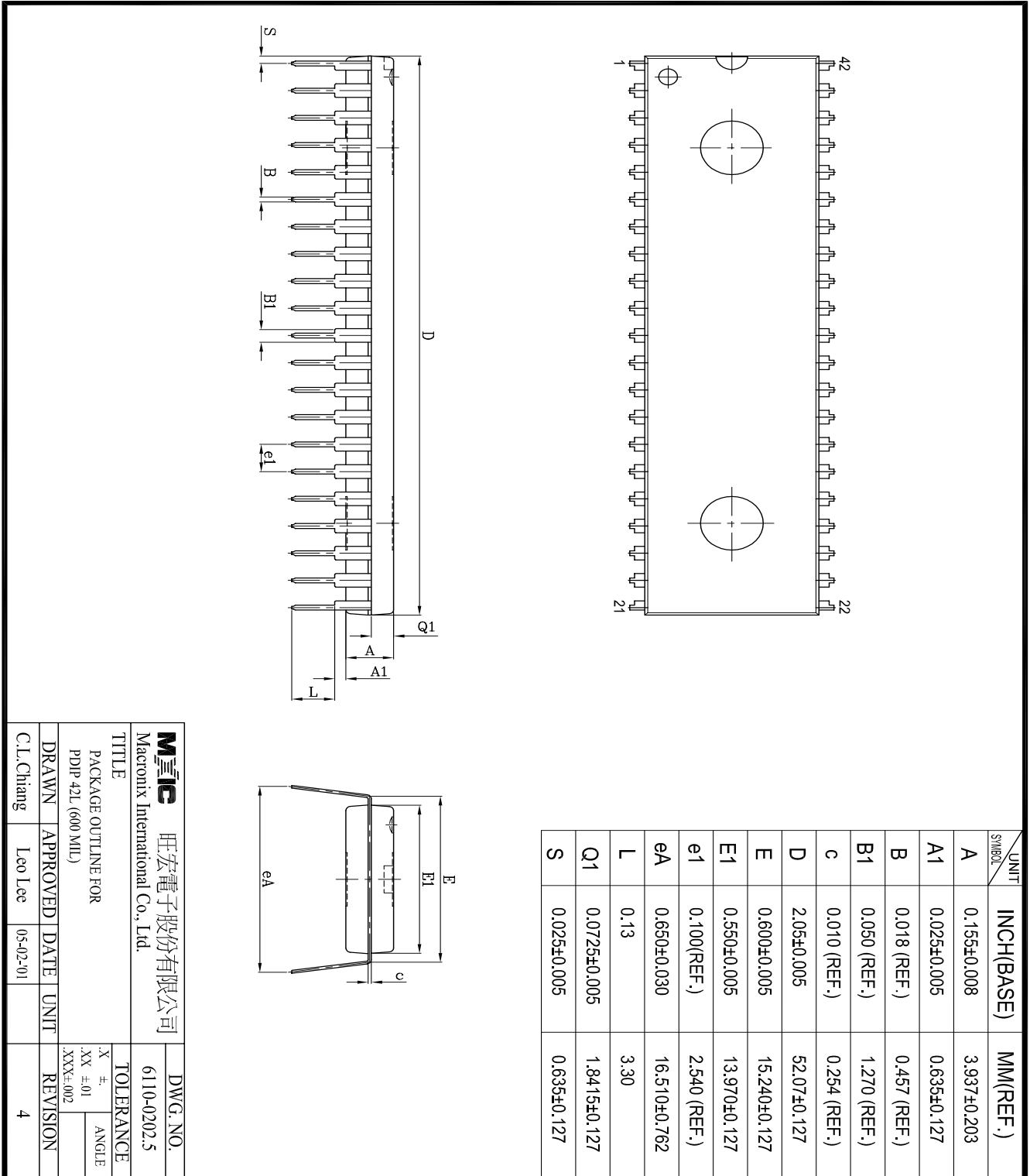
Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM**RANDOM READ**

PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)



Mxic 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0202.5	
TITLE PACKAGE OUTLINE FOR PDIP 42L (600 MIL)			
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-02-01	
TOLERANCE			REVISION
X #			4
XX ±.01			
XXX±.002			

44-PIN PLASTIC SOP

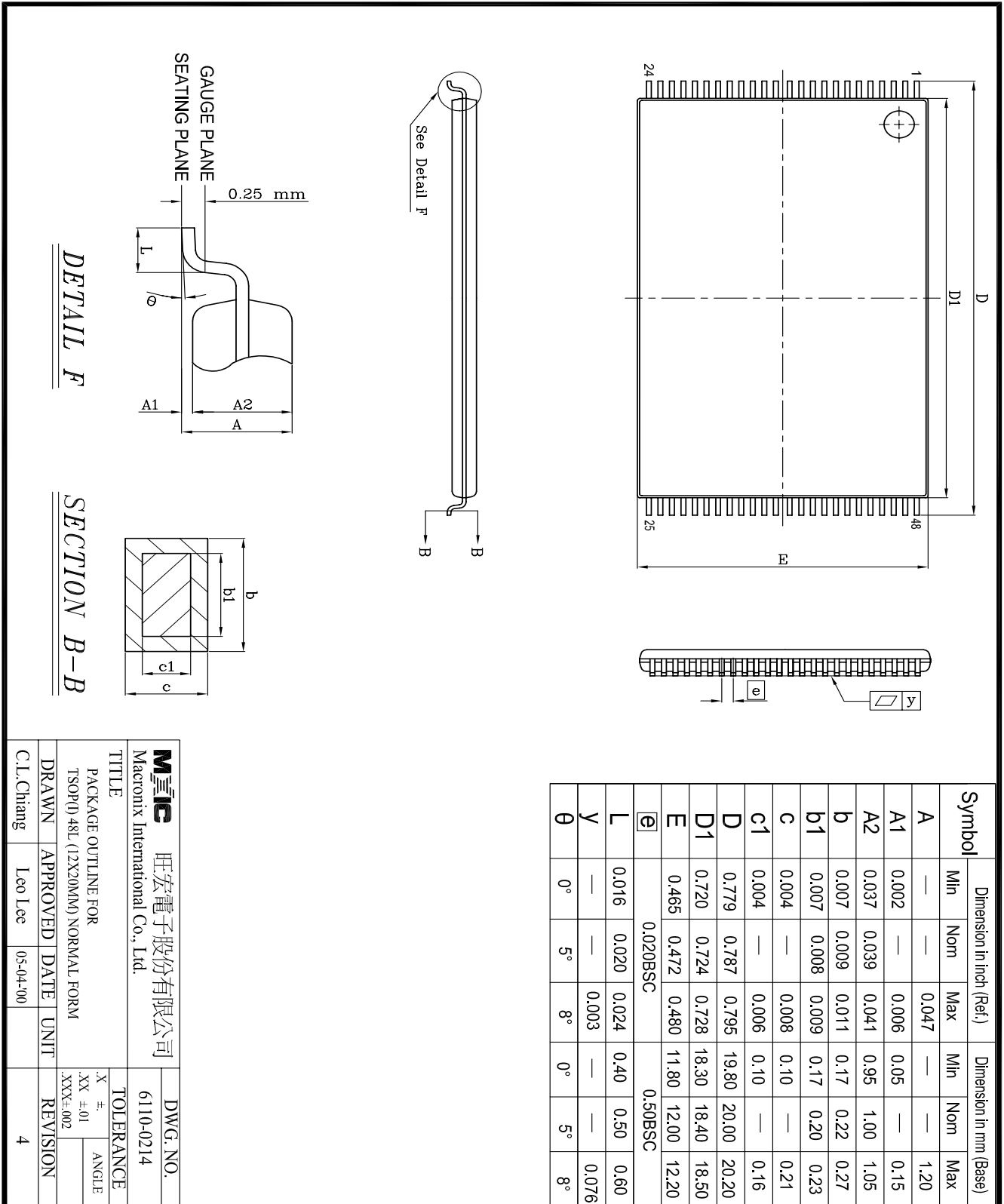
Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b	0.41 REF			0.016 REF		
c	0.20 REF			0.008 REF		
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e	1.27 REF			0.050 REF		
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—		5°	—		5°

JEDEC

DRAWN		C.L.Chang	APPROVED	Dennis Chang	DATE	05-03-01	UNIT	INCH	REVISION	2
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旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO.	61110-0207
TITLE		PACKAGE OUTLINE FOR SOP 44L (500 MIL)	
TOLERANCE		.X ±	ANGLE
		XX ±.01	ROUGHNESS
		.XXX±.002	

48-PIN PLASTIC TSOP



DETAIL F

SECTION B-B

Mxic 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0214	
TITLE PACKAGE OUTLINE FOR TSOP(D) 48L (12X20MM) NORMAL FORM			
DRAWN C.L.Chiang		APPROVED Leo Lee	
DATE 05-04-00		UNIT 4	
REVISION		REVISION	
TOLERANCE .X ±.01 .XX ±.01 .XXX ±.002		ANGLE	



REVISION HISTORY

Revision	Description	Page	Date
1.4	Add new 44pin TSOP (type 2)		Jul/17/1998
1.5	AC CHARACTERISTICS tOH 10ns-->0ns	P3	FEB/01/1999
1.6	Correct Typing error	P1	JUL/16/2001
	Modify Package Information	P5~7	
1.7	Added MX23L8100TI-10 in Order Information	P1	AUG/20/2001



MX23L8100

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