MX29LV161T/B

16M-BIT [2Mx8/1Mx16] CMOS SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

- Extended single - supply voltage range 2.7V to 3.6V
- 2,097,152 x 8/1,048,576 x 16 switchable
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- Fast access time: 70/90ns
- Low power consumption
  - 20mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - Byte/word Programming (9us/11us typical)
  - Sector Erase (Sector structure 16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x31)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase.
- Status Reply
  - $\overline{\text{Data}}$ polling & Toggle bit for detection of program and erase operation completion.
- Ready/$\overline{\text{Busy}}$ pin (RY/$\overline{\text{BY}}$)
  - Provides a hardware method of detecting program or erase operation completion.
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Tempoary sector unprotect allows code changes in previously locked sectors.
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 2.3V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
  - 48 Ball CSP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash

GENERAL DESCRIPTION

The MX29LV161T/B is a 16-mega bit Flash memory organized as 2M bytes of 8 bits or 1M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV161T/B is packaged in 44-pin SOP, 48-pin TSOP, and 48CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV161T/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV161T/B has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

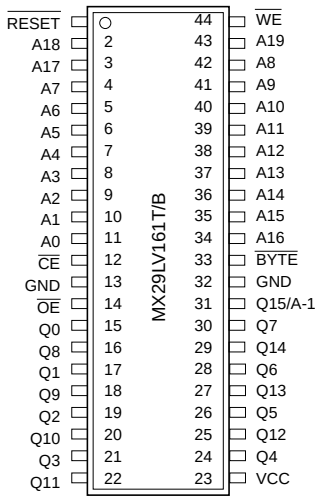
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV161T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV161T/B uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

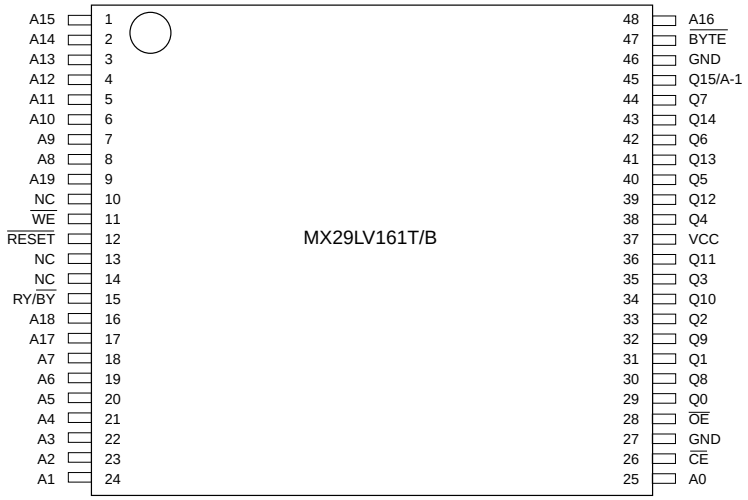
44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BYTE}$	Word/Byte Selction input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{OE}$	Output Enable Input
RY/$\overline{BY}$	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

48 TSOP (Standard Type) (12mm x 20mm)



48-Ball CSP 8mm x 13mm (Ball Pitch=0.8mm) Top View, Balls Facing Down

	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	$\overline{BYTE}$	Q15/A-1	GND
5	A9	A8	A10	A11	Q7	Q14	Q13	Q6
4	$\overline{WE}$	$\overline{RESET}$	NC	A19	Q5	Q12	VCC	Q4
3	RY/$\overline{BY}$	NC	A18	NC	Q2	Q10	Q11	Q3
2	A7	A17	A6	A5	Q0	Q8	Q9	Q1
1	A3	A4	A2	A1	A0	$\overline{CE}$	$\overline{OE}$	GND

BLOCK STRUCTURE

Table 1: MX29LV161T SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode(x8)	Word Mode(x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	000000-00FFFF	00000-07FFF	0	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA15	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA16	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA17	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA18	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA19	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA20	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA21	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA22	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA23	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA24	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA25	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA26	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA27	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA28	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA29	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA30	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-F7FFF	1	1	1	1	0	X	X	X
SA31	32Kbytes	16Kwords	1F0000-1F7FFF	F8000-FBFFF	1	1	1	1	1	0	X	X
SA32	8Kbytes	4Kwords	1F8000-1F9FFF	FC000-ECFFF	1	1	1	1	1	1	0	0
SA33	8Kbytes	4Kwords	1FA000-1FBFFF	FD000-FDFFF	1	1	1	1	1	1	0	1
SA34	16Kbytes	8Kwords	1FC000-1FFFFF	FE000-FFFFF	1	1	1	1	1	1	1	X

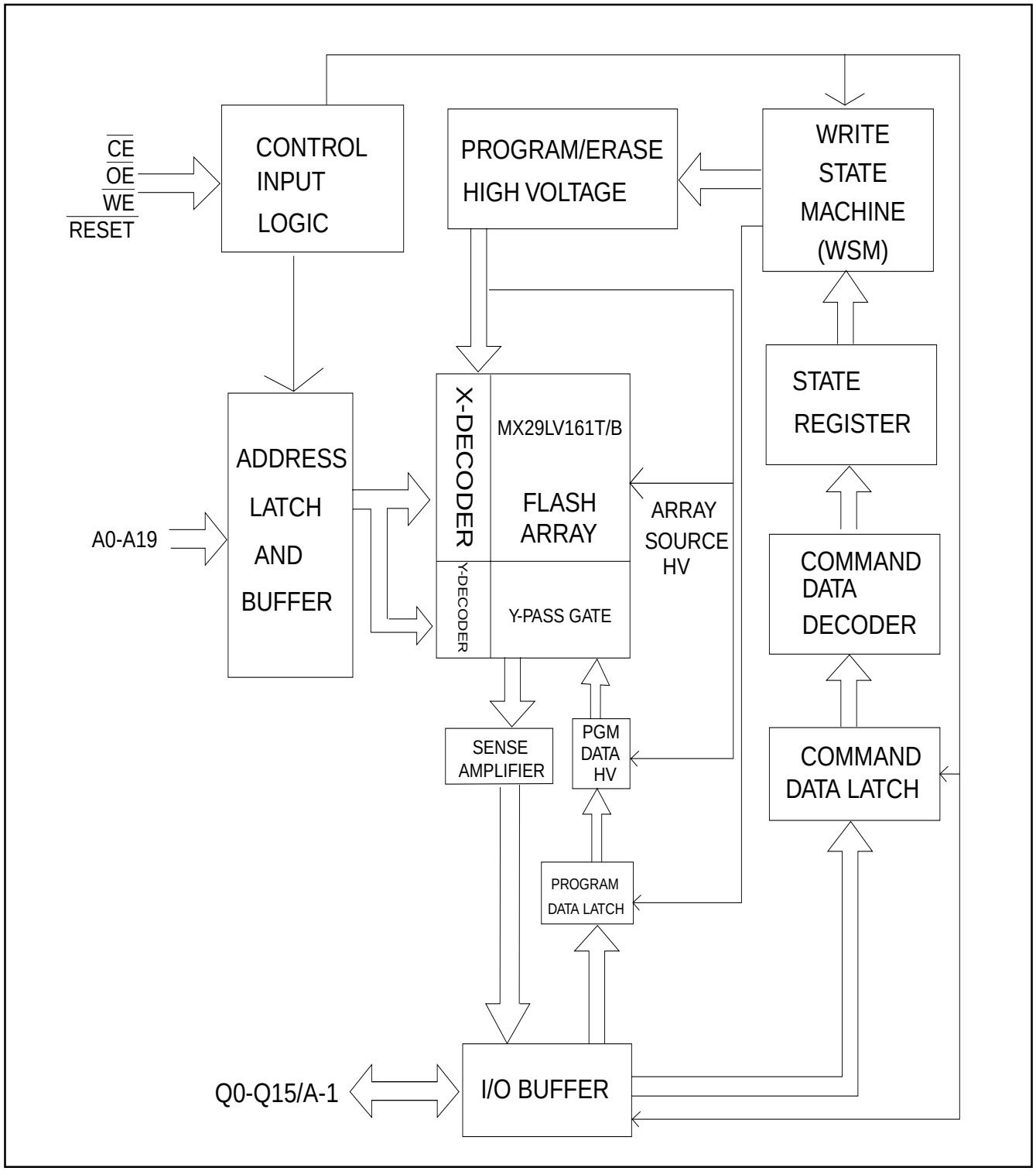
Note: Byte mode:address range A19:A-1, word mode:address range A19:A0.

Table 2: MX29LV161B SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	000000-003FFF	00000-01FFF	0	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	004000-005FFF	02000-02FFF	0	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	006000-007FFF	03000-03FFF	0	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	008000-00FFFF	04000-07FFF	0	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA19	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA20	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA21	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA22	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA23	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA24	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA25	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA26	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA27	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA28	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA29	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA30	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA31	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA32	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA33	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-FFFFF	1	1	1	1	0	X	X	X
SA34	64Kbytes	32Kwords	1F0000-1FFFFF	F8000-FFFFF	1	1	1	1	1	X	X	X

Note: Byte mode:address range A19:A-1, word mode:address range A19:A0.

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29LV161T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29LV161T/B is less than 10 seconds.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. The device provides an unlock bypass mode with faster programming. Only two write cycles are needed to program a word or byte, instead of four. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation. Refer to write operation status, table7, for more information on these status bits.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 25 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LV161T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device. An erase operation can erase one sector, multiple sectors, or the entire device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the erasing operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV161T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

AUTOMATIC SELECT

The auto select mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on Q7~Q0. This mode is mainly adapted for programming equipment on the device to be programmed with its programming algorithm. When programming by high voltage method, automatic select mode requires VID (11.5V to 12.5V) on address pin A9 and other address pin A6, A1 and A0 as referring to Table 3. In addition, to access the automatic select codes in-system, the host can issue the automatic se-

lect command through the command register without requiring VID, as shown in table4.

To verify whether or not sector being protected, the sector address must appear on the appropriate highest order address bit (see Table 1 and Table 2). The rest of address bits, as shown in table3, are don't care. Once all necessary bits have been set as required, the programming equipment may read the corresponding identifier code on Q7~Q0.

TABLE 3. MX29LV161T/B AUTO SELECT MODE BUS OPERATION (A9=VID)

Description	Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	A19 | A12	A11 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	Q15~Q0
Read Silicon ID Manfacturer Code		L	L	H	H	X	X	VID	X	L	X	L	L	C2H
Read Silicon ID	Word	L	L	H	H	X	X	VID	X	L	X	L	H	22C4H
(Top Boot Block)	Byte	L	L	H	H	X	X	VID	X	L	X	L	H	XXC4H
Device ID	Word	L	L	H	H	X	X	VID	X	L	X	L	H	2249H
(Bottom Boot Block)	Byte	L	L	H	H	X	X	VID	X	L	X	L	H	XX49H
Sector Protection Verification		L	L	H	H	SA	X	VID	X	L	X	H	L	XX01H (protected) / XX00H (unprotected)

NOTE:SA=Sector Address, X=Don't Care, L=Logic Low, H=Logic High

TABLE 4. MX29LV161T/B COMMAND DEFINITIONS

Command		Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycle	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset		1	XXXH	F0H										
Read		1	RA	RD										
Read Silicon ID	Word	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	ADI	DDI				
Sector Protect Verify	Word	4	555H	AAH	2AAH	55H	555H	90H	(SA)	XX00H				
									x02H	XX01H				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	(SA)	00H				
									x04H	01H				
Porgram	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
	Byte	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD				
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA	30H
Sector Erase Suspend		1	XXXH	B0H										
Sector Erase Resume		1	XXXH	30H										

Note:

1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacturer code,A1=0, A0 = 1 for device code. A2-A18=do not care. (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, C4H/49H (x8) and 22C4H/2249H (x16) for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address of the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 in word mode/AAAH or 555H to Address A10~A-1 in byte mode.
   Address bit A11~A19=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A19 in either state.
4. For Sector Protect Verify operation:If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

TABLE 5. MX29LV161T/B BUS OPERATION

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RESET	ADDRESS								Q0~Q7	Q8~Q15	
					A19 | A11	A10	A9	A8 | A7	A6	A5 | A2	A1	A0		BYTE =VIH	BYTE =VIL
Read	L	L	H	H	AIN								Dout	Dout	=High Z DQ15=A-1
Write	L	H	L	H	AIN								DIN(3)	DIN	
Reset	X	X	X	L	X								High Z	High Z	High Z
Temproary sector unlock	X	X	X	VID	AIN								DIN	DIN	High Z
Output Disable	L	H	H	H	X								High Z	High Z	High Z
Standby	Vcc± 0.3V	X	X	Vcc± 0.3V	X								High Z	High Z	High Z
Sector Protect	L	H	L	VID	SA	X	X	X	L	X	H	L	DIN	X	X
Chip Unprotect	L	H	L	VID	X	X	X	X	H	X	H	L	DIN	X	X
Sector Protection Verify	L	L	H	H	SA	X	VID	X	L	X	H	L	CODE(5)	X	X

NOTES:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 4.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 4 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/XX00H means unprotected.
   Code=01H/XX01H means protected.
6. A19~A12=Sector address for sector protect.
7. The sector protect and chip unprotect functions may also be implemented via programming equipment.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to VIL. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory contect occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the sysytem must drive $\overline{WE}$ and $\overline{CE}$ to VIL, and $\overline{OE}$ to VIH.

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors , or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data."section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal reqister (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

STANDBY MODE

When using both pins of $\overline{CE}$ and $\overline{RESET}$, the device enter CMOS Standby with both pins held at Vcc ± 0.3V. IF $\overline{CE}$ and $\overline{RESET}$ are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby currect will be larger. During Auto Algorithm operation, Vcc active current (Icc2) is required even $\overline{CE}$ = "H" until the operation is complated. The device can be read with standard access time (tCE) from either of these standby modes, before it is ready to read data.

OUTPUT DISABLE

With the $\overline{OE}$ input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

$\overline{RESET}$ OPERATION

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the $\overline{RESET}$ pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the $\overline{RESET}$ pluse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If $\overline{RESET}$ is held at VIL but not within VSS±0.3V, the standby current will be greater.

The $\overline{RESET}$ pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firm-ware from

the Flash memory.

If RESET is asserted during a program or erase operation, the RY/BY pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The sysytem can thus monitor RY/BY to determine whether the reset operation is complete. If RESET is asserted when a program or erase operation is commpleted within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET pin returns to VIH.

Refer to the AC Characteristics tables for RESET parameters and to Figure 22 for the timing diagram.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage(VID). However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29LV161T/Bcontains a Silicon-ID-Read operation to supple traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H/00C2H. A read cycle with A1=VIL, A0=VIH returns the device code of C4H/22C4H for MX29LV161T, 49H/2249H for MX29LV161B.

SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H or sector erase command 30H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 7), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE or CE pulse, whichever happens first in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 6. SILICON ID CODE

Pins		A0	A1	Q15~Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	Word	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
	Byte	VIL	VIL	X	1	1	0	0	0	0	1	0	C2H
Device code	Word	VIH	VIL	22H	1	1	0	0	0	1	0	0	22C4H
for MX29LV161T	Byte	VIH	VIL	X	1	1	0	0	0	1	0	0	C4H
Device code	Word	VIH	VIL	22H	0	1	0	0	1	0	0	1	2249H
for MX29LV161B	Byte	VIH	VIL	X	0	1	0	0	1	0	0	1	49H
Sector Protection	Word	X	VIH	X	0	0	0	0	0	0	0	1	01H (Protected)
Verification	Byte	X	VIH	X	0	0	0	0	0	0	0	0	00H (Unprotected)

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See rase Suspend/Erase Resume Commands" for more infor-mation on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence be-fore programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins,however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading
array data (also applies during Erase Suspend).

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Sector Erase Set-up command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while the command(data) is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Each successive sector load cycle started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later must begin within 50us from the rising edge of the preceding $\overline{WE}$ or $\overline{CE}$, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend Command is issued during the sector erase operation, the device requires a maximum 20us to suspend the sector erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to Erase Resume, program data to , or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

WORD/BYTE PROGRAM COMMAND SEQUENCE

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 4 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/$\overline{BY}$. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Em-

bedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operat ion. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1" ," or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY. Table 7 and the following subsections describe the functions of these bits. Q7, RY/BY, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Q7: Data Polling

The Data Polling bit, Q7, indicates to the host sys-tem whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Er ase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, $\overline{Data}$ Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{Data}$ Polling produces a "1" on Q7. This is analogous to the complement/true datum out-put described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0"." The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchr onously with Q0-Q6 while Output Enable ($\overline{OE}$) is asserted low.

RY/$\overline{BY}$:Ready/Busy

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to Vcc.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.)If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 7 shows the outputs for RY/$\overline{BY}$ during write operation.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence(prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2 us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 7 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively eraseing (that is, the Automatic Erase alorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ or $\overline{CE}$, whichever happens first, in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 7 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfuly completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase op-

eration, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition will not appear if a user tries to program a non blank location without erasing. Please note that this is not a device failure condition since the device was incorrectly used.

Table 7. WRITE OPERATION STATUS

	Status		**Q7 (Note1)**	**Q6**	**Q5 (Note2)**	**Q3**	**Q2**	**RY/$\overline{BY}$**
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MX29LV161T/Bis designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on CE or WE will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE = VIL, CE = VIH or WE = VIH. To initiate a write cycle CE and WE must be a logical zero while OE is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

POWER-UP SEQUENCE

The MX29LV161T/Bpowers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

TEMPORARY SECTOR UNPROTECT

This feature allows temporary unprotection of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as un-protected sector. Once VID is remove from the RESET pin,all the previously protected sectors are protected again.

SECTOR PROTECTION

The MX29LV161T/Bfeatures hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and OE (suggest VID = 12V). Programming of the protection circuitry begins on the falling edge of the WE pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE and OE at VIL and WE at VIH). When A1=VIH, A0=VIL, A6=VIL, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses,except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT

The MX29LV161T/Balso features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ pins must be set at VIL. Pins A6 must be set to VIH. Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector.

It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, $\overline{OE}$, and

$\overline{RESET}$ (Note 2) . . . .-0.5 V to +12.5 V

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9, $\overline{OE}$, and $\overline{RESET}$ is -0.5 V. During voltage transitions, A9, $\overline{OE}$, and $\overline{RESET}$ may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Rat-ings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . . +3.0 V to 3.6 V

V_{CC} for full voltage range. . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

Table 8. DC CHARACTERISTICS TA = -40°C TO 85°C, VCC = 3V±10% (VCC=3.0~3.6V for MX29LV161T/B-70R, MX29LV161T/B-90R)

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS	
ILI	Input Leakage Current			± 1	uA	VIN = VSS to VCC	
ILIT	A9 Input Leakage Current			35	uA	VCC=VCC max; A9=12.5V	
ILO	Output Leakage Current			± 1	uA	VOUT = VSS to VCC, VCC=VCC max	
ICC1	VCC Active Read Currect		9	16	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	@5MHz
			2	4	mA	(Byte Mode)	@1MHz
			9	16	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	@5MHz
			2	4	mA	(Word Mode)	@1MHz
ICC2	VCC Active write Currect		20	30	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	
ICC3	VCC Standby Currect		0.2	5	uA	$\overline{CE}$; $\overline{RESET}$=VCC ± 0.3V	
ICC4	VCC Standby Currect During Reset (See Conditions)		0.2	5	uA	$\overline{RESET}$=VSS ± 0.3V	
ICC5	Automative sleep mode		0.2	5	uA	VIH=VCC ± 0.3V;VIL=VSS ± 0.3V	
VIL	Input Low Voltage(Note 1)	-0.5		0.8	V		
VIH	Input High Voltage	0.7xVCC		VCC+ 0.3	V		
VID	Voltage for Automative Select and Temporary Sector Unprotect	11.5		12.5	V	VCC=3.3V	
VOL	Output Low Voltage			0.45	V	IOL = 4.0mA, VCC= VCC min	
VOH1	Output High Voltage(TTL)	0.85xVCC				IOH = -2mA, VCC=VCC min	
VOH2	Output High Voltage (CMOS)	VCC-0.4				IOH = -100uA, VCC min	
VLKO	Low VCC Lock-out Voltage	2.3		2.5	V		

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for tACC +30ns.

AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 2.7V~3.6V (VCC=3.0~3.6V for MX29LV161T/B-70R, MX29LV161T/B-90R)

Table 9. READ OPERATIONS

			29LV161T/B-70		29LV161T/B-70R (Note3)			
Symbol	**PARAMETER**		**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tRC	Read Cycle Time (Note 1)			70		70	ns	
tACC	Address to Output Delay			70		70	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay			70		70	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay			30		30	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note2)		0	25	0	25	ns	$\overline{CE}$=VIL
tOEH	Output Enable	Read	0		0		ns	
	Hold Time	Toggle and Data Polling	10		10		ns	
tOH	Address to Output hold		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

			29LV161T/B-90		29LV161T/B-90R (Note3)			
Symbol	**PARAMETER**		**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tRC	Read Cycle Time (Note 1)			90		90	ns	
tACC	Address to Output Delay			90		90	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay			90		90	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay			35		35	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note2)		0	30	0	30	ns	$\overline{CE}$=VIL
tOEH	Output Enable	Read	0		0		ns	
	Hold Time	Toggle and Data Polling	10		10		ns	
tOH	Address to Output hold		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

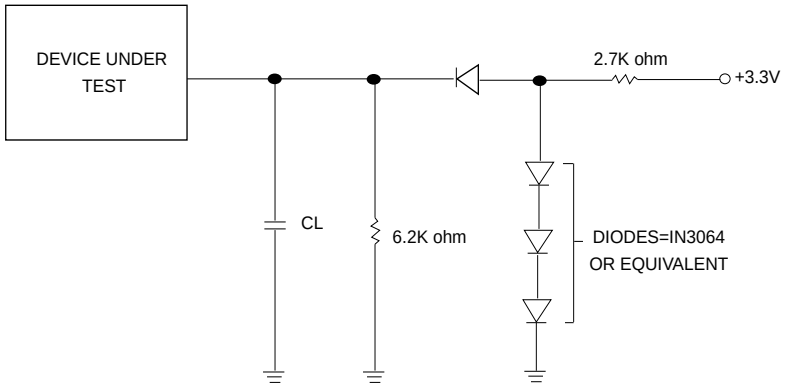
TEST CONDITIONS:

- Input pulse levels: 0V/3.0V.
- Input rise and fall times is equal to or less than 5ns.
- Output load: 1 TTL gate + 100pF (Including scope and jig), for 29LV161T/B-90. 1 TTL gate + 30pF (Including scope and jig) for 29LV161T/B-70 and 29LV161T/B-70R.
- Reference levels for measuring timing: 1.5V.

NOTE:

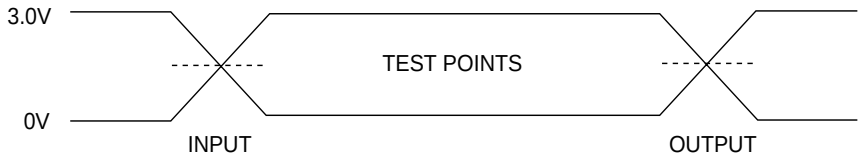
1. Not 100% tested.
2. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
3. 29LV161T/B-70R & 29LV161T/B-90R operates at VCC=3.0~3.6V.

SWITCHING TEST CIRCUITS



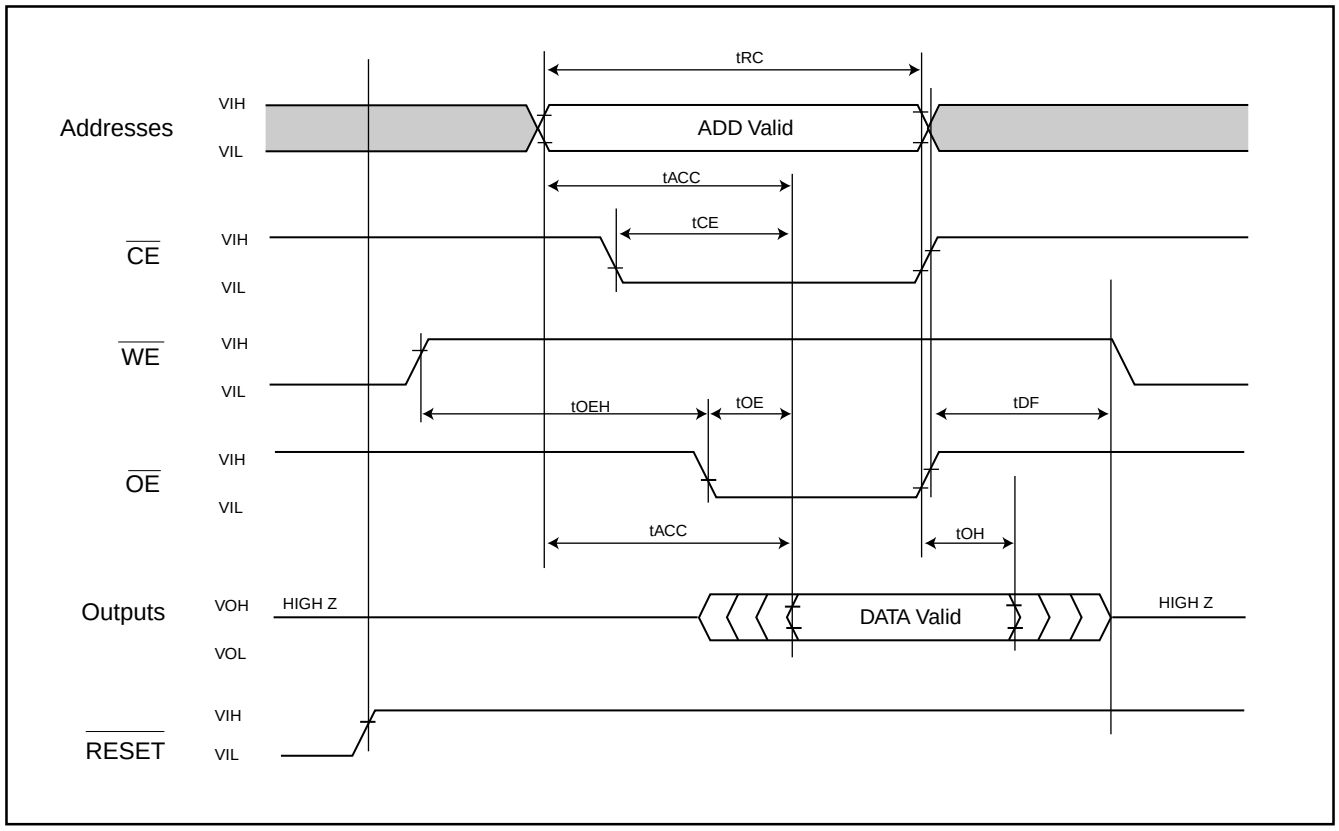
CL=100pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

Figure 1. READ TIMING WAVEFORMS



AC CHARACTERISTICS **TA = -40°C to 85°C, VCC = 2.7V~3.6V**
(VCC=3.0~3.6V for MX29LV161T/B-70R, MX29LV161T/B-90R)

Table 10. Erase/Program Operations

		29LV161T/B-70(R),		29LV161T/B-90(R),		
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**
tWC	Write Cycle Time (Note 1)	70		90		ns
tAS	Address Setup Time	0		0		ns
tAH	Address Hold Time	45		45		ns
tDS	Data Setup Time	35		45		ns
tDH	Data Hold Time	0		0		ns
tOES	Output Enable Setup Time	0		0		ns
tGHWL	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)	0		0		ns
tCS	$\overline{CE}$ Setup Time	0		0		ns
tCH	$\overline{CE}$ Hold Time	0		0		ns
tWP	Write Pulse Width	35		35		ns
tWPH	Write Pulse Width High	30		30		ns
tWHWH1	Programming Operation (Note 2) (Byte/Word program time)	9/11(typ.)		9/11(typ.)		us
tWHWH2	Sector Erase Operation (Note 2)	0.7(typ.)		0.7(typ.)		sec
tVCS	VCC Setup Time (Note 1)	50		50		us
tRB	Recovery Time from RY/$\overline{BY}$	0		0		ns
tBUSY	Sector Erase Valid to RY/$\overline{BY}$ Delay		90		90	ns
	Chip Erase Valid to RY/$\overline{BY}$ Delay		90		90	ns
	Program Valid to RY/$\overline{BY}$ Delay		90		90	ns
tWPP1	Write pulse width for sector protect (A9, $\overline{OE}$ Control)	100ns	10us(typ.)	100ns	10us(typ.)	
tWPP2	Write pulse width for sector unprotect (A9, $\overline{OE}$ Control)	100ns	12ms(typ.)	100ns	12ms(typ.)	

NOTES:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

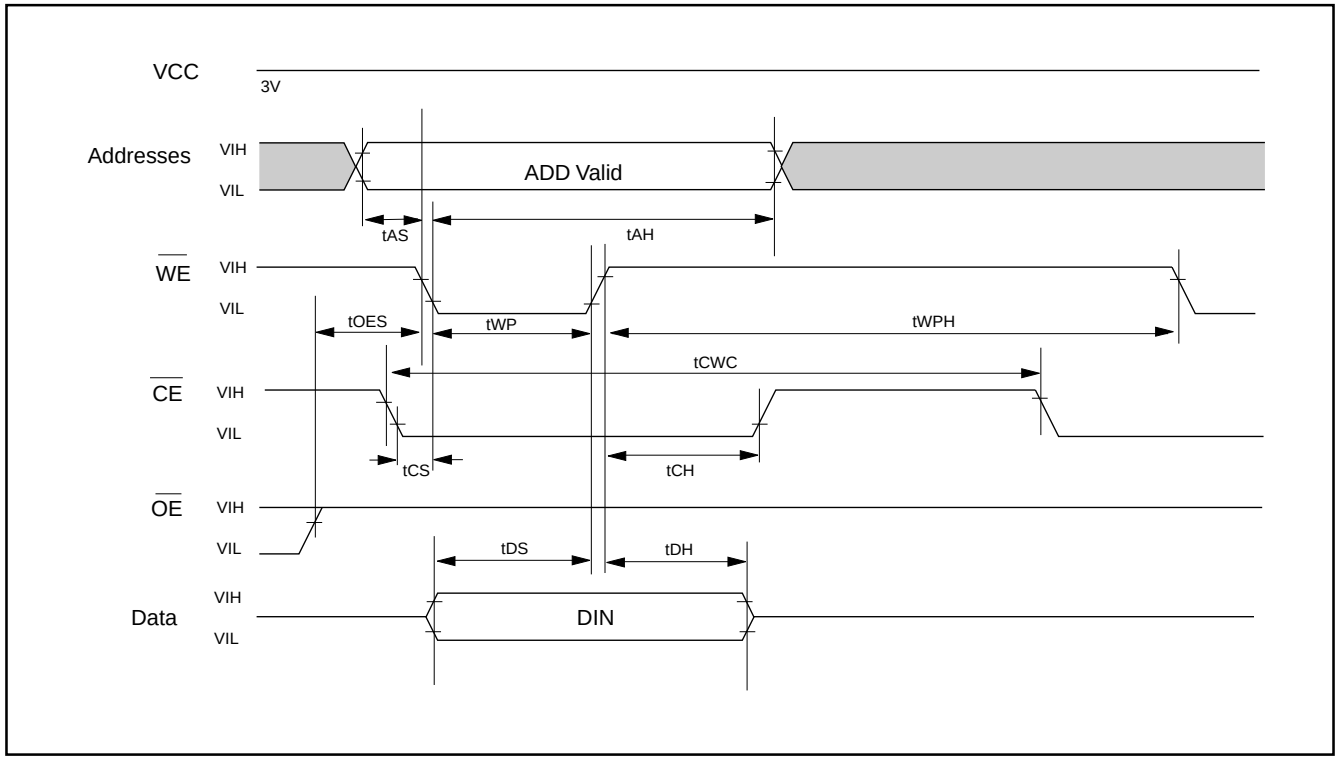
AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 2.7V~3.6V (VCC=3.0~3.6V for MX29LV161T/B-70R, MX29LV161T/B-90R)

Table 11. Alternate $\overline{CE}$ Controlled Erase/Program Operations

			29LV161T/B-70(R)		29LV161T/B-90(R)		
SYMBOL	**PARAMETER**		**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**
tWC	Write Cycle Time (Note 1)		70		90		ns
tAS	Address Setup Time		0		0		ns
tAH	Address Hold Time		45		45		ns
tDS	Data Setup Time		35		45		ns
tDH	Data Hold Time		0		0		ns
tOES	Output Enable Setup Time		0		0		ns
tGHEL	Read Recovery Time Before Write		0		0		ns
tWS	$\overline{WE}$ Setup Time		0		0		ns
tWH	$\overline{WE}$ Hold Time		0		0		ns
tCP	$\overline{CE}$ Pulse Width		35		35		ns
tCPH	$\overline{CE}$ Pulse Width High		30		30		ns
tWHWH1	Programming	Byte	9(Typ.)		9(Typ.)		us
	Operation(note2)	Word	11(Typ.)		11(Typ.)		us
tWHWH2	Sector Erase Operation (note2)		0.7(Typ.)		0.7(Typ.)		sec

NOTE:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

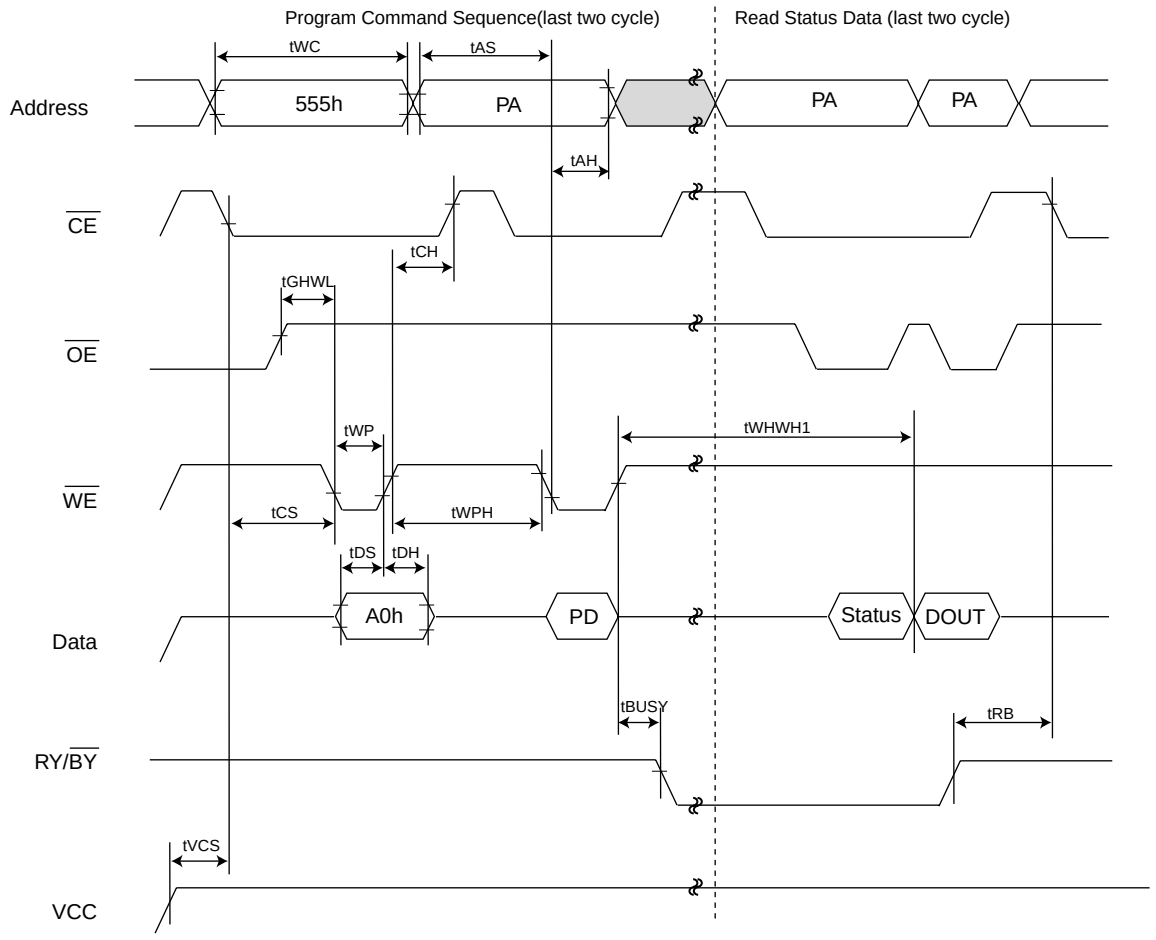
Figure 2. COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional verification by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic programming starts. Device outputs $\overline{DATA}$ during programming and $\overline{DATA}$ after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

Figure 3. AUTOMATIC PROGRAMMING TIMING WAVEFORM



NOTES:
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

Figure 4. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

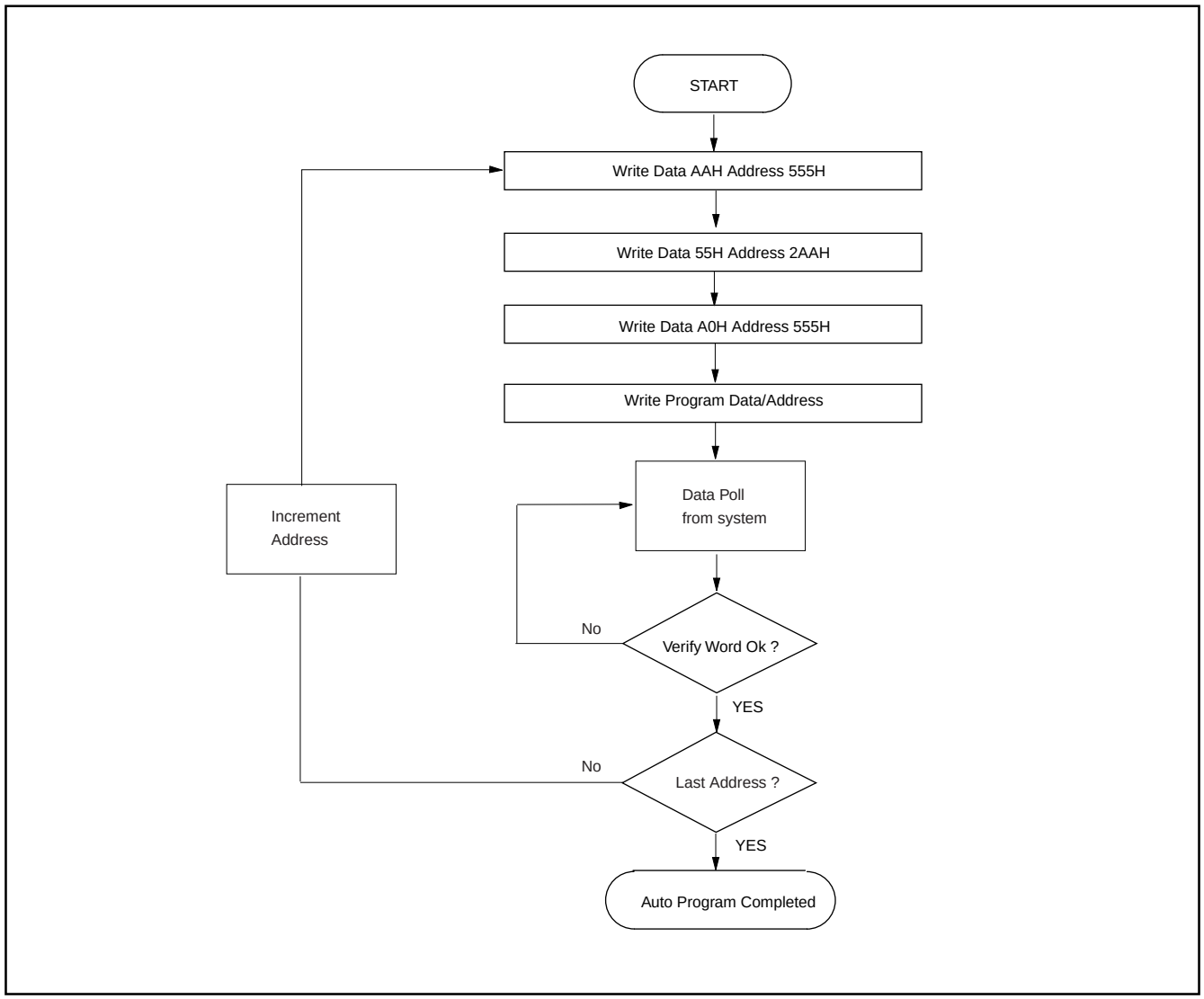
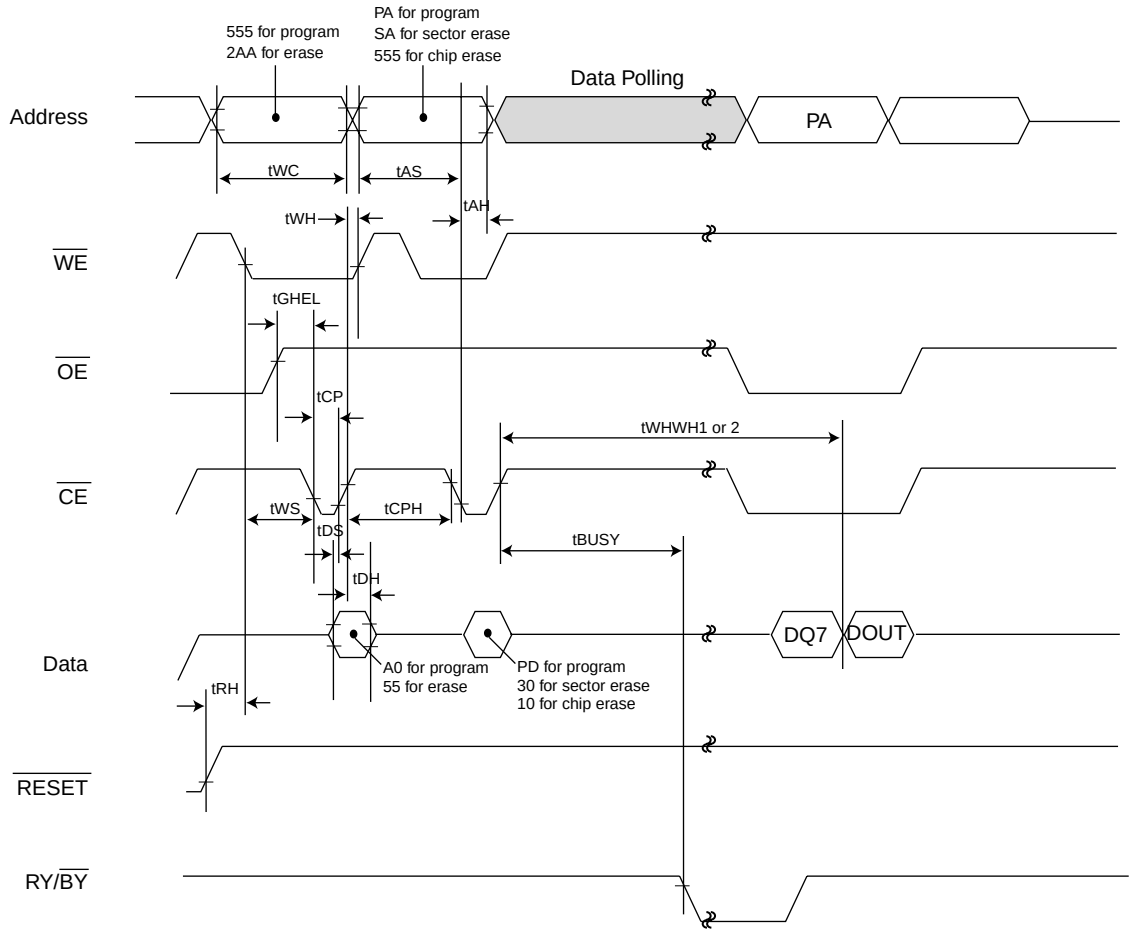


Figure 5. $\overline{CE}$ CONTROLLED PROGRAM TIMING WAVEFORM



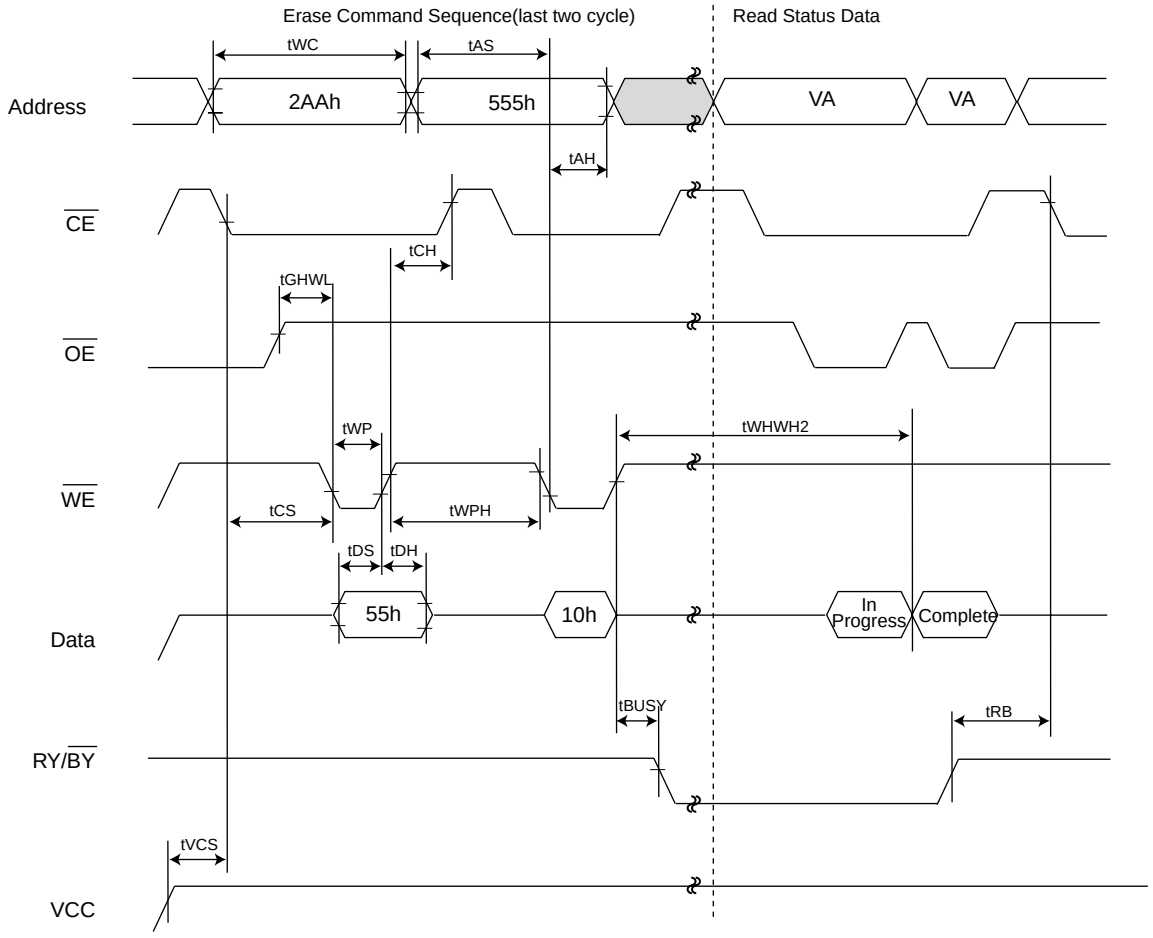
NOTES:

1.PA=Program Address, PD=Program Data, DOUT=Data Out, DQ7=complement of data written to device.
2.Figure indicates the last two bus cycles of the command sequence.

AUTOMATIC CHIP ERASE TIMING WAVEFORM

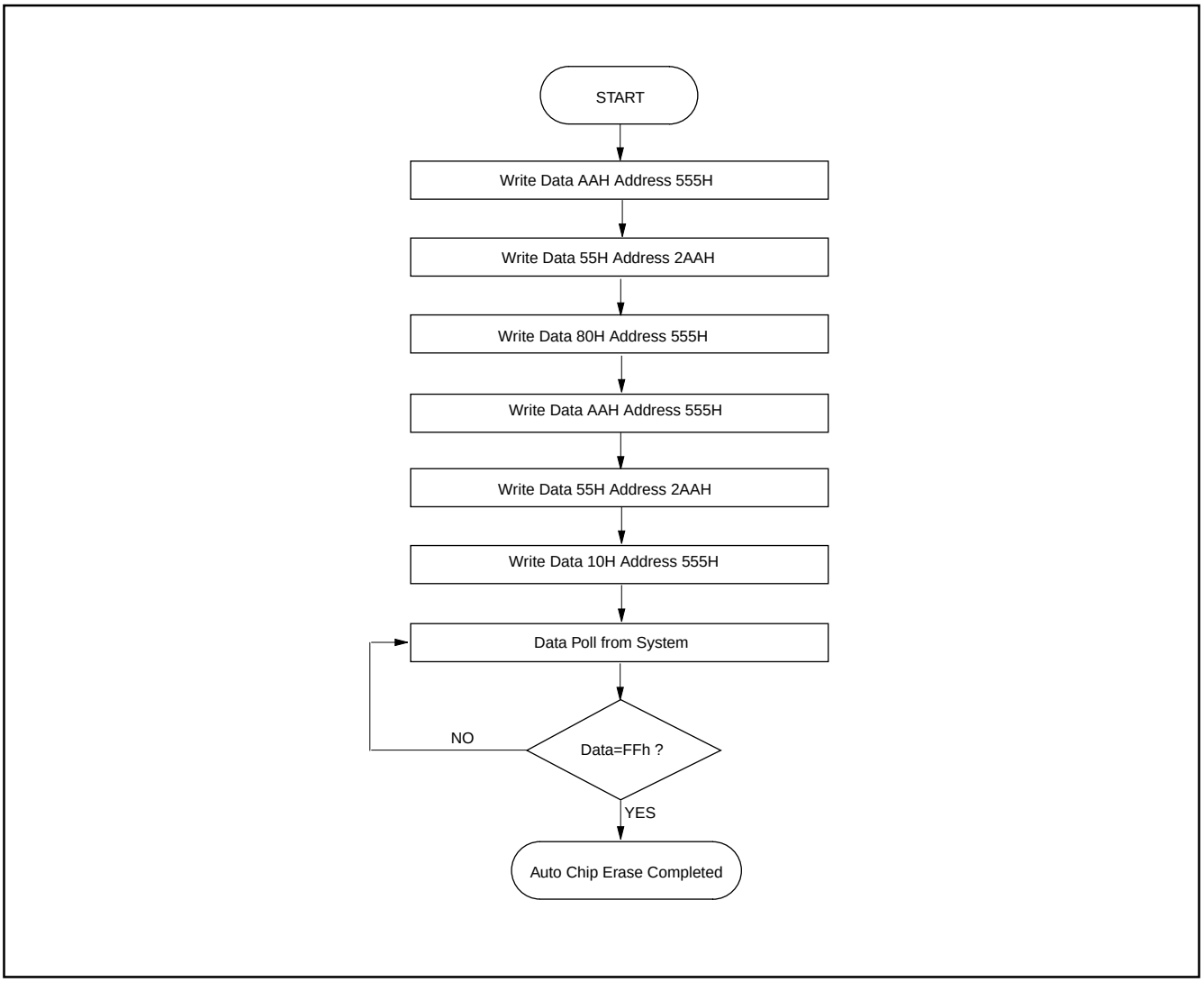
All data in chip are erased. External erase verification is not required because data is verified automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

Figure 6. AUTOMATIC CHIP ERASE TIMING WAVEFORM



NOTES:
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

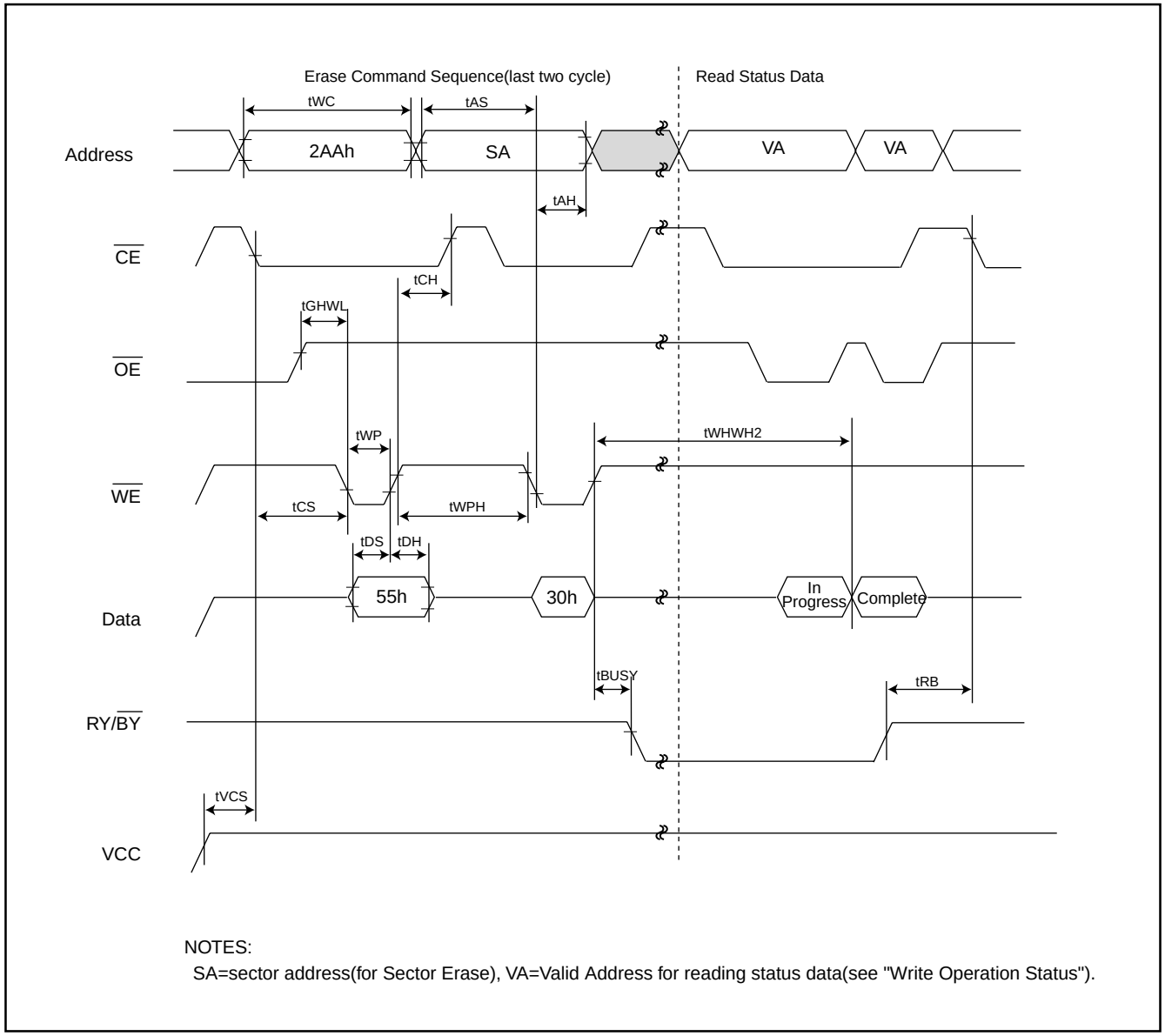
Figure 7. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector indicated by A12 to A19 are erased. External erase verify is not required because data are verified automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

Figure 8. AUTOMATIC SECTOR ERASE TIMING WAVEFORM



NOTES:
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Figure 9. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

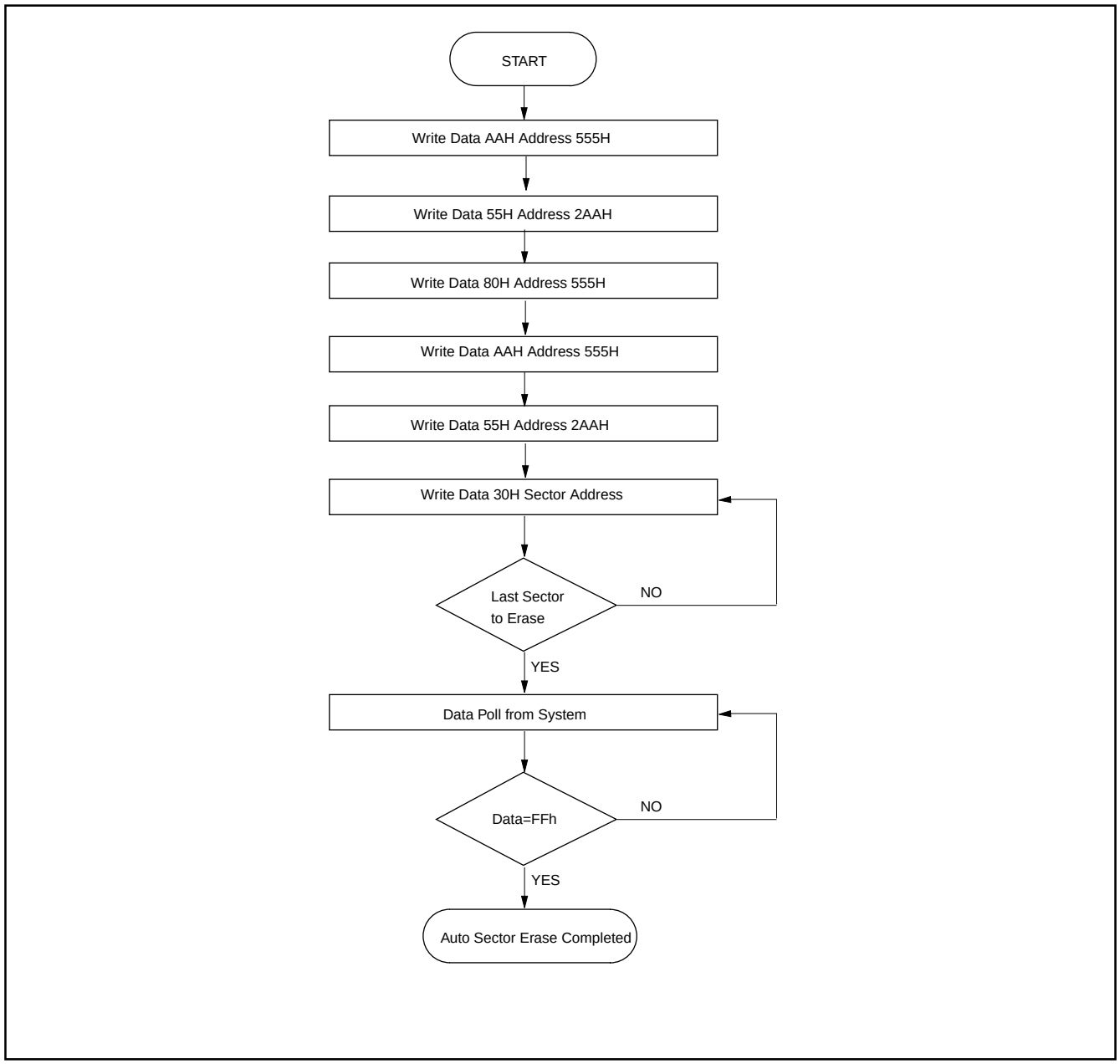


Figure 10. ERASE SUSPEND/ERASE RESUME FLOWCHART

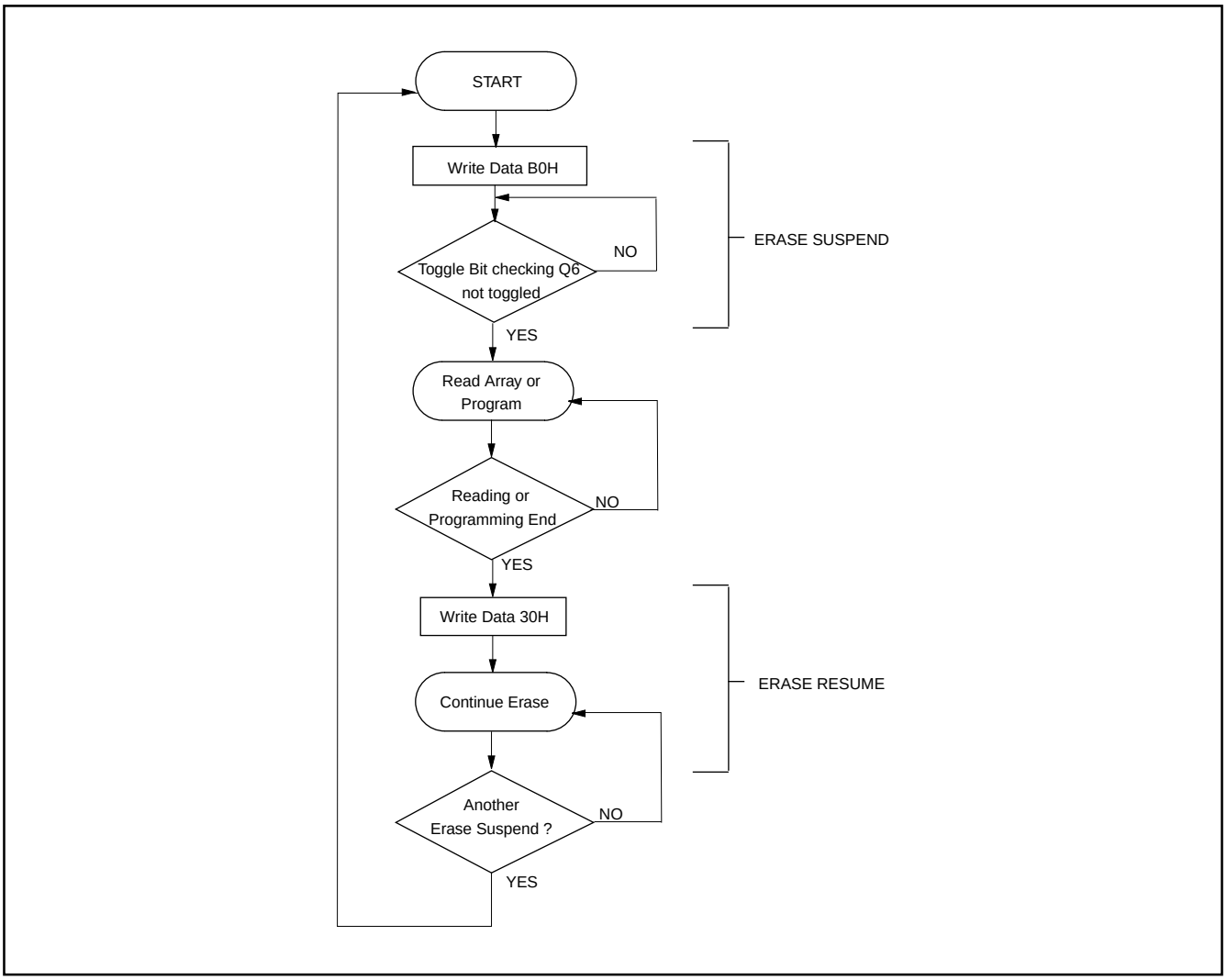
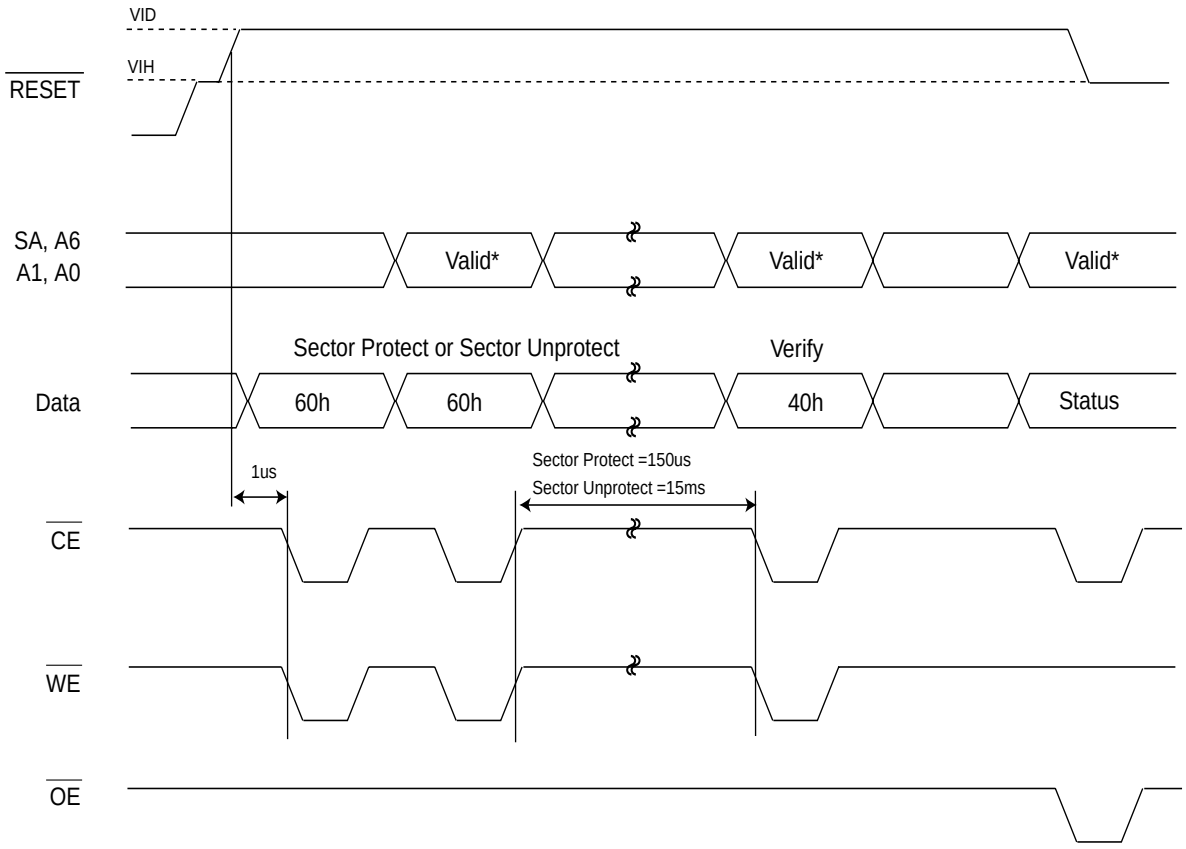


Figure 11. IN-SYSTEM SECTOR PROTECT/UNPROTECT TIMING WAVEFORM ($\overline{\text{RESET}}$ Control)



Note: When sector protect, A6=0, A1=1, A0=0. When sector unprotect, A6=1, A1=1, A0=0.

Figure 12. SECTOR PROTECT TIMING WAVEFORM(A9, $\overline{OE}$ Control)

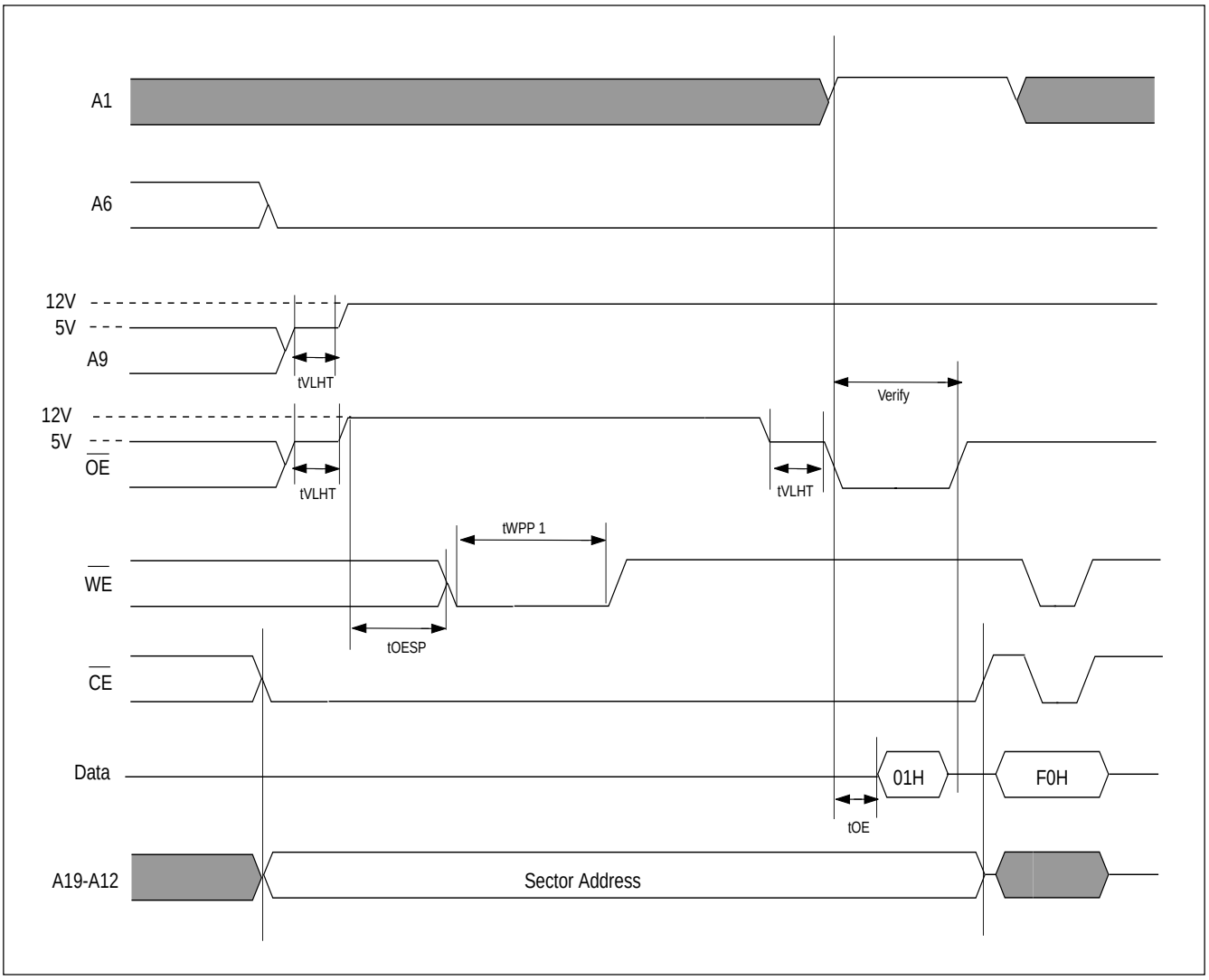


Figure 13. SECTOR PROTECTION ALGORITHM (A9, $\overline{OE}$ Control)

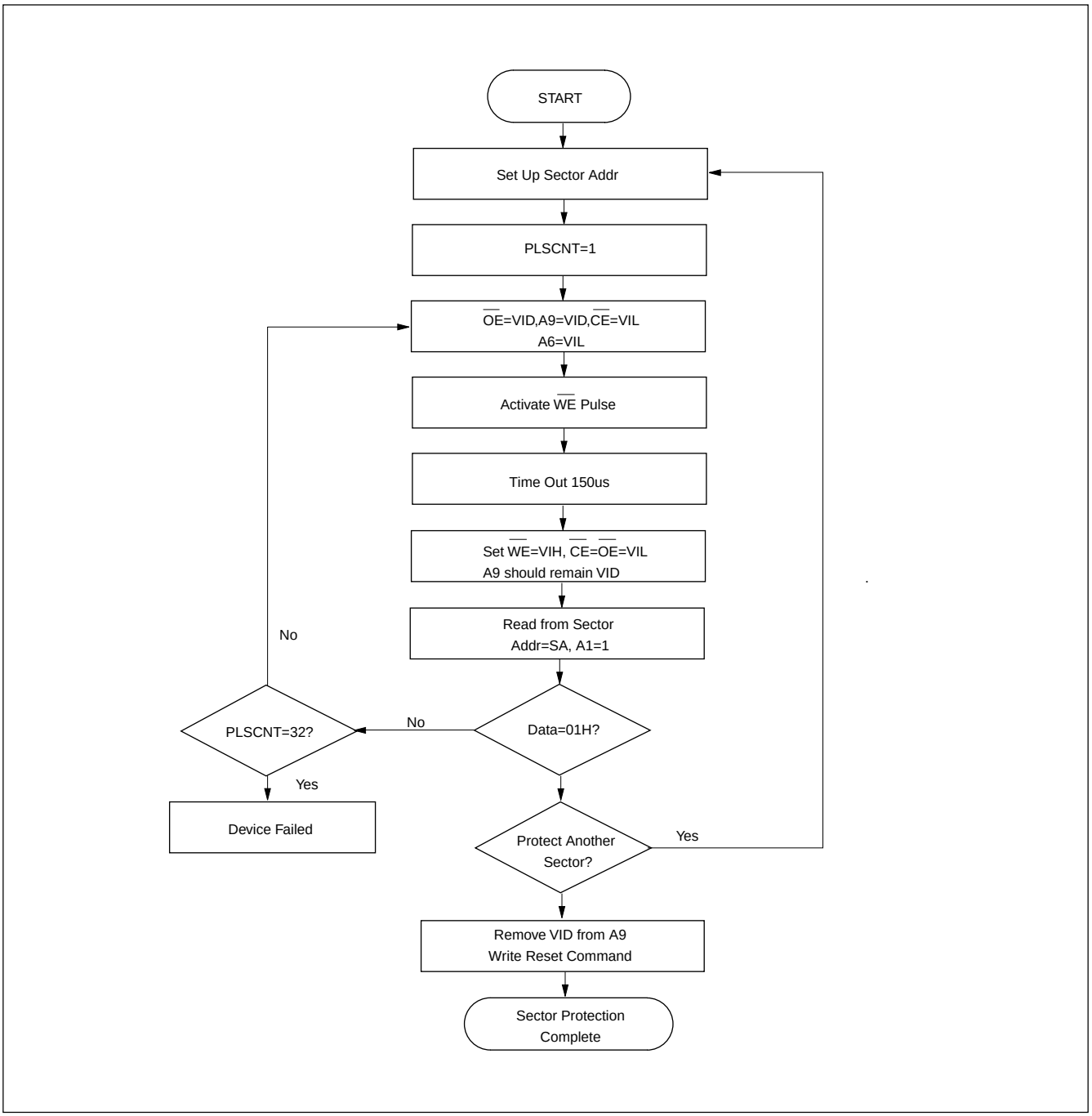


Figure 14. IN-SYSTEM SECTOR PROTECTION ALGORITHM WITH $\overline{\text{RESET}}$=VID

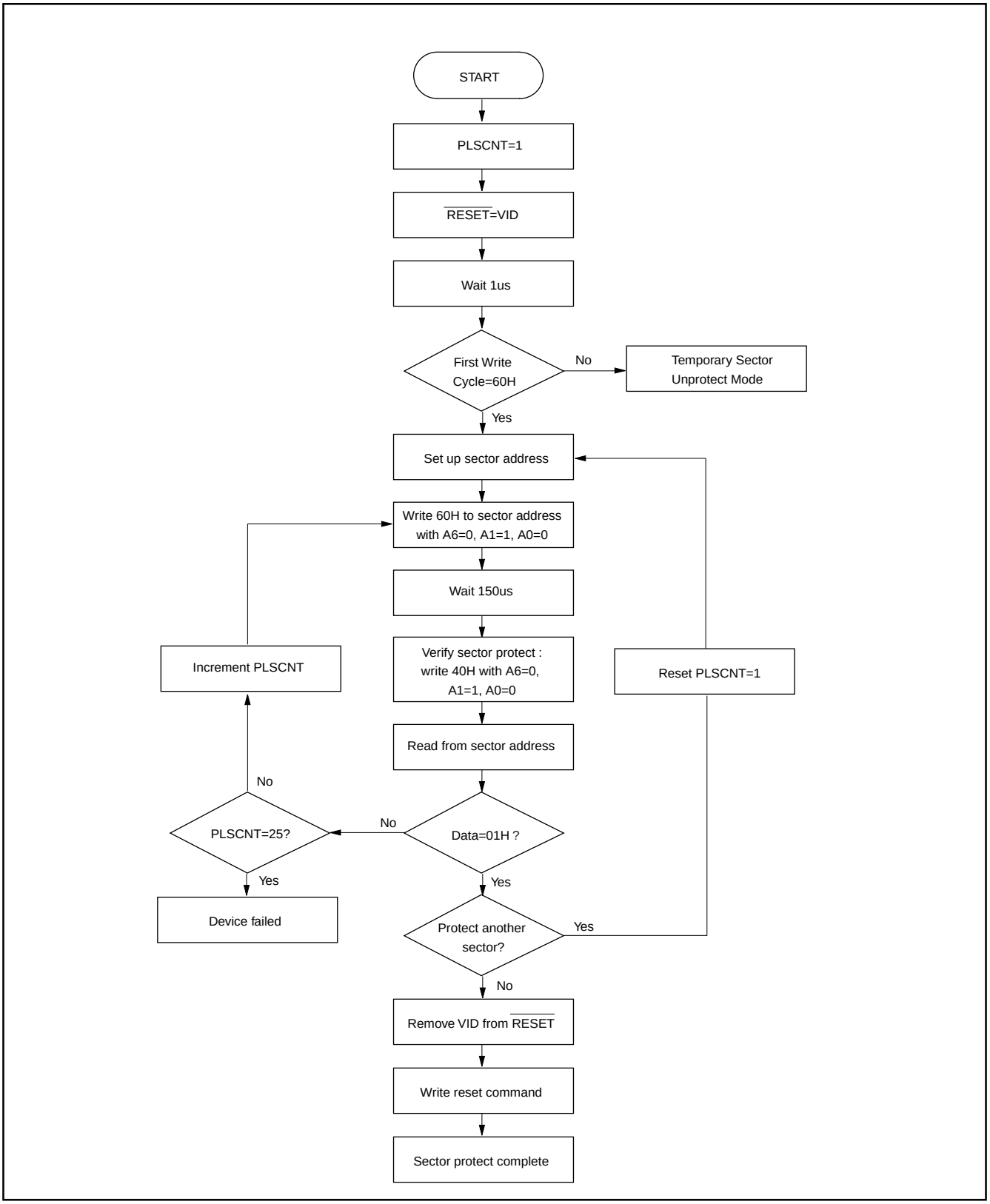


Figure 15. IN-SYSTEM SECTOR UNPROTECTION ALGORITHM WITH $\overline{\text{RESET}}$=VID

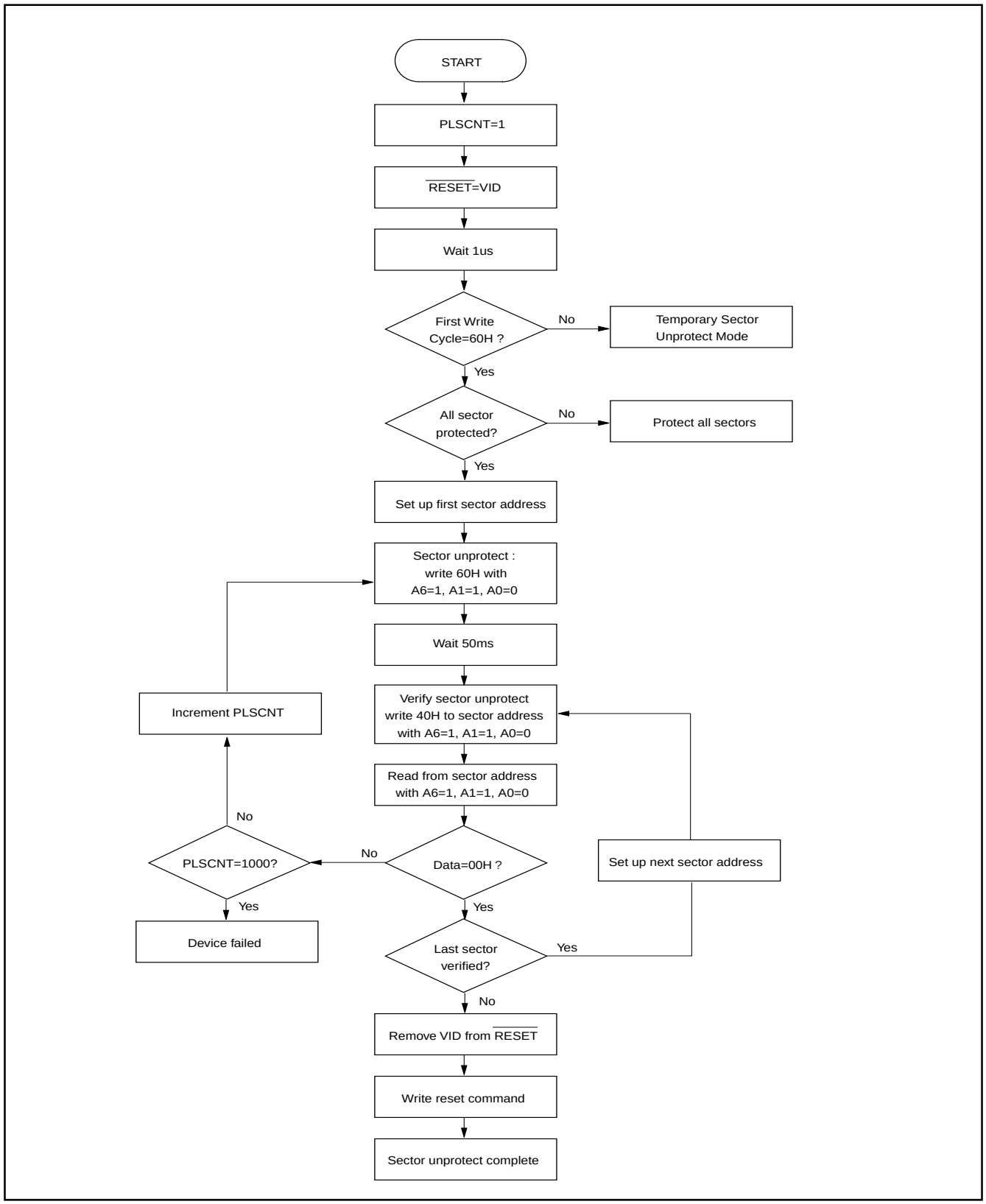
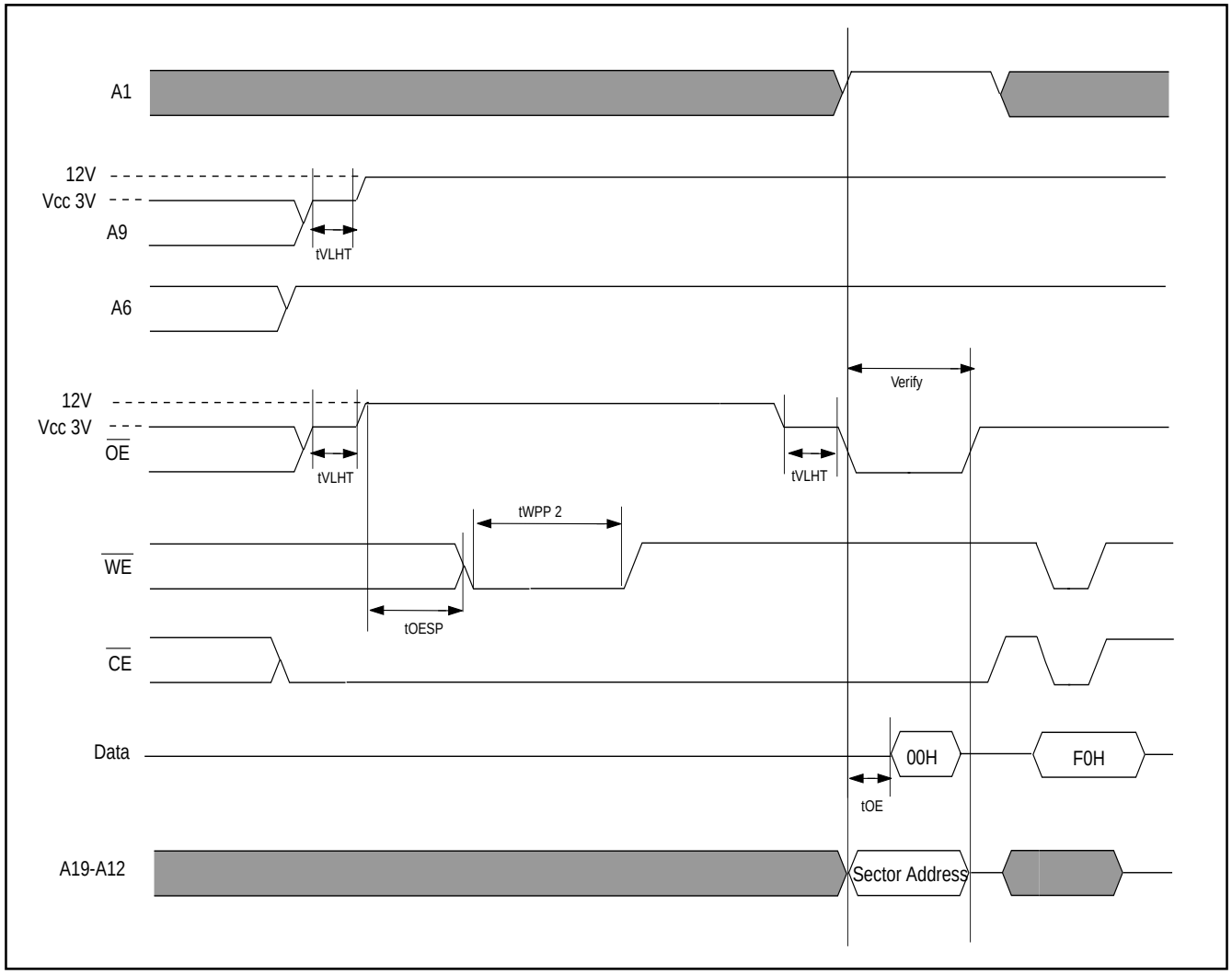
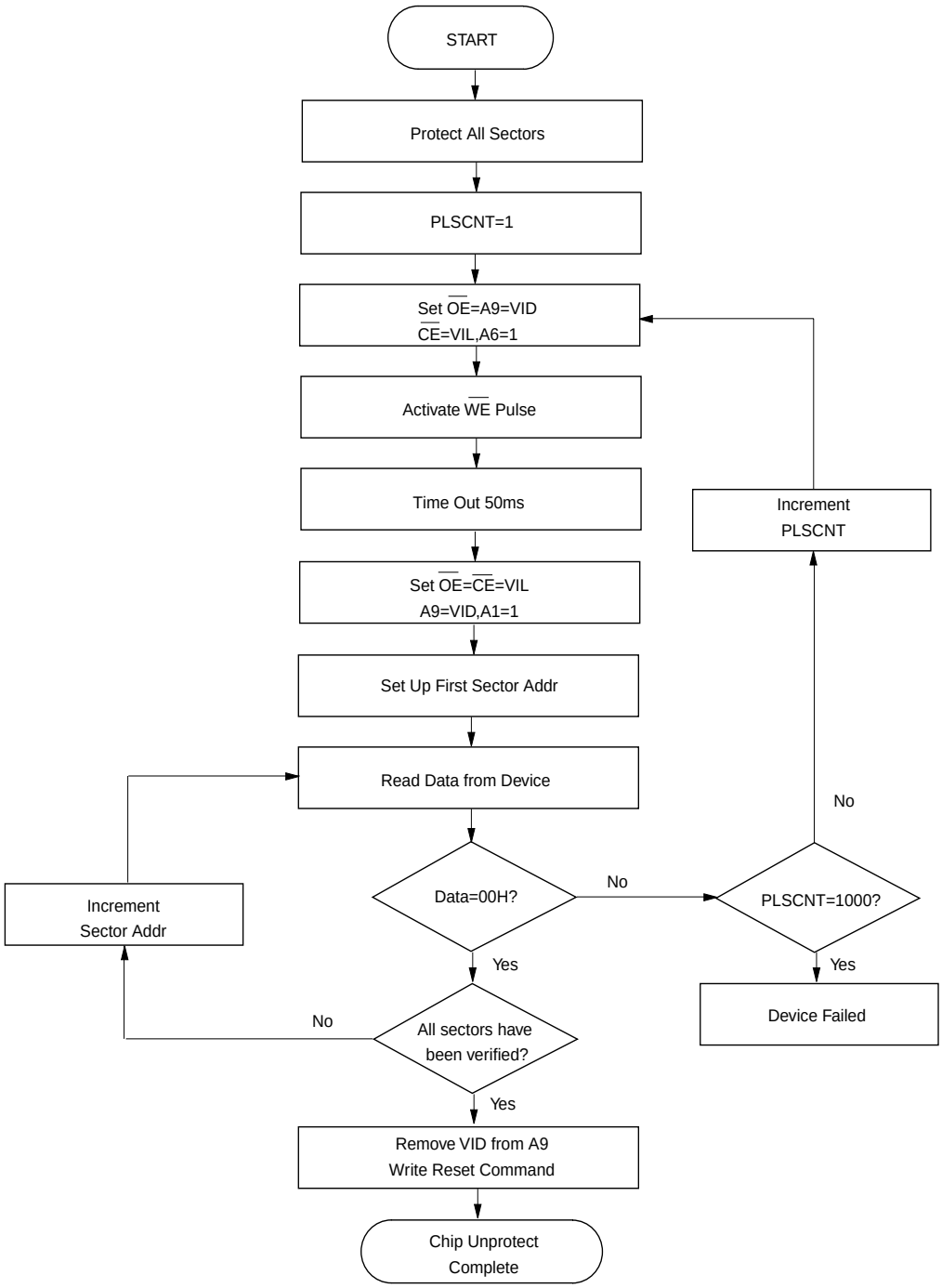


Figure 16. TIMING WAVEFORM FOR CHIP UNPROTECTION (A9, $\overline{OE}$ Control)



Notes: tVLHT (Voltage transition time)=4us min.
tWPP1 (Write pulse width for sector protect)=100ns min.
tWPP2 (Write pulse width for sector unprotect)=100ns min.
tOESP ($\overline{OE}$ setup time to $\overline{WE}$ active)=4us min.

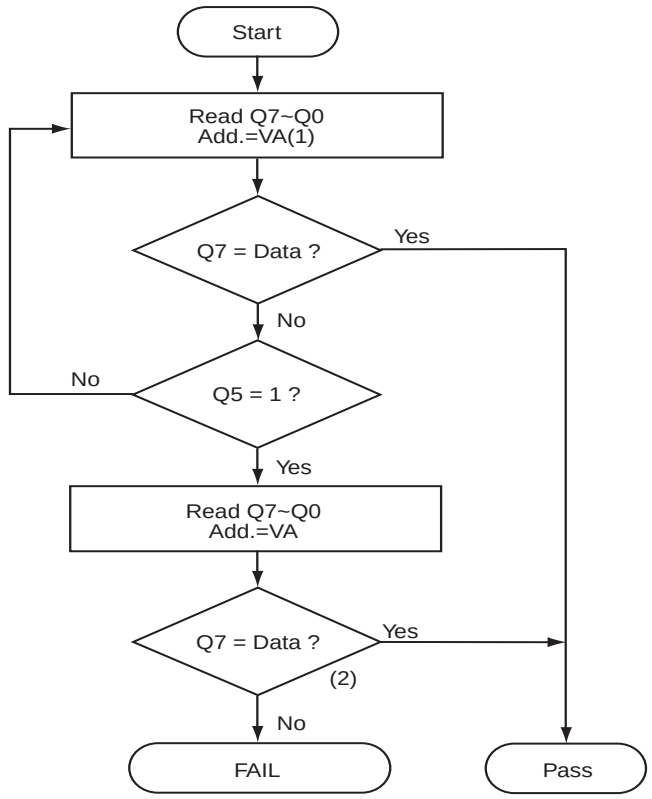
Figure 17. CHIP UNPROTECTION ALGORITHM (A9, $\overline{OE}$ Control)



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

WRITE OPERATION STATUS

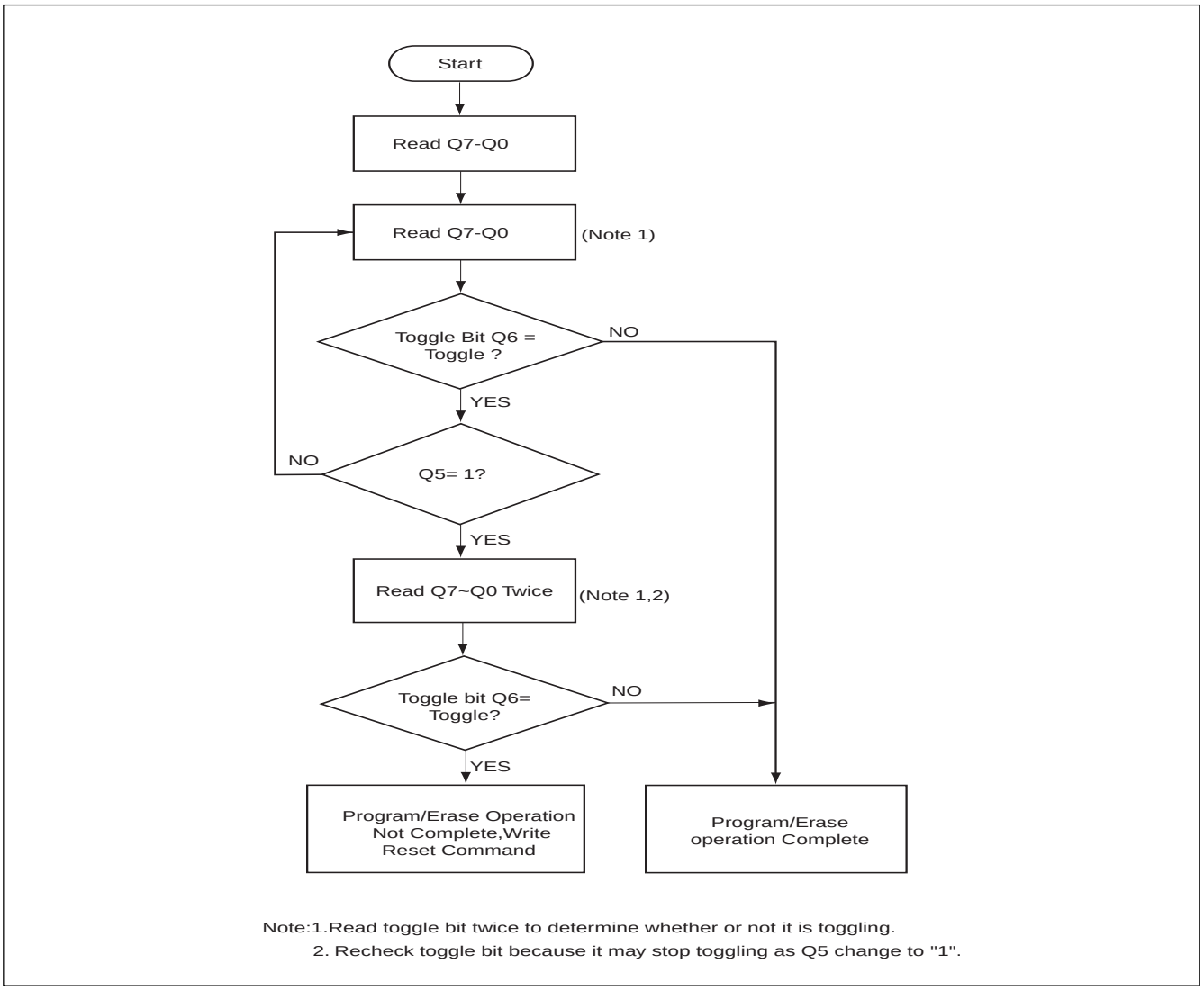
Figure 18. $\overline{\text{DATA}}$ POLLING ALGORITHM



NOTE : 1.VA=Valid address for programming

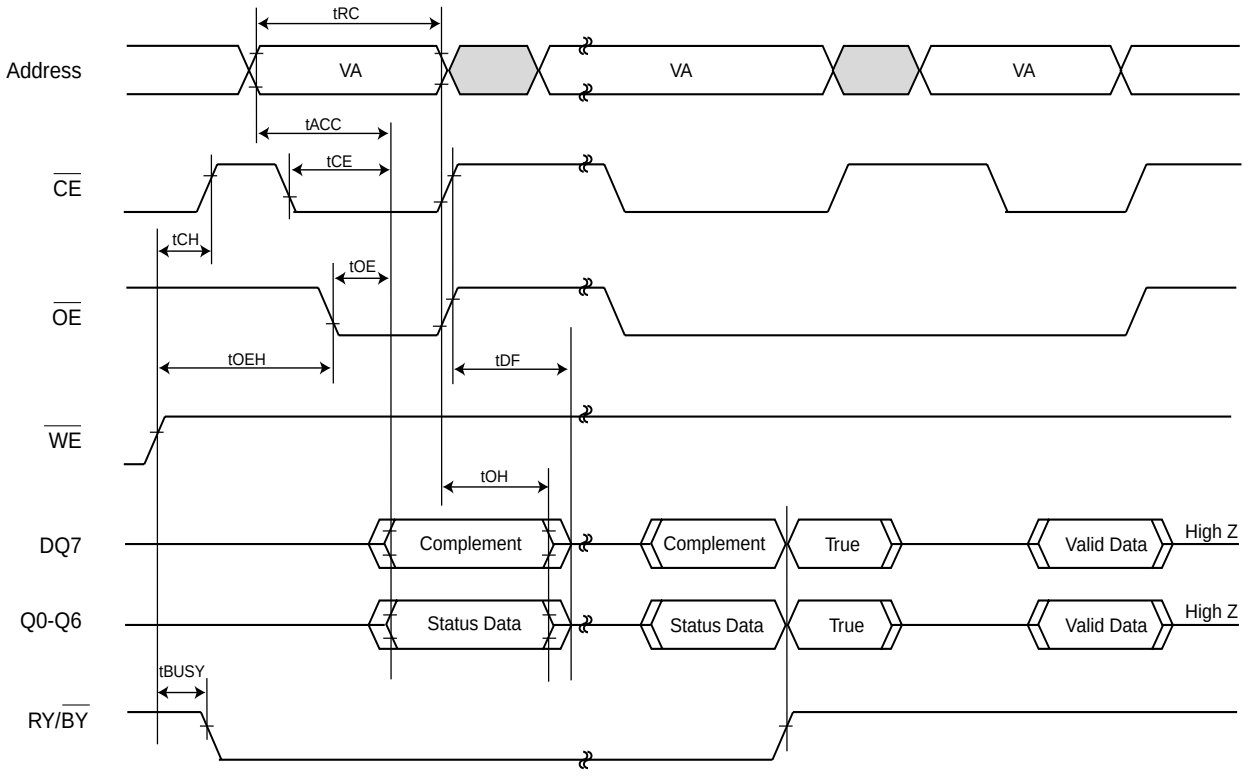
2.Q7 should be re-checked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 19. TOGGLE BIT ALOGRITHM



Note:1.Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 change to "1".

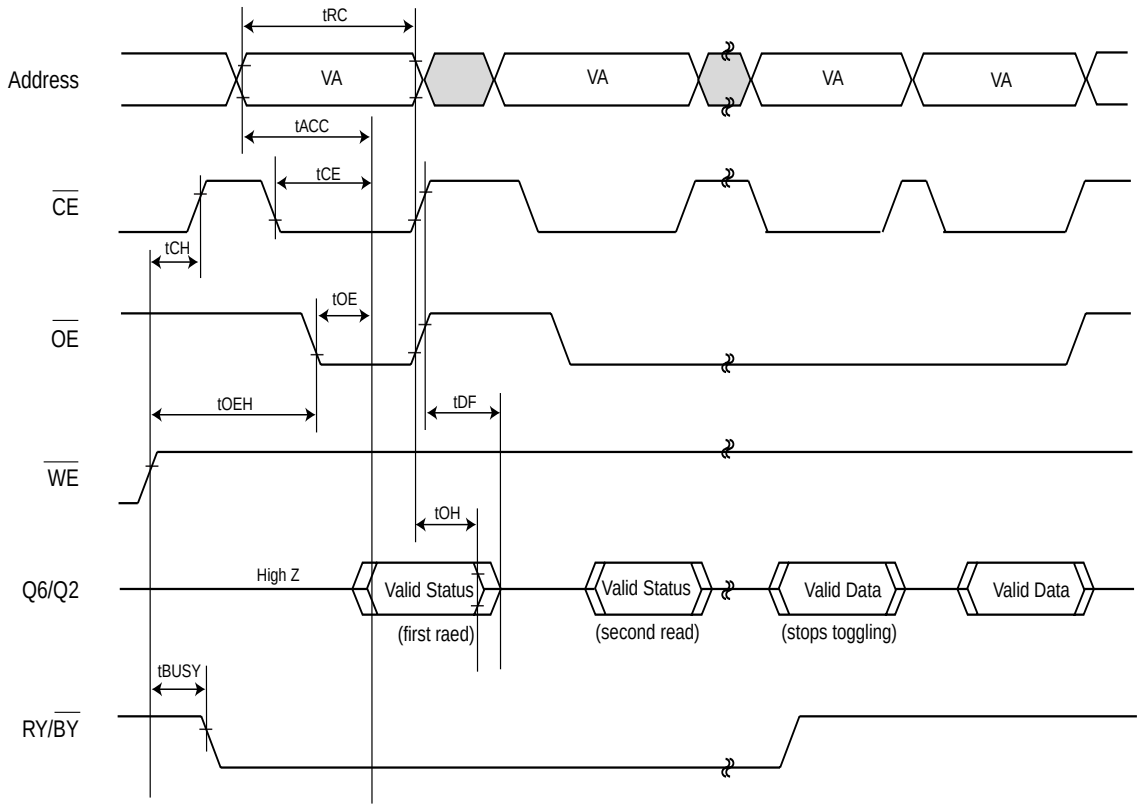
Figure 20. $\overline{\text{Data}}$ Polling Timings (During Automatic Algorithms)



NOTES:

VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 21. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALOGRITHMS)



NOTES:

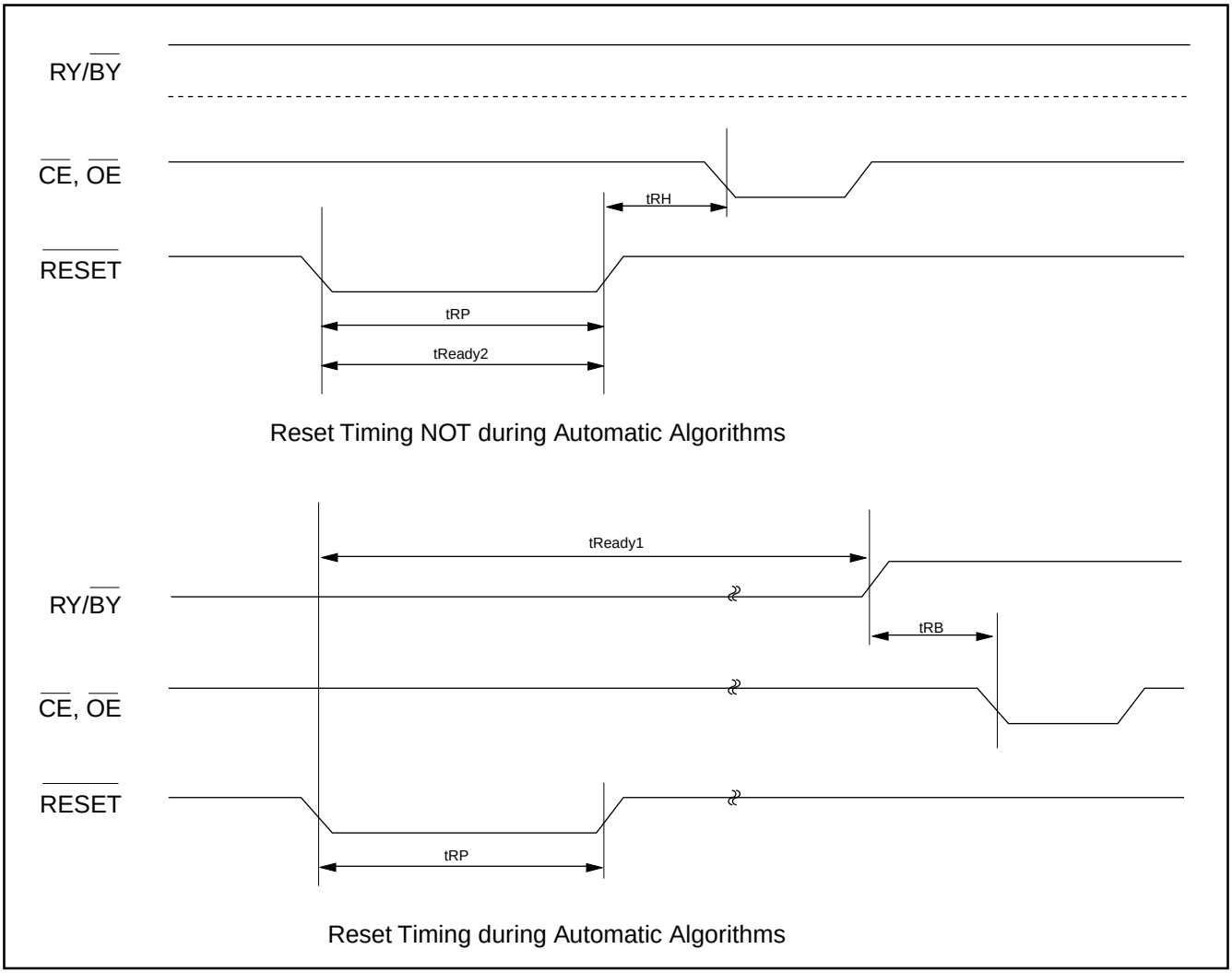
VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Table 12. AC CHARACTERISTICS

Parameter Std	Description	Test Setup	All Speed Options	Unit
tREADY1	$\overline{\text{RESET}}$ PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	$\overline{\text{RESET}}$ PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	$\overline{\text{RESET}}$ Pulse Width (During Automatic Algorithms)	MIN	500	ns
tRH	$\overline{\text{RESET}}$ High Time Before Read(See Note)	MIN	50	ns
tRB	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{CE}}$, $\overline{\text{OE}}$ go low)	MIN	0	ns

Note:Not 100% tested

Figure 22. $\overline{\text{RESET}}$ TIMING WAVFORM



AC CHARACTERISTICS

WORD/BYTE CONFIGURATION ($\overline{BYTE}$)

Parameter		Description		Speed Options		Unit
JEDEC	Std			-70 (R)	-90 (R)	
	tELFL/tELFH	$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	Max	5		ns
	tFLQZ	$\overline{BYTE}$ Switching Low to Output HIGH Z	Max	25	30	ns
	tFHQV	$\overline{BYTE}$ Switching High to Output Active	Min	70	90	ns

Figure 23. $\overline{BYTE}$ TIMING WAVEFORM FOR READ OPERATIONS ($\overline{BYTE}$ switching from byte mode to word mode)

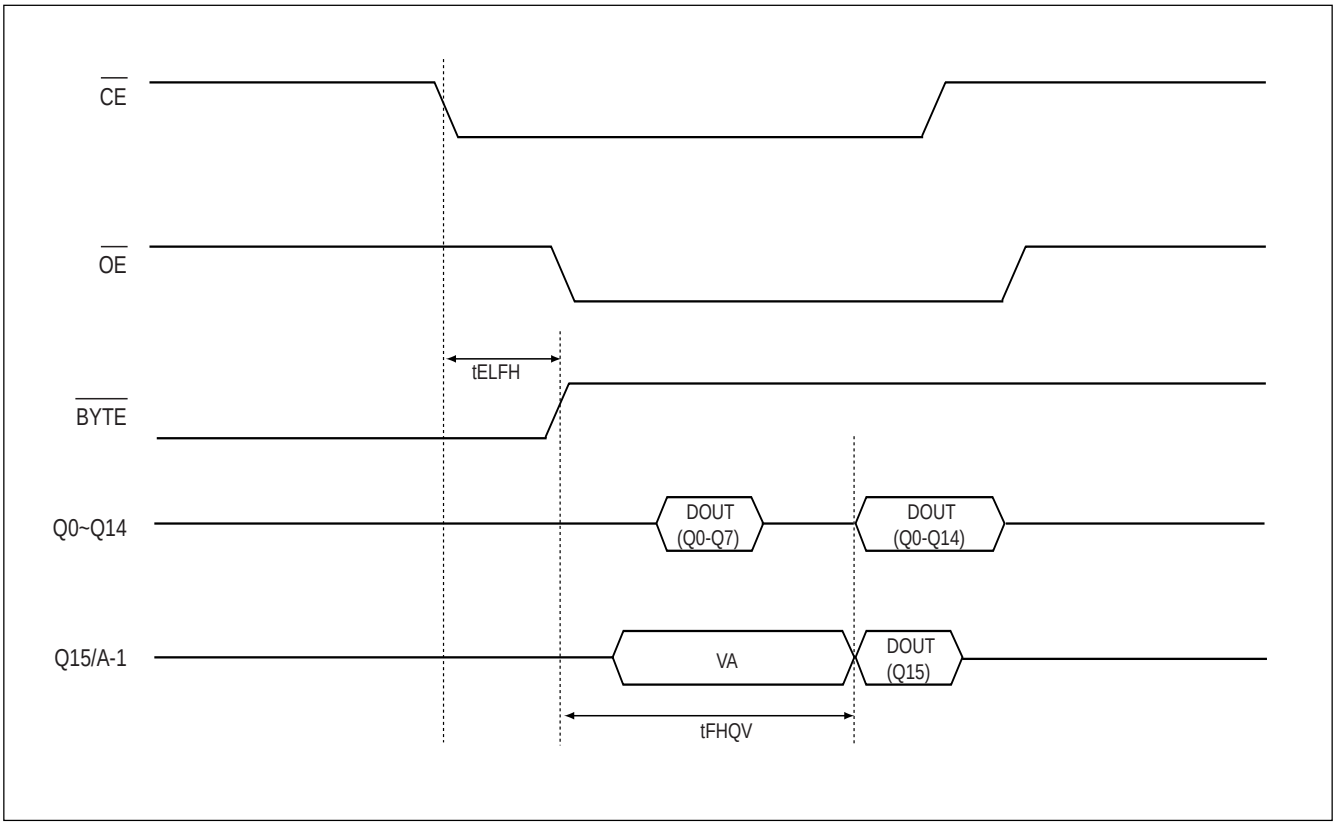


Figure 24. $\overline{\text{BYTE}}$ TIMING WAVEFORM FOR READ OPERATIONS ($\overline{\text{BYTE}}$ switching from word mode to byte mode)

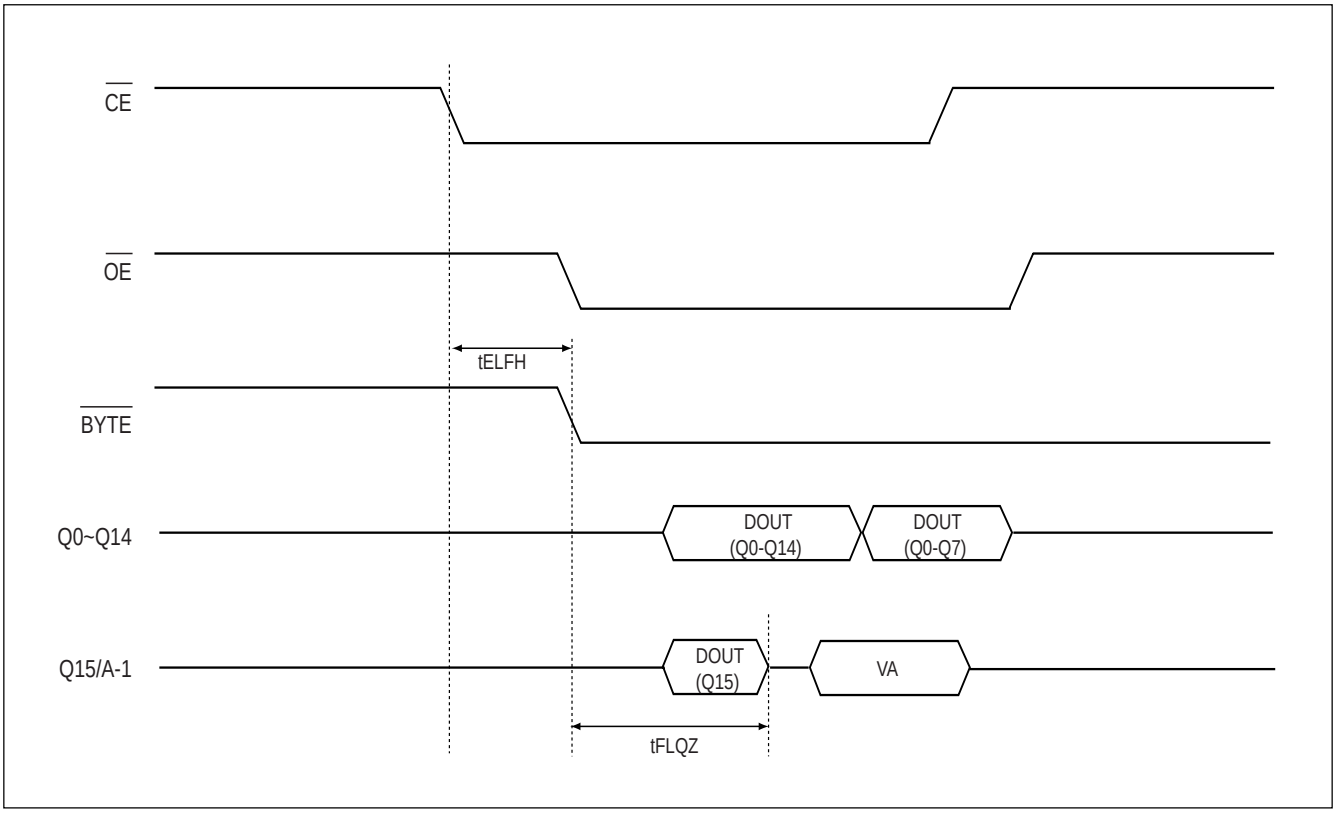


Figure 25. $\overline{\text{BYTE}}$ TIMING WAVEFORM FOR PROGRAM OPERATIONS

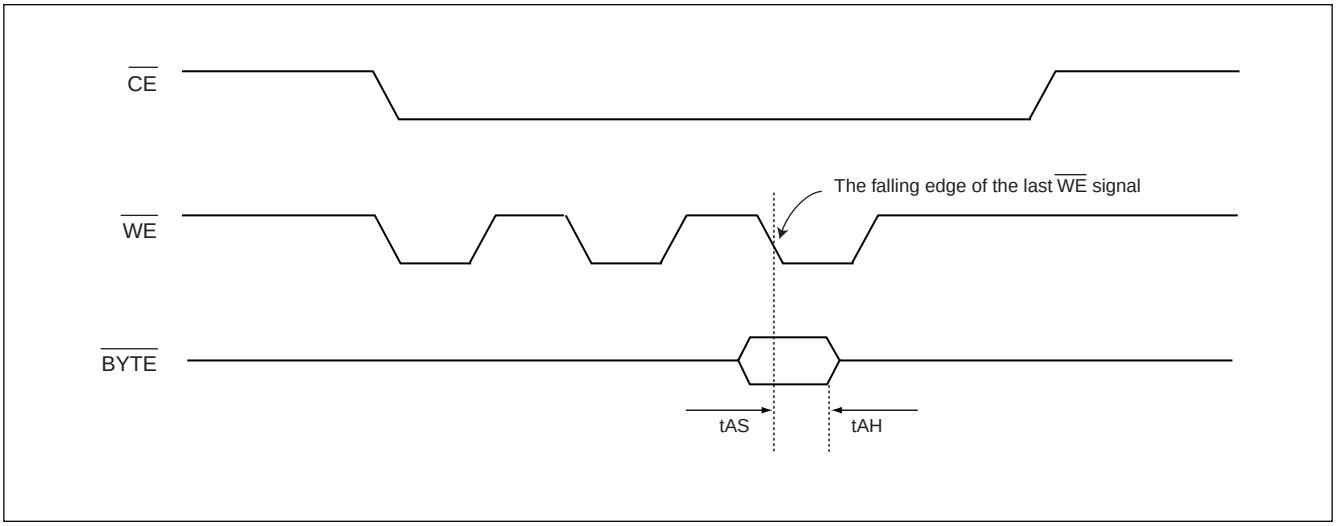


Table 13. TEMPORARY SECTOR UNPROTECT

Parameter Std.	Description	Test Setup	AllSpeed Options	Unit
tVIDR	VID Rise and Fall Time (See Note)	Min	500	ns
tRSP	$\overline{\text{RESET}}$ Setup Time for Temporary Sector Unprotect	Min	4	us

Note:
Not 100% tested

FIgure 26. TEMPORARY SECTOR UNPROTECT TIMING DIAGRAM

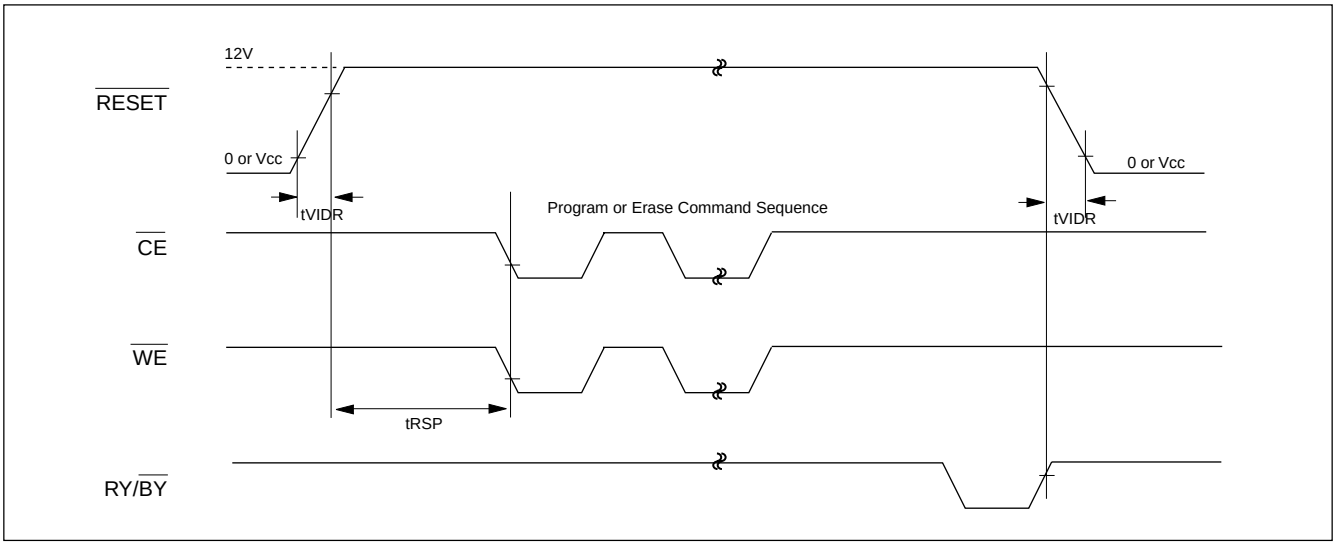
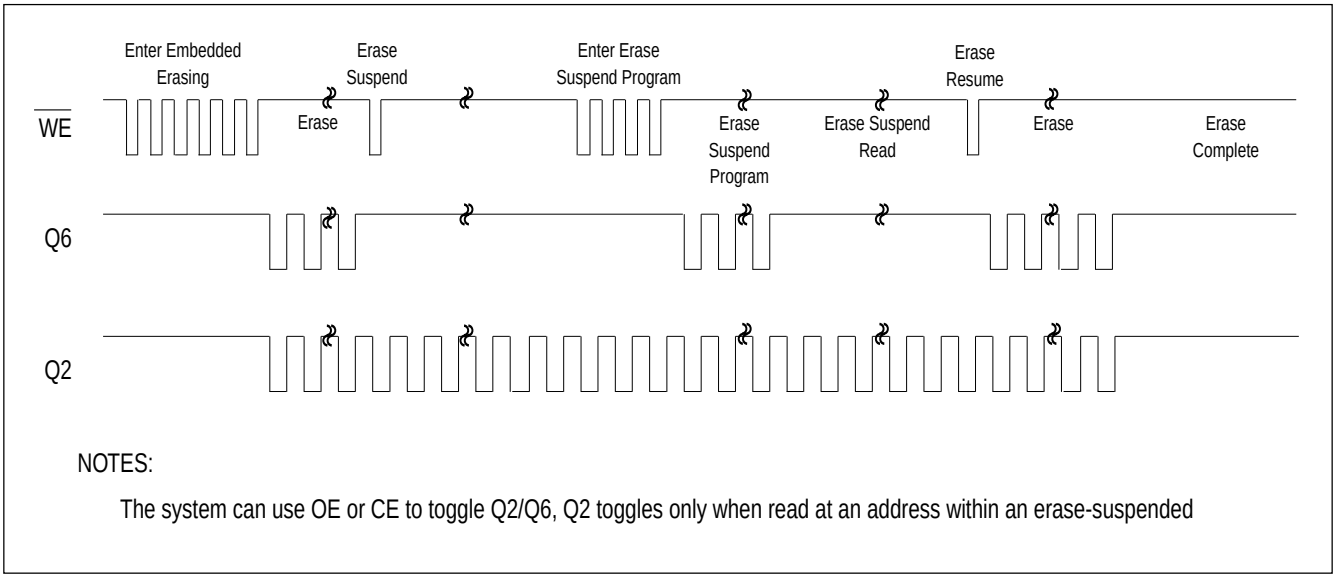


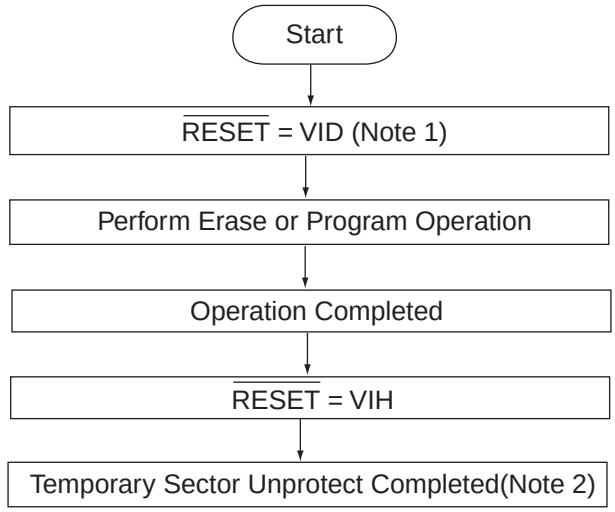
Figure 27. Q6 vs Q2 for Erase and Erase Suspend Operations



NOTES:

The system can use OE or CE to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

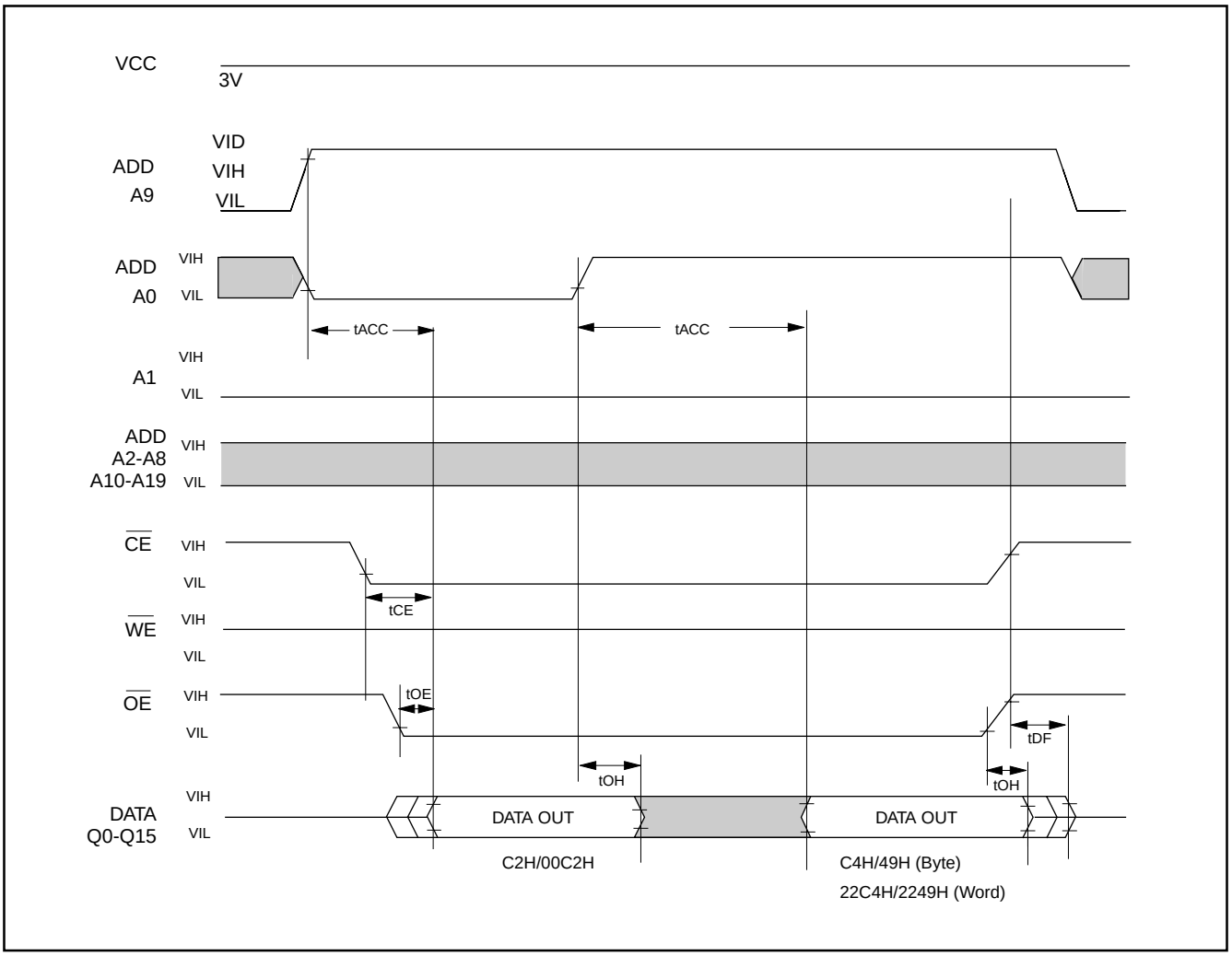
Figure 28. TEMPORARY SECTOR UNPROTECT ALGORITHM



Note : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

2. All previously protected sectors are protected again.

Figure 29. ID CODE READ TIMING WAVEFORM



ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER		LIMITS MIN.	LIMITS TYP.(2)	LIMITS MAX.(3)	UNITS
Sector Erase Time			0.7	15	sec
Chip Erase Time			25		sec
Byte Programming Time			9	300	us
Word Programming Time			11	360	us
Chip Programming Time	Byte Mode		18	54	sec
	Word Mode		12	36	sec
Erase/Program Cycles		100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25℃, 3V.
3.Maximum values measured at 25℃, 2.7V.

LATCHUP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	12.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 3.0V, one pin at a time.		

ORDERING INFORMATION

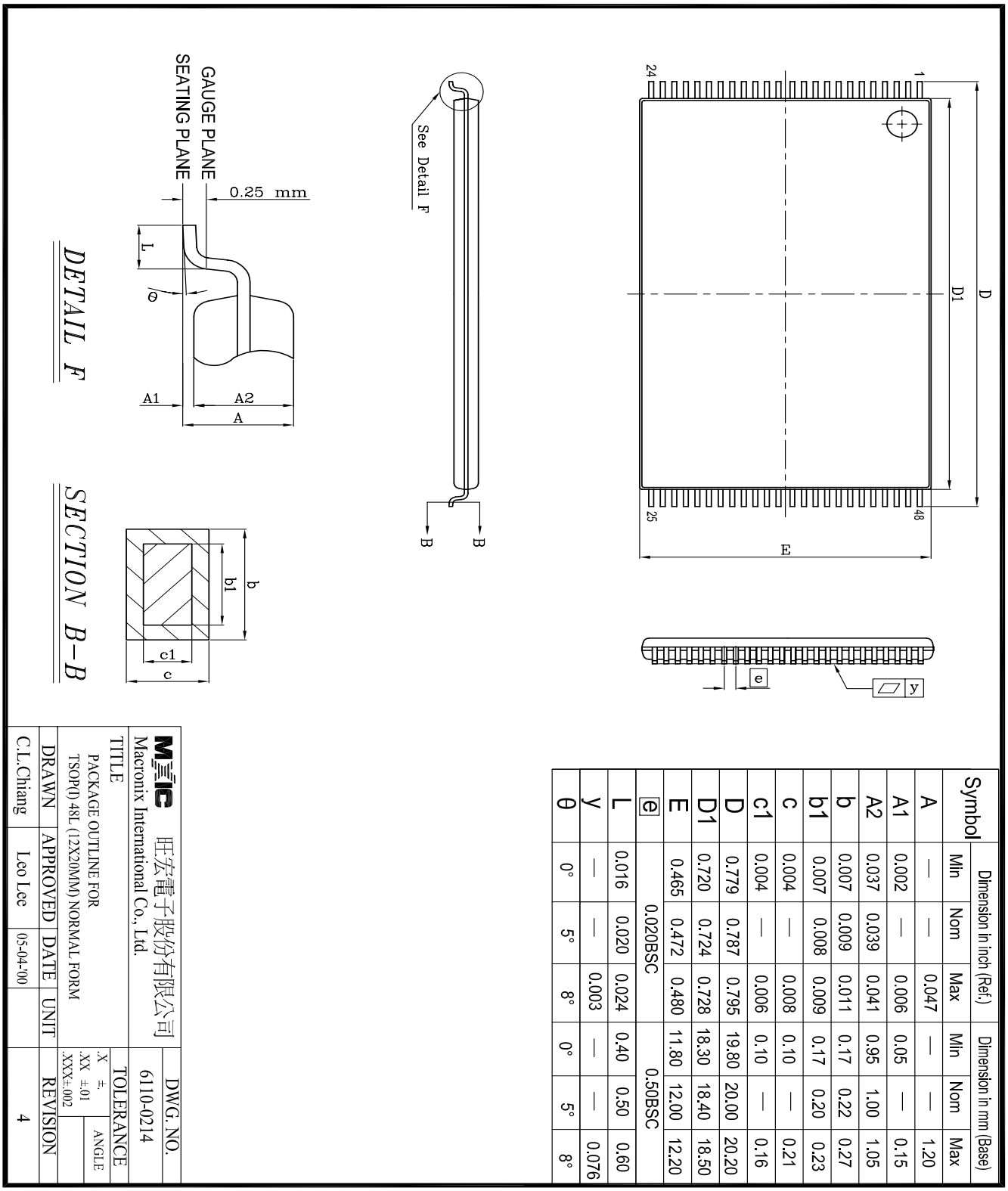
PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29LV161TMC-70	70	30	5	44 Pin SOP
MX29LV161BMC-70	70	30	5	44 Pin SOP
MX29LV161TMC-90	90	30	5	44 Pin SOP
MX29LV161BMC-90	90	30	5	44 Pin SOP
MX29LV161TTC-70	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTC-70	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTC-90	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTC-90	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTI-70	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTI-70	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTI-90	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTI-90	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTC-70R	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTC-70R	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTI-70R	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTI-70R	70	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTC-90R	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTC-90R	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161TTI-90R	90	30	5	48 Pin TSOP (Normal Type)
MX29LV161BTI-90R	90	30	5	48 Pin TSOP (Normal Type)

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29LV161TXBC-70	70	30	5	48 Ball CSP
MX29LV161BXBC-70	70	30	5	48 Ball CSP
MX29LV161TXBC-90	90	30	5	48 Ball CSP
MX29LV161BXBC-90	90	30	5	48 Ball CSP
MX29LV161TXBC-70R	70	30	5	48 Ball CSP
MX29LV161BXBC-70R	70	30	5	48 Ball CSP
MX29LV161TXBC-90R	90	30	5	48 Ball CSP
MX29LV161BXBC-90R	90	30	5	48 Ball CSP
MX29LV161TXBI-70	70	30	5	48 Ball CSP
MX29LV161BXBI-70	70	30	5	48 Ball CSP
MX29LV161TXBI-90	90	30	5	48 Ball CSP
MX29LV161BXBI-90	90	30	5	48 Ball CSP
MX29LV161TXBI-70R	70	30	5	48 Ball CSP
MX29LV161BXBI-70R	70	30	5	48 Ball CSP
MX29LV161TXBI-90R	90	30	5	48 Ball CSP
MX29LV161BXBI-90R	90	30	5	48 Ball CSP

PACKAGE INFORMATION

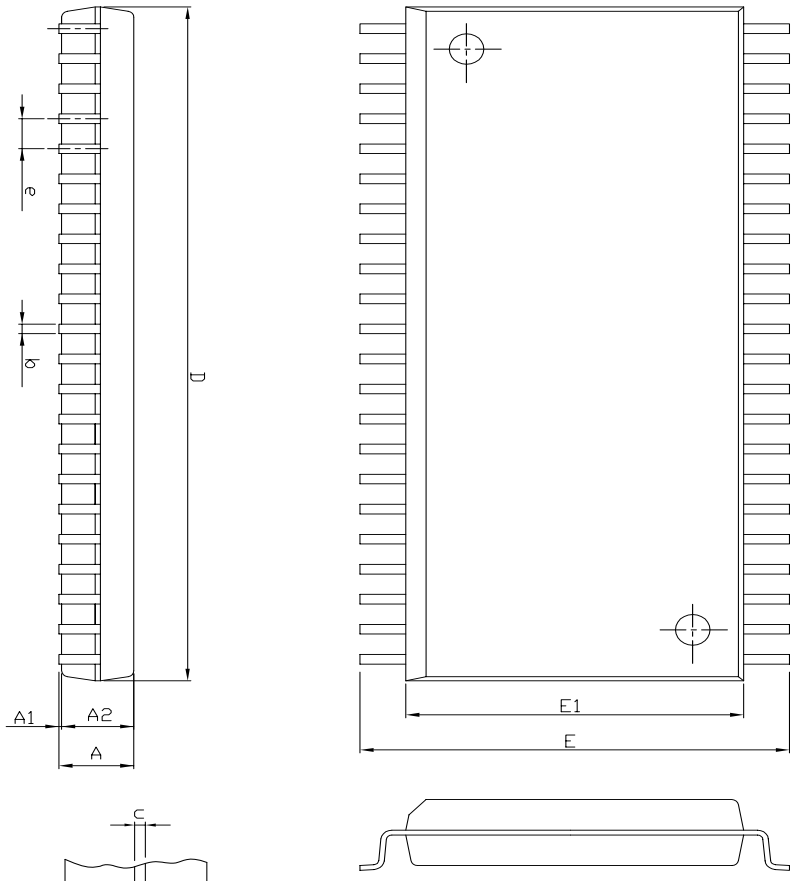
48-PIN PLASTIC TSOP



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
c	0.004	—	0.008	0.10	—	0.21
c1	0.004	—	0.006	0.10	—	0.16
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	0.465	0.472	0.480	11.80	12.00	12.20
e		0.020BSC			0.50BSC	
L	0.016	0.020	0.024	0.40	0.50	0.60
y	—	—	0.003	—	—	0.076
θ	0°	5°	8°	0°	5°	8°

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0214
TITLE PACKAGE OUTLINE FOR TSOP(I) 48L (12X20MM) NORMAL FORM			TOLERANCE .X ±. ANGLE .XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-04-'00	
			REVISION 4

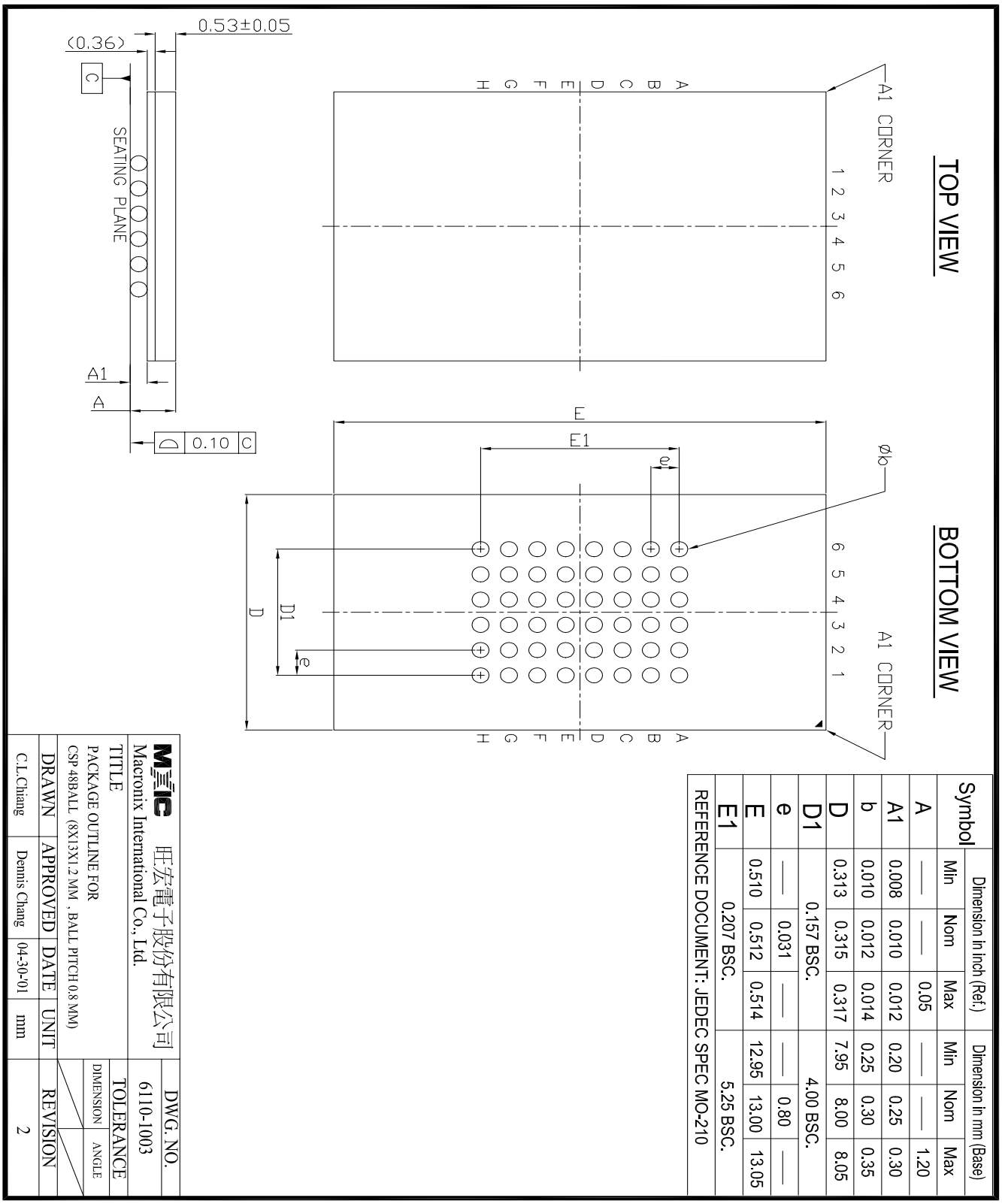
44-PIN PLASTIC SOP



Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b		0.41REF			0.016 REF	
c		0.20 REF			0.008 REF	
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e		1.27 REF			0.050 REF	
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—
JEDEC						

MXIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0207
TITLE			TOLERANCE
PACKAGE OUTLINE FOR SOP 44L (500 MIL)			.X ±. .XX ±.01 .XXX±.002 ANGLE ROUGHNESS
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-03-'01	INCH
			REVISION
			2

48 BALL CSP



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.05	——	——	1.20
A1	0.008	0.010	0.012	0.20	0.25	0.30
b	0.010	0.012	0.014	0.25	0.30	0.35
D	0.313	0.315	0.317	7.95	8.00	8.05
D1	0.157 BSC.			4.00 BSC.		
e	——	0.031	——	——	0.80	——
E	0.510	0.512	0.514	12.95	13.00	13.05
E1	0.207 BSC.			5.25 BSC.		

REFERENCE DOCUMENT: JEDEC SPEC MO-210

旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO.
			6110-1003
TITLE PACKAGE OUTLINE FOR CSP 48BALL (8X13X1.2 MM , BALL PITCH 0.8 MM)			TOLERANCE
			DIMENSION / ANGLE
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	04-30-'01	mm
			REVISION
			2

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