MX97103

ISDN S/T-PCI TRANSCEIVER

FEATURE

- Single chip solution for ISDN PC card with PCI interface
- Supports full duplex 2B+D ISDN S/T transceiver according to ITU I.430
- Integrate S-interface, D & B channel protocol controllers, and PCI controller
- 32-bit PCI bus interface
- Each B channel has 2x64 byte FIFO for each direction
- D channel has 2x32 byte FIFO for each direction
- EEPROM interface for loading vendor-specific data
- One programmable LED
- Comply to ACPI Rev 1.0
- 0.5u CMOS
- 100-pin PQFP package

GENERAL DESCRIPTION

MX97103 is a single chip solution for ISDN-S connection on PCI bus. It integrates S-transceiver, D and B channel protocol controllers, and PCI interface.

It can be divided into the following major functional blocks : analog front end, layer 1 function, GCI interface. LAPD controller, B channel HDLC controllers, EEPROM interface and PCI interface. The important function of each major block will be described below.

According to ITU 1.430 spec. the S/T interface is a 4-wire interface. Among them, 2 wires are used for transmitting, and the other two are for receiving. The wiring configurations include short passive bus, extended passive bus and point-to-point connection. For short passive bus, the operation distance is from 100m to 200m, and the TEs(max 8)can be connected at random points along the full length of the cable. For extended passive bus, TEs connect to the cable at the far end from the NT. The total length would be at least 500m and a differential distance between TE connection points is of 25 to 50m. For point-to-point connection, the cable length can be 1km.

The analog front end deals with the signals transmitted to and received from the wiring cable. It accepts the digital data from layer 1 block and converts them into appropriate signals to be sent out to the wire, and it also receive the attenuated and distorted signal from the wire and recover them to be processed by layer 1 block.

The layer 1 block comprises of PDLL, DAC, RT and MFC functions. DPLL's function is to establish S/T frame synchronization. DAC resolves the contention issue for differnet TE accessing D channel at the same time. RT deals with the receiving S/T data extraction and put out the transmitted data at the corrent time slot. MFC is the multiframing S and Q channel control block.

GCI is the digital bus for the IC. It can accomodate 8 GCI-compatible devices. This block converts the frame between GCI and S/T interface.

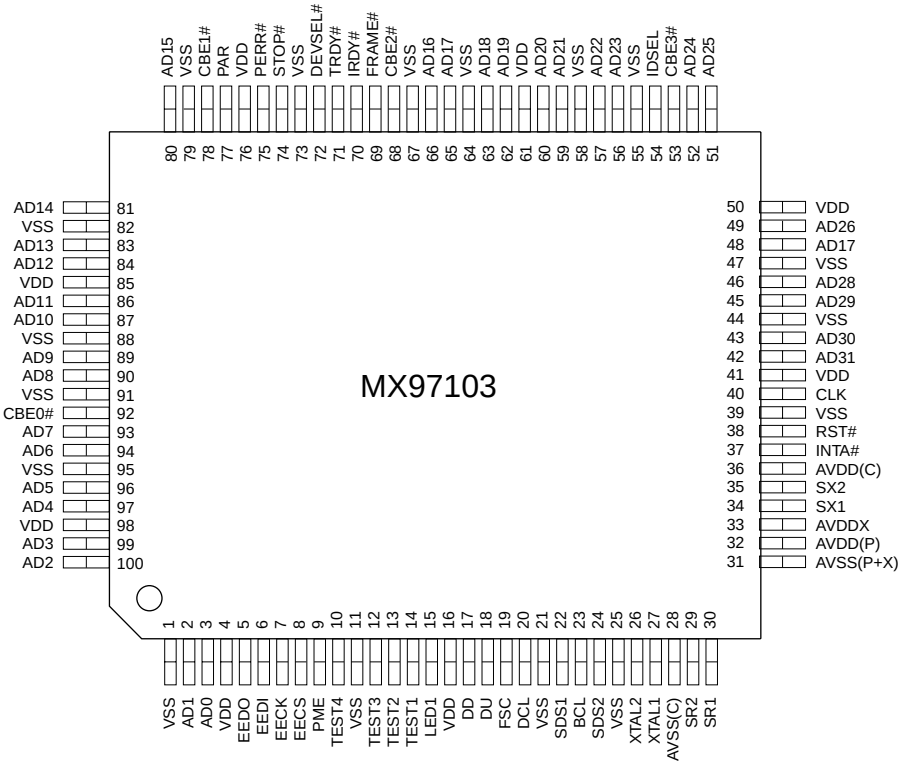
LAPD block relieves the microprocessor of the duty to generate HDLC frame on the D channel. It can generate flag, CRC, address and control field automatically. And it can generate S-frame for HDLC protocol. It contains 2 FIFO of 2x32 byte each to facilitate the D packet transmission and reception.

Two B channel HDLC controllers can handle tasks like flag and CRC generation, zero insertion and deletion. For each direction a 2x64 byte FIFO is provided to buffer the data.

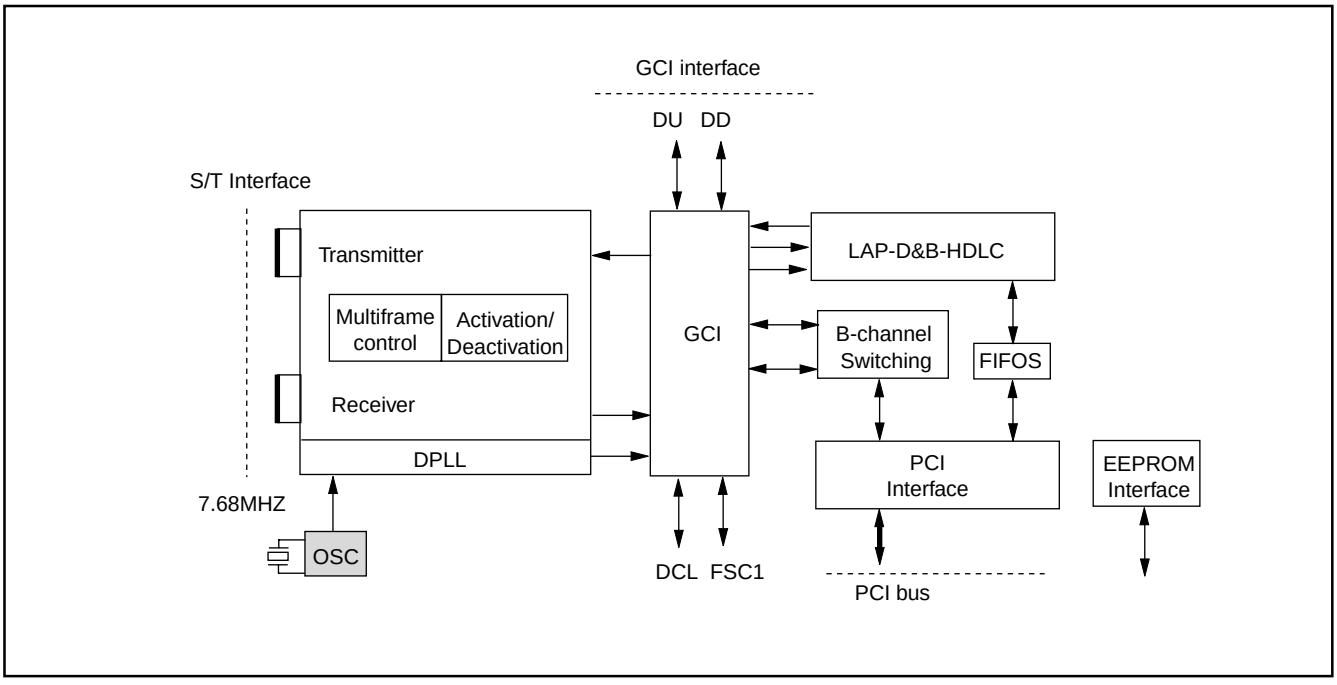
The EEPROM interface is used to load specific vendor information after system hardware reset. Vendor ID and device ID can be load to distinguish different products. If EEPROM is not used, default values will be set.

The PCI interface enables the chip attached to PCI bus directly without any glue logic. The bus speed can be from 25MHz to 33MHz.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

PAD#	PIN NAME	TYPE	DESCRIPTION
42, 43, 45, 46, 48, 49, 51, 52, 56, 57, 59, 60, 62, 63, 65, 66, 80, 81, 83, 84, 86, 87, 89, 90, 93, 94, 96, 97, 99, 100, 2, 3	AD[31:0]	I/O	PCI address/data bus.
53, 68, 78, 92	CBE[3:0]#	I	PCI command/byte enable, command during address phase, byte enable during data phase.
69	FRAME#	I	PCI FRAME# signal, asserted to indicate the start of a bus transaction.
71	TRDY#	O	PCI Target ready, asserted by target agent.
70	IRDY#	I	PCI master ready, data transferred on the rising edge of CLK when IRDY# and TRDY# both asserted.
72	DEVSEL#	O	PCI slave device select, specific for configuration cycle.
54	IDSEL	I	PCI Initialization device select, specific for configuration cycle.
40	CLK	I	PCI clock, 33MHz
38	RST#	I	PCI bus reset
37	INTA#	O/D	PCI bus interrupt request
75	PERR#	I/O	PCI bus data error
77	PAR	I/O	PCI bus parity bit, even parity for AD and CBE
74	STOP#	O	PCI stop signal
23	BCL	O	GCI bit clock, 768KHz
22	SDS1	O	GCI serial data strobe 1, programmable strobe signal
24	SDS2	O	GCI serial data strobe 2, programmable strobe signal
19	FSC	O(I)	GCI frame sync
20	DCL	O(I)	GCI data clock, 1.536MHz
18	DU	I/O	GCI data upward to ST interface
17	DD	I/O	GCI data downward from ST interface
34	SX1	O	S-bus transmitter output(positive)
35	SX2	O	S-bus transmitter output(negative)
29	SR2	I	S-bus receiver input
30	SR1	I	S-bus receiver reference
27	XTAL1	I	Connection for 7.68MHz crystal/oscillator input
26	XTAL2	O	Crystal output
9	LED2	O	Auxillisry LED output 0
15	LED1	O	Auxilliary LED output 1

PAD#	PIN NAME	TYPE	DESCRIPTION
8	EECS	O	EEPROM chip select
7	EECK	O	EEPROM interface clock
6	EEDI	O	Output data to EEPROM
5	EEDO	I	Input data from EEPROM
10, 12, 13, 14	TEST[4:1]		test pins
36, 33, 32	AVDD		Analog power
31, 28	AVSS		Analog ground
4, 16, 41, 50, 61, 76, 85, 98	VDD		Digital power
1, 11, 21, 25, 39, 44, 47, 55, 58, 64, 67, 73, 79, 82, 88, 91, 95	VSS		Digital ground

ABSOLUTE MAXIMUM RATINGS

Supply Voltage(VDD)	4.75V to 5.25V
DC Input Voltage(Vin)	-0.5V to VDD+0.5V
DC Output Voltage(Vout)	-0.5V to VDD+0.5V
Storage Temperature Range(Tstg)	-55℃ to 150℃
Power Dissipation(PD)	500mW
Lead Temp.(TL)(Soldering, 10sec)	260℃
ESD Rating(Rzap=1.5k, Czap=100pf)	2000V
Clamp Diode Current	±20mA

DC CHARACTERISTICS

PCI BUS D.C SPECS

PCI System signals
CLK, RST#
PCI Shared signals
AD[31:0](t/s), CBE[3:0]#(t/s), FRAME#(s/t/s), TRDY#(s/t/s), IDSEL(in), IRDY#(s/t/s), STOP#(s/t/s), DEVSEL#(s/t/s), PAR(t/s), PERR#(s/t/s), INTA#(o/d), SERR#(s/t/s)

Temperature from 0 to 70℃; VDD=5V±5%, VSS=0V, AVSS=0V

SYMBOL	PARAMETER	CONDITIONS	MIN. VALUE	MAX. VALUE	NOTES
VIL	L-input voltage			0.8V	
VIH	H-input voltage		2.0V	5.4V	
VOL	L-output voltage	IOL1=3mA IOL2=6mA		0.45V	1
VOH	H-output voltage	IOH=-2mA	2.4V		
IIL	L-input current	VIN=0.5V		-70uA	
IIH	H-input current	VIN=2.7V		70uA	
CI/O	Input/output capacitance	at 1MHz		10pF	
CCLK	CLK input capacitance	at 1MHz		17pF	
CL	Load capacitance			50pF	

NOTE:
1. IOL2 applies to signals with external pull-ups: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#

GCI BUS & EEPROM INTERFACE D.C. SPECS

GCI signals:
BCL, DCL, DD, DU, FSC.SDS1, SDS2
EEPROM signals:
EECS, EECK, EEDI, EEDO

SYMBOL	PARAMETER	CONDITIONS	MIN. VALUE	MAX. VALUE	NOTES
VIL	L-input voltage			0.8V	
VIH	H-input voltage		2.0V	5.4V	
VOL	L-output voltage	IOL1=2mA IOL2=7mA		0.45V	1
VOH	H-output voltage	IOH=-400uA	2.4V		

NOTE:
1. IOL2 is for DD only.

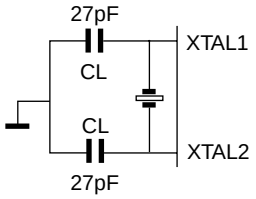
S-BUS D.C. SPECS

SX1, SX2, SR1, SR2

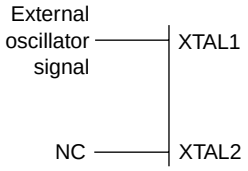
SYMBOL	PARAMETER	CONDITIONS	MIN. VALUE	MAX. VALUE	NOTES
VX	Absolute value of output pulse amplitude (VSX2-VSX1)	RL=50 ohm RL=400 ohm	2.03V 2.10V	2.31V 2.39V	SX1, SX2
IX	Transmitter output current	RL=5.6 ohm	7.5mA	13.4mA	
RX	Transmitter output impedance	(1) Inactive or during binary 1, (2) during binary 0 RL=50 ohm	(1)10K ohm (2) 0 ohm		
VSR1	Receive output voltage	IO<5uA	2.35V	2.6V	SR1, SR2
VTR	Receiver threshold voltage (VSR2-VSR1)	Dependent on peak level	225mV	375mV	SR1, SR2

NOTE:
1. Due to the transformer, the load resistance seen by the circuit is four times RL.

CRYSTAL SPEC



Crystal mode



Driving from external source

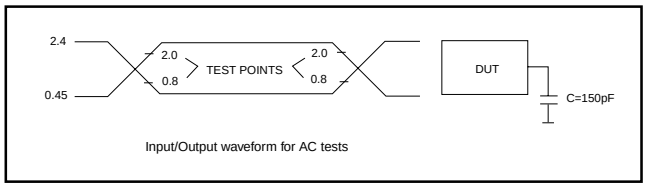
PARAMETER	SYMBOL	LIMIT VALUES	UNIT
Frequency	*f*	7.680	MHz
Frequency calibration tolerance		max. 100	ppm
Load capacitance	CL	max. 35	pF
Oscillator mode		fundamental	

XTAL1 CLOCK CHARACTERISTICS

PARAMETER	LIMIT VALUES	
	MIN.	MAX.
Duty cycle	1:2	2:1

AC CHARACTERISTICS

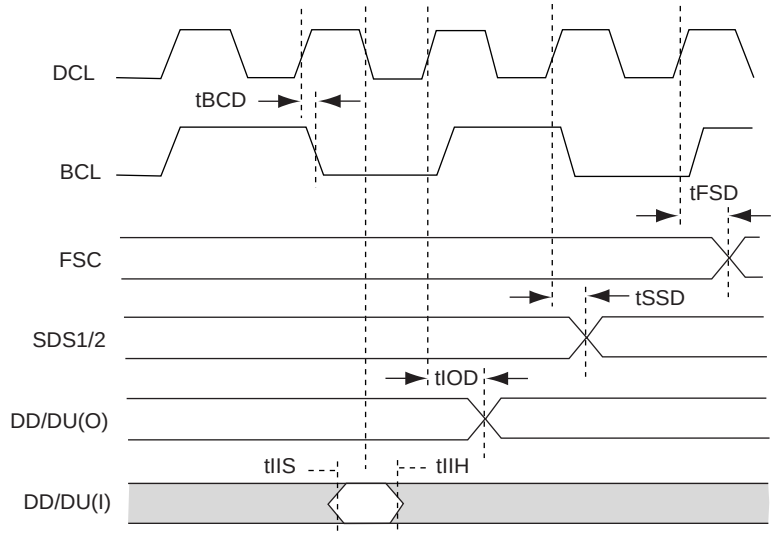
Temperature from 0 to 70℃, VDD=5V±5%
Inputs are driven to 2.4V for a logical "1" and to 0.4V for a logical "0". Timing meansurements are made at 2.0V for a logical "1" and 0.8v for a logical "0". The AC-testing output is loaded with a 150pF capacitor.



Input/Output waveform for AC tests

TIMING WAVEFORM

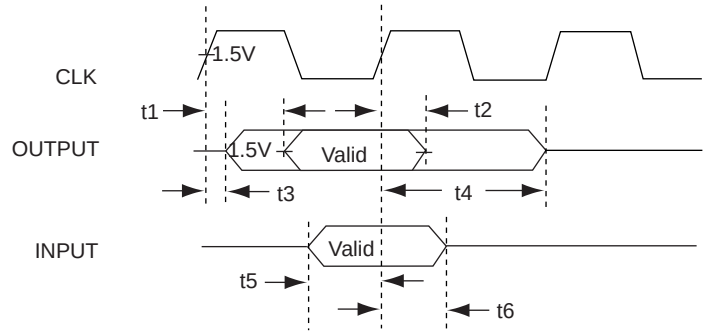
SERIAL INTERFACE TIMING



GCI TIMING

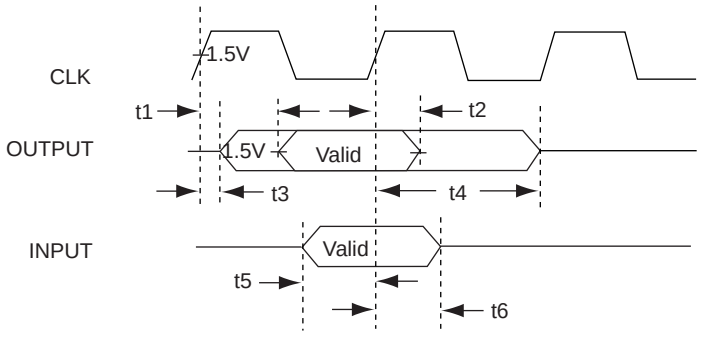
PARAMETER	SYMBOL	MIN.	MAX.
GCI output data delay	tIOD	20ns	100ns
GCI input data setup	tIIS	20ns	
GCI input data hold	tIIH	20ns	
FSC strobe delay	tFSD	-20ns	20ns
SDS strobe delay	tSDD		120ns
Bit clock delay	tBCD	-20ns	20ns

PCI SHARED SIGNALS A.C. TIMING WAVEFORM



PARAMETER	SYMBOL	MIN.	MAX.	NOTES
CLK signal valid delay	t1		11ns	CL=50pF
CLK to signal invalid delay	t2	2ns		
Hi-Z to active delay from CLK	t3	2ns		
Active to Hi-Z delay from CLK	t4		28ns	
Input signal valid setup time before CLK	t5	7ns		
Input signal hold time from CLK	t6	0ns		

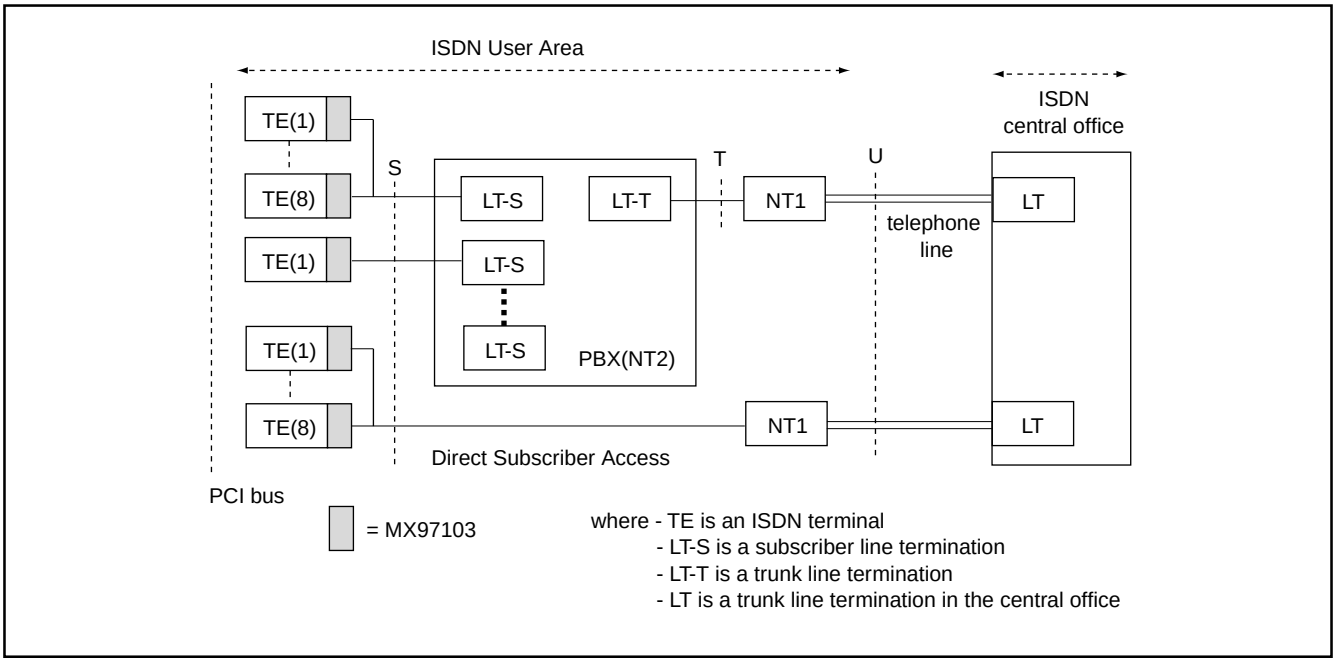
PCI SIDEBAND SIGNALS A.C. TIMING WAVEFORM



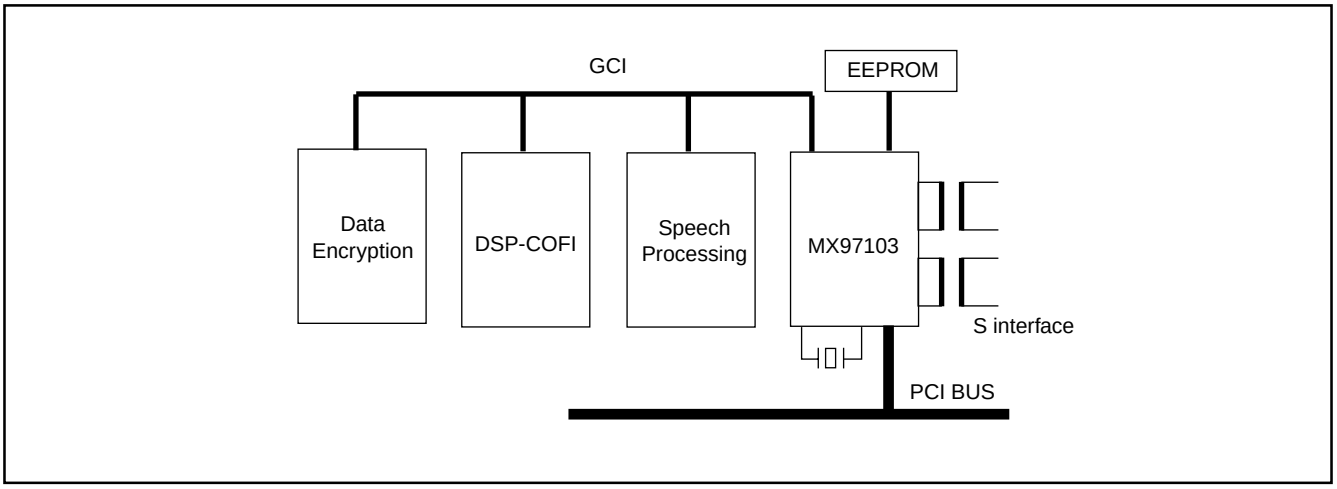
PARAMETER	SYMBOL	MIN.	MAX.	NOTES
CLK to sideband signal valid delay	t1		12ns	CL=50pF
CLK to signal invalid delay	t2	2ns		
Hi-Z to active delay from CLK	t3	2ns		
Active to Hi-Z delay from CLK	t4		28ns	
Sideband signal valid setup time before CLK	t5	12ns		
Input signal hold time from CLK	t6	0ns		

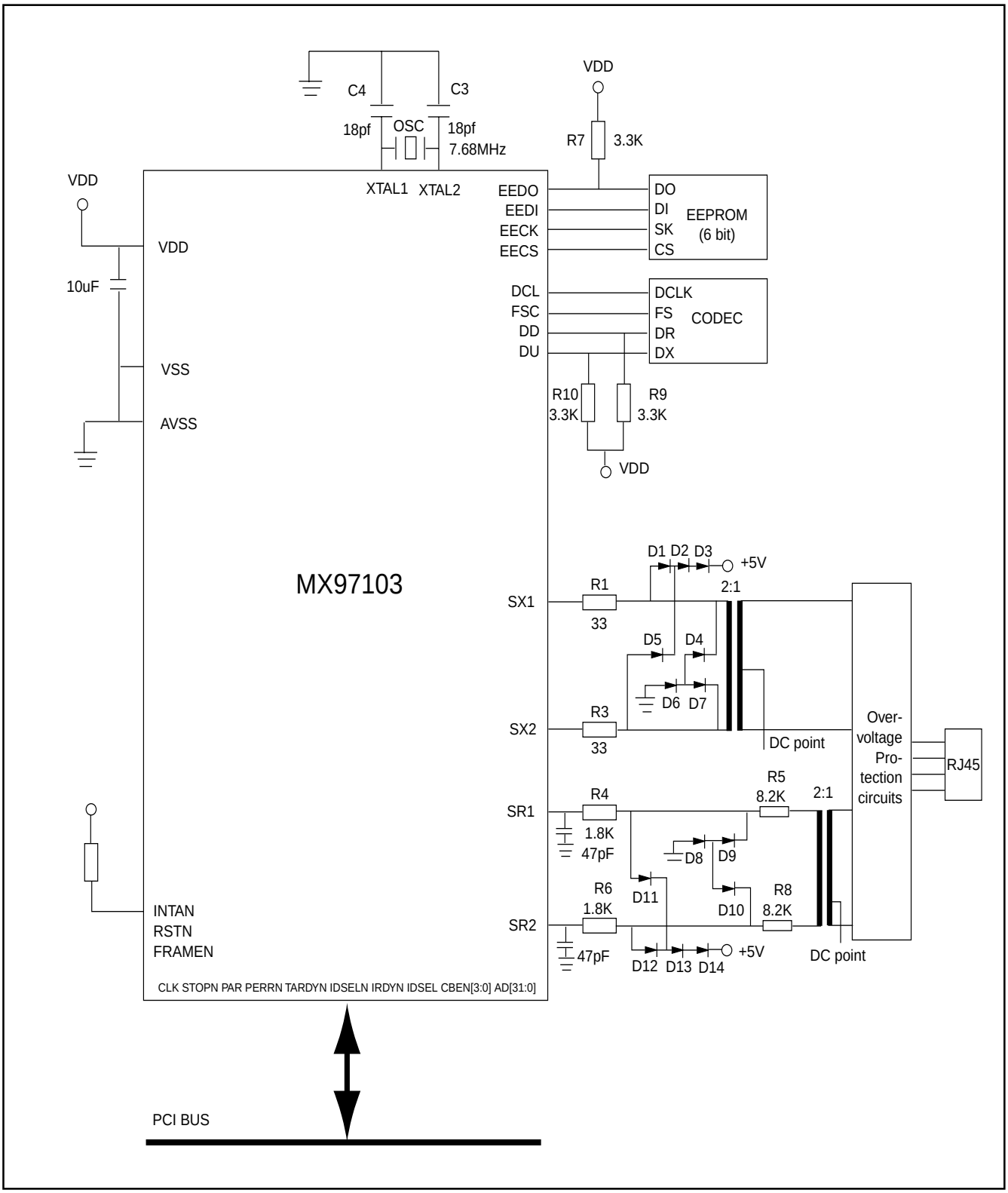
APPLICATION

ISDN ACCESS ARCHITECTURE



GCI CONNECTION




C4
C3
18pf
OSC
18pf
7.68MHz
XTAL1
XTAL2
VDD
R7
3.3K
VDD
10uF
VDD
VSS
AVSS
EEDO
EEDI
EECK
EECS
DO
DI
SK
CS
EEPROM
(6 bit)
DCL
FSC
DD
DU
DCLK
FS
DR
DX
CODEC
R10
3.3K
R9
3.3K
VDD
MX97103
D1 D2 D3
+5V
SX1
R1
33
2:1
D5
D4
D6 D7
SX2
R3
33
DC point
Over-
voltage
Pro-
tection
circuits
RJ45
R5
8.2K
2:1
SR1
R4
1.8K
47pF
D8
D9
R6
1.8K
D11
D10
R8
8.2K
SR2
47pF
D12 D13 D14
+5V
DC point
INTAN
RSTN
FRAMEN
CLK STOPN PAR PERRN TARDYN IDSELN IRDYN IDSEL CBEN[3:0] AD[31:0]
PCI BUS

TEST CIRCUIT

To test digital function separately, DTMC[TMODE] can be set to enable the stimulus inputs from test1~4 pins.

PIN	DTMC	SP2	SP1	SP0	I/O	SIGNAL	DESCRIPTION
TEST1	1	X	X	X	I	XRAMI1	test RAMI1 input signal
TEST2	1	X	X	X	I	XRAMI2	test RAMI2 input signal
TEST3	1	X	X	X	I	XZC	test ZC input signal
TEST4	1	X	X	X	I	XI0N	test I0N input signal
TEST1	0	0	0	0	O	ARAMI1	RAMI1 from analog module
TEST2	0	0	0	0	O	ARAMI2	RAMI2 from analog module
TEST3	0	0	0	0	O	AZC	ZC from analog module
TEST4	0	0	0	0	O	SAMP	SAMP from analog module
TEST1	0	0	0	1	O	S[0]	activation/deactivation state code
TEST2	0	0	0	1	O	S[1]	
TEST3	0	0	0	1	O	S[2]	
TEST4	0	0	0	1	O	S[3]	
TEST1	0	0	1	0	O	MBAS1	TIC bus arbitration state code
TEST2	0	0	1	0	O	MBAS2	
TEST3	0	0	1	0	O	CLS	D channel collision
TEST4	0	0	1	0	O	AI0N	I0N from analog module
TEST1	0	0	1	1	O	RFN	layer sync.

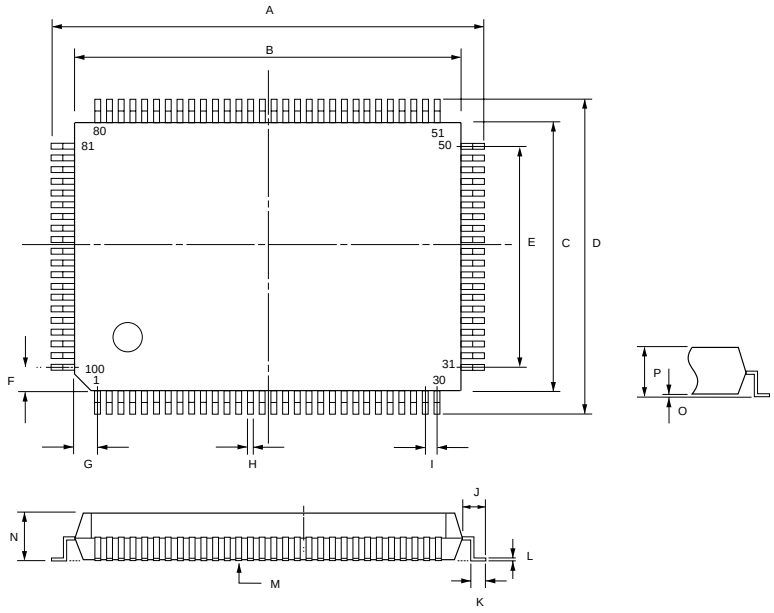
For normal operation, DTMC should be set to 0. Test1~4 pins can be programmed to output internal signals for monitoring purpose.

PACKAGE INFORMATION

100-PIN PLASTIC QUAD FLAT PACKAGE (PQFP)

ITEM	MILLIMETERS	INCHES
A	24.80±.40	.967±.016
B	20.00±.13	.787±.005
C	14.00±.13	.551±.005
D	18.80±.40	.740±.016
E	12.35 [REF]	.486 [REF]
F	.83 [REF]	.033 [REF]
G	.58 [REF]	.023 [REF]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	2.40 [Typ.]	.094 [Typ.]
K	1.20 [Typ.]	.047 [Typ.]
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	2.75±.15	.018±.006
O	.10 min.	.004 min.
P	3.30 max.	.103 max.

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



ORDERING INFORMATION

PART NO.	PACKAGE
MX97103FC	100-PIN PQFP

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com