MX98L715BEC

3.3V SINGLE CHIP FAST ETHERNET NIC CONTROLLER

1. FEATURES10/100M

Ethernet Interface

- A single chip solution integrates 100/10 Base-T fast Ethernet MAC, PHY and PMD
- Fully comply to IEEE 802.3u specification
- Operates over 100 meters of STP and cat 5 UTP cable
- Support full and half duplex operations in both 100 Base-TX and 10 Base-T mode
- Supports IEEE802.3x Frame Based Flow Control scheme in full duplex mode.
- Supports transmission and reception of IEEE802.1Q tagged frames.
- Supports QoS with prioritized traffic.
- Supports network and communication device class OnNow requirements for Microsoft's PC99 specifications, including 3 wake up events :
  - Link Change (link-on)
  - Wake Up Frames
  - Magic Packet
- 100/10 Base-T NWAY auto-negotiation function
- Support up to 5 LEDs for various network activities
- Supports early interrupt on both transmit and receive operations.
- Support a variety of flexible address filtering modes with 16 CAM address and 64 bits hash table

Home PNA interface

- Support 7-wire general purpose serial interface to link with 1M8 PHY for home networking

PCI/MiniPCI interface

- Fully comply to PCI spec. 2.2 and Mini PCI spec. 0.73 up to 33MHz
- Fully comply to Advanced Configuration and Power Interface (ACPI) Rev 1.1
- Fully comply to PCI Bus Power Management Interface spec. Rev 1.1
- Bus master architecture with linked host buffers delivers the most optimized performance
- 32-bit bus master DMA channel provides ultra low CPU utilization suitable for server and windows applications.
- Proprietary Adaptive Network Throughput Control (ANTC) technology to optimize data integrity and throughput

Other features

- Large on-chip FIFOs for both transmit and receive operations without external local memory
- Support up to 128K bytes boot ROM/Flash interface
- MicroWire interface to EEPROM for customer's IDs and configuration data
- Single 3.3V power supply, CMOS technology, 128-pin PQFP package

(Magic Packet Technology is a trademark of Advanced Micro Device Corp.)

2. GENERAL DESCRIPTIONS

The MX98L715BEC controller is an IEEE802.3u compliant single chip 32-bit full duplex, 10/100Mbps highly integrated Fast Ethernet combo solution, designed to address high performance local area networking (LAN) system application requirements.

MX98L715BEC's PCI bus master architecture delivers the optimized performance for future high speed and powerful processor technologies. In other words, the MX98L715BEC not only keeps CPU utilization low while maximizing data throughput, but it also optimizes the PCI bandwidth providing the highest PCI bandwidth utilization. To further reduce maintenance costs the MX98L715BEC uses drivers that are backward compatible with the original MXIC MX98715 series controllers.

The MX98L715BEC contains a PCI local bus glueless interface, a Direct Memory Access (DMA) buffer management unit, an IEEE802.3u-compliant Media Access Controller (MAC), large Transmit and Receive FIFOs, and an on-chip 10 Base-T and 100 Base-TX transceiver simplifying system design and improving high speed signal quality. Full-duplex operation are supported in both 10 Base-T and 100 Base-TX modes that increases the controller's operating bandwidth up to 200Mbps. Equipped with intelligent IEEE802.3u-compliant auto-negotiation, the MX98L715BEC-based adapter allows a single RJ-45 connector to link with the other IEEE802.3u-compliant device without re-configuration.
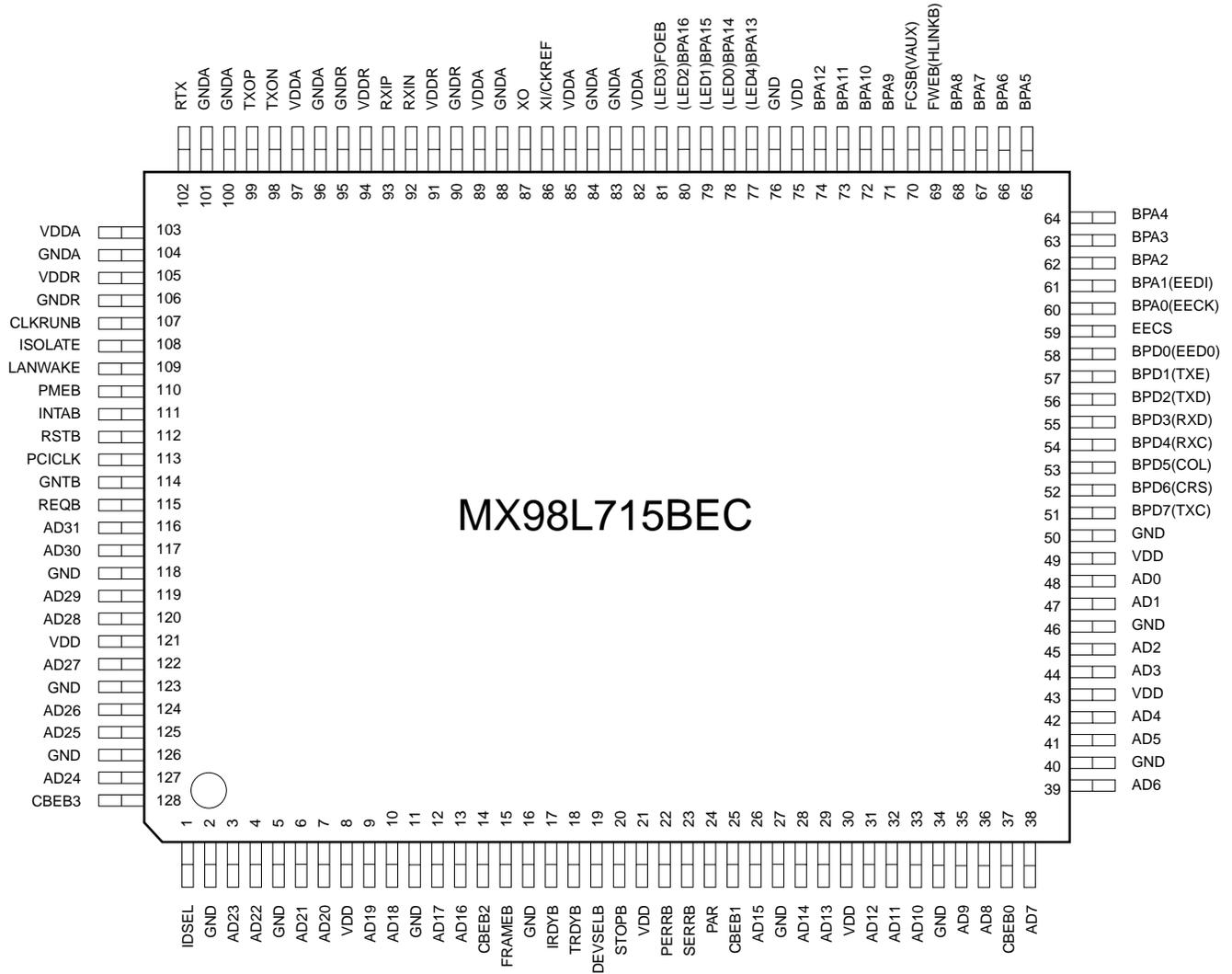
In MX98L715BEC, an innovative and proprietary design "Adaptive Network Throughput Control" (ANTC) is built-in to configure itself automatically by MXIC's driver based on the PCI burst throughput of different PCs. With this proprietary design, MX98L715BEC can always optimize its operating bandwidth, network data integrity and throughput for different PCs.

The MX98L715BEC features Remote-Power-On and Re-mote-Wake-Up capability and is compliant with the Ad-vanced Configuration and Power Interface version 1.0 (ACPI). This support enables a wide range of wake-up capabilities, including the ability to customize the content of specified packet which PC should respond to, even when it is in a low-power state. PCs and worksta-tions could take advantage of these capabilities of be-ing waked up and served simultaneous over the network by remote server or workstation. It helps organizations reduce their maintenance cost of PC network.

The 32-bit multiplexed bus interface unit of MX98L715BEC provides a direct interface to a PCI lo-cal bus, simplifying the design of an Ethernet adapter in a PC system. With its on-chip support for both little and big ending byte alignment, MX98L715BEC can also ad-dress non-PC applications.

3. PIN CONFIGURATIONS

Pin configuration diagram for MX98L715BEC (128-pin package).

Top side (pins 65–102): RTX, GNDA, GNDA, TXOP, TXON, VDDA, GNDA, GNDR, VDDR, RXIP, RXIN, VDDR, GNDR, VDDA, GNDA, XO, XI/CKREF, VDDA, GNDA, GNDA, VDDA, (LED3)FOEB, (LED2)BPA16, (LED1)BPA15, (LED0)BPA14, (LED4)BPA13, GND, VDD, BPA12, BPA11, BPA10, BPA9, FCSB(VAUX), FWEB(HLINKB), BPA8, BPA7, BPA6, BPA5

Left side (pins 103–128):
103 VDDA, 104 GNDA, 105 VDDR, 106 GNDR, 107 CLKRUNB, 108 ISOLATE, 109 LANWAKE, 110 PMEB, 111 INTAB, 112 RSTB, 113 PCICLK, 114 GNTB, 115 REQB, 116 AD31, 117 AD30, 118 GND, 119 AD29, 120 AD28, 121 VDD, 122 AD27, 123 GND, 124 AD26, 125 AD25, 126 GND, 127 AD24, 128 CBEB3

Right side (pins 39–64):
64 BPA4, 63 BPA3, 62 BPA2, 61 BPA1(EEDI), 60 BPA0(EECK), 59 EECS, 58 BPD0(EED0), 57 BPD1(TXE), 56 BPD2(TXD), 55 BPD3(RXD), 54 BPD4(RXC), 53 BPD5(COL), 52 BPD6(CRS), 51 BPD7(TXC), 50 GND, 49 VDD, 48 AD0, 47 AD1, 46 GND, 45 AD2, 44 AD3, 43 VDD, 42 AD4, 41 AD5, 40 GND, 39 AD6

Bottom side (pins 1–38): IDSEL, GND, AD23, AD22, GND, AD21, AD20, VDD, AD19, AD18, GND, AD17, AD16, CBEB2, FRAMEB, GND, IRDYB, TRDYB, DEVSELB, STOPB, VDD, PERRB, SERRB, PAR, CBEB1, AD15, GND, AD14, AD13, VDD, AD12, AD11, AD10, GND, AD9, AD8, CBEB0, AD7

4. PIN DESCRIPTION (128 PIN PQFP)

(T/S : tri-state, S/T/S : sustained tri-state, I : input, O : output, O/D : open drain)

Pin Name	Type	Pin No	128 Pin Function and Driver
AD[31:0]	T/S	116, 117 119,120, 122,124, 125,127, 3,4,6,7,9, 10,12,13, 26,28,29, 31-33,35, 36,38,39, 41,42,44, 45,47,48	PCI address/data bus: shared PCI address/data bus lines. Little or big ending byte ordering are supported.
CBEB[3:0]	T/S	128,14 25,37	PCI command and byte enable bus: shared PCI command byte enable bus, during the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable.
FRAMEB	S/T/S	15	PCI FRAMEB signal: shared PCI cycle start signal, asserted to indicate the beginning of a bus transaction. As long as FRAMEB is asserted, data transfers continue.
TRDYB	S/T/S	18	PCI Target ready: issued by the target agent, a data phase is completed on the rising edge of PCICLK when both IRDYB and TRDYB are asserted.
IRDYB	S/T/S	17	PCI Master ready: indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of PCICLK when both IRDYB and TRDYB are asserted.
DEVSELB	S/T/S	19	PCI slave device select: asserted by the target of the current bus access. When MX98L715BEC is the initiator of current bus access, the target must assert DEVSELB within 5 bus cycles, otherwise cycle is aborted.
IDSEL	I	1	PCI initialization device select: target specific device select signal for configuration cycles issued by host.
PCICLK	I	113	PCI bus clock input: PCI bus clock range from 16MHz to 33MHz.
RSTB	I	112	PCI bus reset: host system hardware reset.
LANWAKE	O	109	LAN wake up signal:asserts high to indicate one of the 3 wake up events has been detested in remote power on mode.
INTAB	O/D	111	PCI bus interrupt request signal: wired to INTAB line.
SERRB	O/D	23	PCI bus system error signal: If an address parity error is detected and CFCS bit 8 is enabled, SERRB and CFCS's bit 30 will be asserted.
PERRB	S/T/S	22	PCI bus data error signal: As a bus master, when a data parity error is detected and CFCS bit 8 is enabled, CFCS bit 24 and CSR5 bit 13 will be asserted. As a bus target, a data parity error will cause PERRB to be asserted.

Pin Name	Type	Pin No	128 Pin Function and Driver
PAR	T/S	24	PCI bus parity bit: shared PCI bus even parity bit for 32 bits AD bus and CBE bus.
STOPB	S/T/S	20	PCI Target requested transfer stop signal: as bus master, assertion of STOPB cause MX98L715BEC either to retry, disconnect, or abort.
REQB	T/S	115	PCI bus request signal: to initiate a bus master cycle request
GNTB	I	114	PCI bus grant acknowledge signal: host asserts to inform MX98L715BEC that access to the bus is granted
EECS	O	59	EEPROM Chip Select pin.
BPA1 (EEDI)	O	61	Boot PROM address bit 1(EECS=0): together with BPA[15:0] to access external boot PROM up to 256KB. EEPROM data in(EECS=1): EEPROM serial data input pin.
BPA0 (EECK)	O	60	Boot PROM address bit 0(EECS=0): together with BPA[15:0] to access external boot PROM up to 256KB. EEPROM clock(EECS=1): EEPROM clock input pin
BPA[12:0]	O	74-71, 68-60	Boot PROM address line.
BPA13 (LED4)	O	77	Boot PROM address line 13 (LED4)
BPA14 (LED0)	O	78	Boot PROM address line 14 (LED0)
BPA15 (LED1)	O	79	Boot PROM address line 15 (LED1)
BPA16 (LED2)	O	80	Boot PROM address line 16 (LED2)
BPD0 (EEDO)	T/S	58	Boot PROM data line 0(EECS=0): boot PROM or flash data line 0. EEPROM data out(EECS=1): EEPROM serial data outpin(during reset initialization).
BPD[7:0]	T/S	51-58	Boot PROM data lines: boot PROM or flash data lines 7-0.
FWEB (HLINKB)	T/S	69	Flash Write Enable Output (or Home PNA Link active low input)
FCSB (VAUX)	T/S	70	Boot PROM Chip Select Output or Auxiliary Vdd input with 10k external resistor pull-up. (Internal pull-down)
FOEB (LED3)	O	81	Boot PROM Output Enable (LED3)
RTX	O	102	Connecting an external resistor to ground, Resistor value=1K ohms
PMEB	O/D	110	Power Management Event Status Output

| Pin Name	Type	Pin No	128 Pin Function and Driver
RXIP	I	93	Twisted pair receive differential input: Support both 10 Base-T and 100 Base-TX receive differential input.
RXIN	I	92	Twisted pair receive differential input: Support both 10 Base-T and 100 Base-TX receive differential input
TXOP	O	99	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
TXON	O	98	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
XI/CKREF	I	86	Reference clock: 25MHz oscillator clock input or Crystal in pin
XO	I	87	Crystal out pin
LED0	O	78	Programmable LED0 pin: CSR9.28=1 Set the LED0 as Link Speed (10/100) LED. CSR9.28=0 Set the LED0 as Activity LED. Default is Activity LED after reset.
LED1	O	79	Programmable LED1 pin: CSR9.29=1 Set the LED1 as Link/Activity LED. CSR9.29=0 Set the LED1 as Good Link LED. Default is Good Link LED after reset.
LED2	O	80	Programmable LED2 pin: CSR9.30=1 Set the LED2 as Collision LED. CSR9.30=0 Set the LED2 as Link Speed (10/100) LED. Default is Link Speed (10/100) LED after reset.
LED3	O	81	Programmable LED3 pin: CSR9.31=1 Set the LED3 as Full/Half Duplex LED. CSR9.31=0 Set the LED3 as RX LED. Default is RX LED after reset.
LED4	O	77	Programmable LED4 pin: CSR9.24=1 Set the LED4 as Power Management Event LED. CSR9.24=0 Set the LED4 as COL LED. Default is Collision LED after reset.
VDD	P	8,21,30,43, 49,75,121	Digital Power pins.
GND	G	2,5,11,16,27 34,40,46,50 76,118,123, 126	Digital Ground pins.

| Pin Name	Type	Pin No	128 Pin Function and Driver
VDDA	P	82, 85, 89, 97,103,	Analog Power pins.
GNDA	G	83,84,88,96, 100,101,104,	Analog Ground pins.
VDDR	P	91, 94,105	Receive Channel Power pins.
GNDR	G	90, 95,106	Receive Channel Ground pins.
TXE (BPD1)	T/S	57	Transmit Enable Output : TXE signal in 7 wire interface for Home PNA connection. (Or BPD1 pin during Flash or boot ROM activities)
TXD (BPD2)	T/S	56	Transmit Data Output : TXD signal in 7 wire interface for Home PNA connection. (Or BPD2 pin during Flash or boot ROM activities)
RXD (BPD3)	T/S	55	Receive Data Input : RXD signal in 7 wire interface for Home PNA connection. (Or BPD3 pin during Flash or boot ROM activities)
RXC (BPD4)	T/S	54	Receive Clock Input : RXC signal in 7 wire interface for Home PNA connection. (Or BPD4 pin during Flash or boot ROM activities)
COL (BPD5)	T/S	53	Collision Input : COL signal in 7 wire interface for Home PNA connection. (Or BPD5 pin during Flash or boot ROM activities)
CRS (BPD6)	T/S	52	Transmit Enable Output : CRS signal in 7 wire interface for Home PNA connection. (Or BPD6 pin during Flash or boot ROM activities)
TXC (BPD7)	T/S	51	Transmit Clock Input : TXC signal in 7 wire interface for Home PNA connection. (Or BPD7 pin during Flash or boot ROM activities)
CLKRUNB	T/S	107	Mini PCI bus CLock Run pin : Indicates the MiniPCI clock status, normally controlled by host, low for normal clocking, high when clock is about to be slowed down. Can be asserted low by MX98L715BEC to request normal clocking when necessary.
ISOLATE	T/S	108	ISOLATE pin : Output pin to isolate external Home PNA PHY chip

5. PROGRAMMING INTERFACE

5.1 PCI CONFIGURATION REGISTERS:

5.1.1 PCI ID REGISTER (PFID) (Offset 03h-00h)
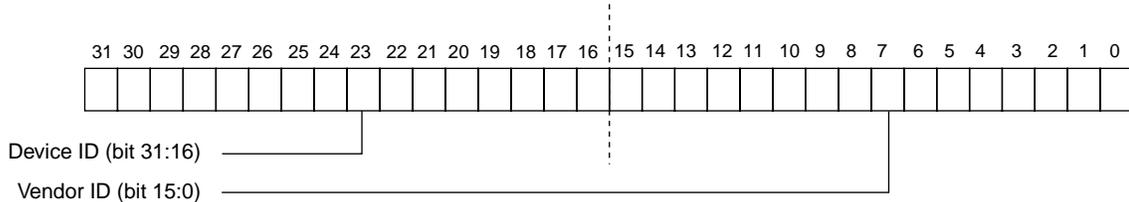
This register can be loaded from external serial EEPROM or use a MXIC preset value of "10D9" and "0531" for vendor ID and device ID respectively. Word location 3Eh and 3Dh in serial EEPROM are used to configure customer's vendor ID and device ID respectively. If location 3Eh contains"FFFF" value then MXIC's vendor ID and device ID will be set in this register, otherwise both 3Eh and 3Dh will be loaded into this register from serial EEPROM.

5.1.2 PCI COMMAND AND STATUS REGISTER (PFCS) (Offset 07h-04h)
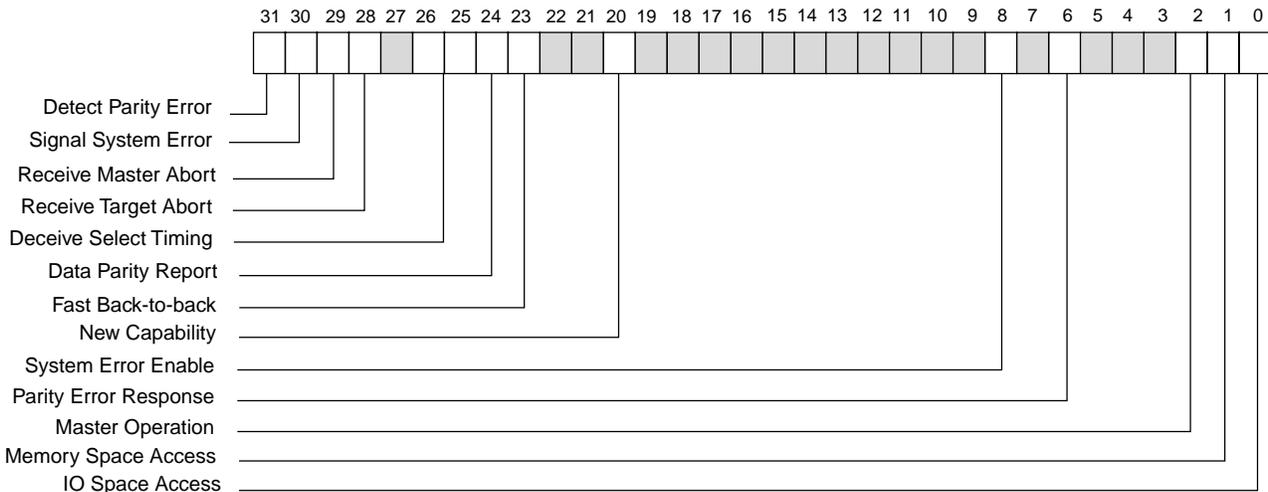
The bit content will be reset to 0 when a 1 is written to the corresponding bit location.

bit 0 : IO Space Access, set to 1 enable IO access
bit 1 : Memory Space Access, set to 1 to enable memory access
bit 2 : Master Operation, set to 1 to support bus master mode
bit 5-3 : not used
bit 6 : Parity Error Response, set to 1 to enable assertion of CSR<13> bit if parity error detected.
bit 7 : not used
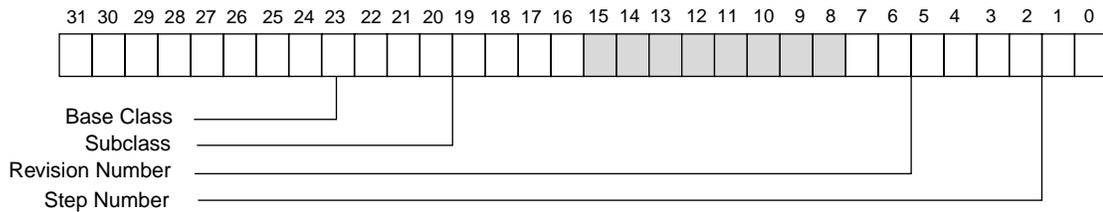bit 8 : System Error Enable, set to 1 to enable SERR# when parity error is detected on address lines and CBE[3:0].
bit 20 : New capability. Set to support PCI power management.
bit 22-bit19 : not used
bit 23 : Fast Back-to back, always set to accept fast back-to-back transactions that are not sent to the same bus device.

bit 24:Data Parity Report, is set to 1 only if PERR# active and PFCS<6> is also set.
bit 26-25:Device Select Timing of DEVSELB pin.
bit 27:not used
bit 28:Receive Target Abort, is set to indicate a transaction is terminated by a target abort.
bit 29:Receive Master Abort, is set to indicate a master transaction with Master abort.
bit 30:Signal System Error, is set to indicate assertion of SERRB.
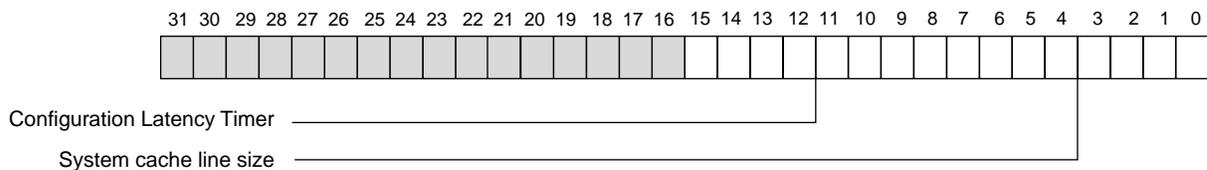bit 31:Detected Parity Error, is set whenever a parity error detected regardless of PFCS<6>.

5.1.3 PCI REVISION REGISTER (PFRV) (Offset 0Bh-08h)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Base Class
Subclass
Revision Number
Step Number

bit 3 - 0 : Step Number, range from 0 to Fh.
bit 7 - 4 : Revision Number, fixed to 6h for MX98L715BEC
bit 15 - 8 : not used
bit 23 - 16 : Subclass, fixed to 0h.
bit 31 - 24 : Base Class, fixed to 2h.

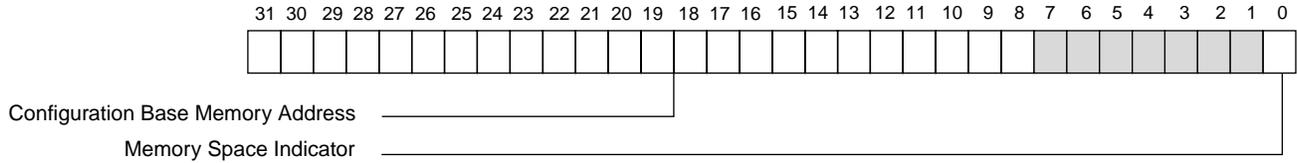### 5.1.4 PCI LATENCY TIMER REGISTER (PFLT) (Offset 0Fh-0Ch)

PFLT Register (0Fh-0Ch)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Configuration Latency Timer
System cache line size

bit 0 - bit 7 : System cache line size in units of 32 bit word, device driver should use this value to program CSR0<15:14>.
bit 8 - bit 15 : Configuration Latency Timer, when MX98L715BEC assert FRAMEB, it enables its latency timer to count.

If MX98L715BEC desserts FRAMEB prior to timer expiration, then timer is ignored. Otherwise, after timer expires, MX98L715BEC initiates transaction termination as soon as its GNTB is deserted.

5.1.5 PCI BASE IO ADDRESS REGISTER (PBIO) (Offset 13h-10h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Configuration Base Memory Address ——————
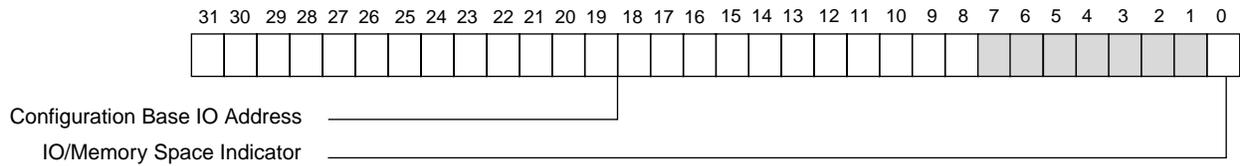
Memory Space Indicator ——————

bit 0 : IO/Memory Space Indicator, fixed to 1 in this field will map into the IO space. This is a read only field.
bit 7 - 1 : not used, all 0 when read
bit 31 - 8 : Defines the address assignment mapping of MX98L715BEC CSR registers.

5.1.6 PCI Base Memory Address Register (PBMA) (Offset 17h-14h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Configuration Base IO Address ——————
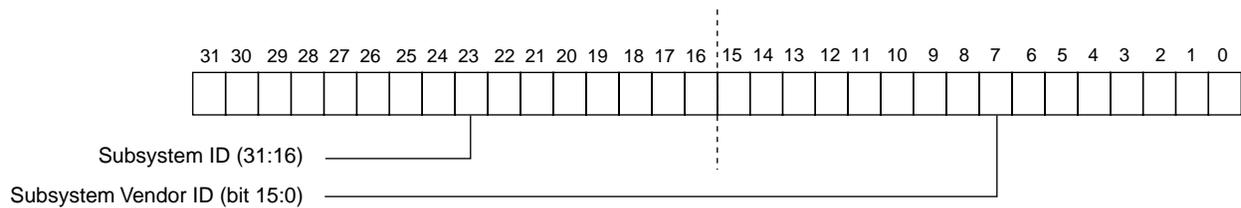
IO/Memory Space Indicator ——————

bit 0 : Memory Space Indicator, fixed to 0 in this field will map into the memory space. This is a read only field.
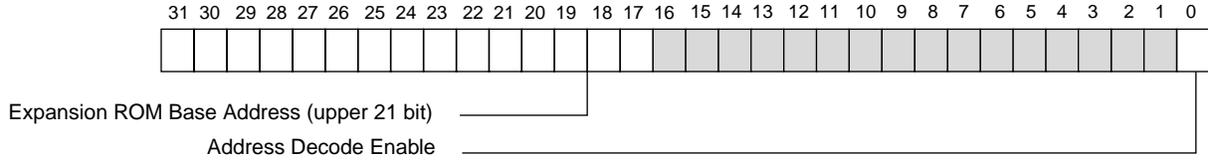bit 7 - 1 : not used, all 0 when read
bit 31 - 7 : Defines the address assignment mapping of MX98L715BEC CSR registers.

5.1.7 PCI SUBSYSTEM ID REGISTER (PSID) (Offset 2Fh-2Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Subsystem ID (31:16) ——————

Subsystem Vendor ID (bit 15:0) ——————

This register is used to uniquely identify the add-on board or subsystem where the NIC controller resides. Values in this register are loaded directly from external serial EEPROM after system reset automatically. Word location 36h of EEPROM is subsystem vendor ID and location 35h is subsystem ID.

5.1.8 PCI BASE EXPANSION ROM ADDRESS REGISTER (PBER) (Offset 33h-30h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Expansion ROM Base Address (upper 21 bit)
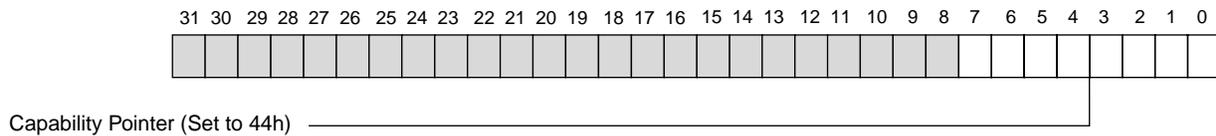
Address Decode Enable

bit 0 : Address Decode Enable, decoding will be enabled if only both enable bit in PFCS<1> and this expansion ROM
register are 1.

bit 16 - 1 : not use

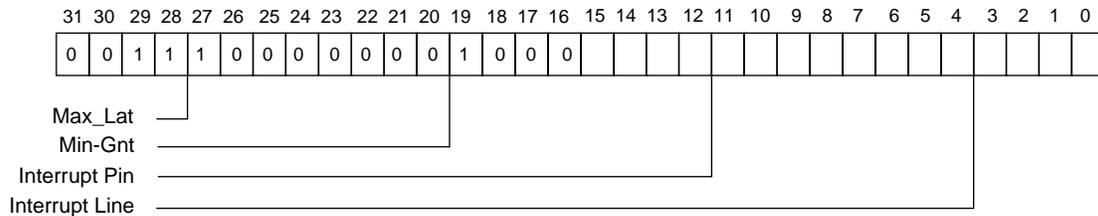bit 31 - 17 : Defines the upper 21 bits of expansion ROM base address.

5.1.9 PCI CAPABILITY POINTER REGISTER (PFCP) (Offset 37h-34h)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Capability Pointer (Set to 44h)

bit 7- 0 : Capability pointer (Cap_Ptr) is set to 44h.

bit 31- 8 : reserved

5.1.10 INTERRUPT REGISTER (PFIT) (Offset 3Fh-3Ch)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0															

Max_Lat

Min-Gnt

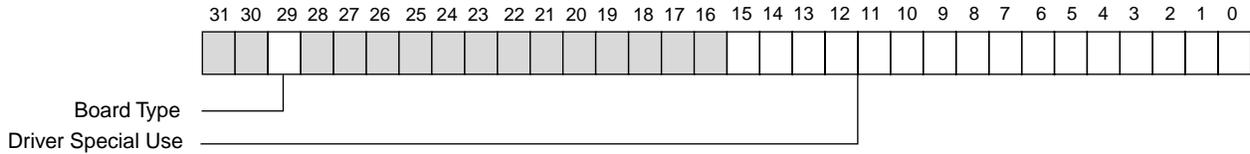Interrupt Pin

Interrupt Line

bit 7 - 0 : Interrupt Line, system BIOS will writes the routing information into this field, driver can use this information
to determine priority and interrupt vector.

bit 15 - 8 : Interrupt Pin, fixed to 01h which use INTA#.

bit 31 - 24 : Max_Lat which is a maximum period for a access to PCI bus.
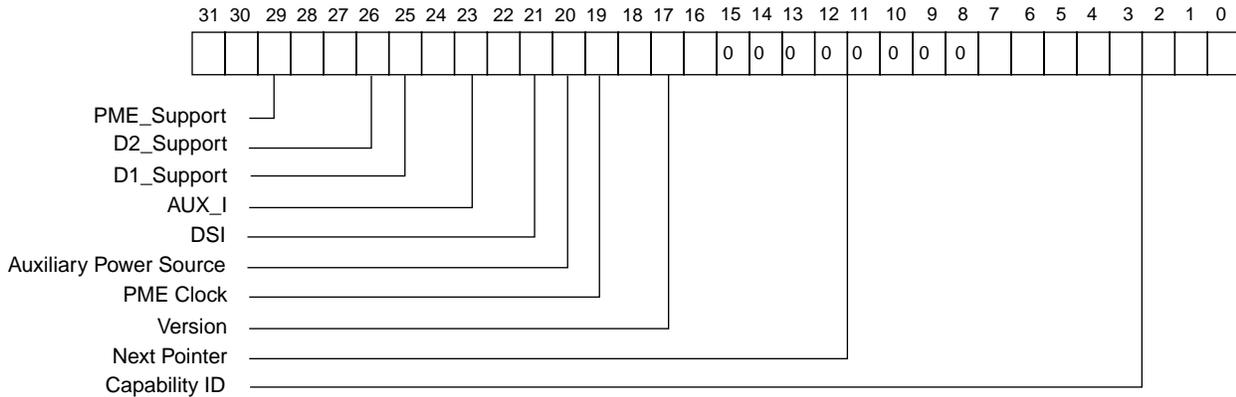
bit 23 - 16 : Min_Gnt which is the maximum period that MX98L715BEC needs to finish a burst PCI cycle.

5.1.11 PCI DRIVER AREA REGISTER (PFDA) (43h-40h)

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Board Type ——
Driver Special Use ——

bit 29 : board type
bit 15 - 8 : driver is free to read and write this field for any purpose.
bit 7 - 0 : not used.

5.1.12 PCI POWER MANAGEMENT CAPABILITY REGISTER (PPMC) (47h-44h)

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |

PME_Support ——
D2_Support ——
D1_Support ——
AUX_I ——
DSI ——
Auxiliary Power Source ——
PME Clock ——
Version ——
Next Pointer ——
Capability ID ——

bit 31- 27 : PME_Support, read only indicates the power states in which the function may assert LANWAKE pin.
  bit 31 ---- PME_D3cold (value depending on Vaux / FCSB pin)
  bit 30 ---- PME_D3hot
  bit 29 ---- PME_D2
  bit 28 ---- PME_D1
  bit 27 ---- PME_D0
bit 26 : D2 mode support, read only, set to 1.
bit 25 : D1 mode support, read only, set to 1.
bit 24-22 : AUX_I bits. Auxiliary current field, set to 000.
bit 21 : DSI, read only, reset to 0.
bit 20 : Auxiliary power source, supporting D3cold, set to 1. This bit is valid only when bit 15 is a '1'.
bit 19 : PME Clock, read only, reset to 0.
bit 18-16 : PCI power management version1.1, set to 010, read only.
bit 15-8 : Next Pointer, all bits reset to 0.
bit 7-0 : Capability ID, read only, set to 1 indicates support of power management

P/N:PM0695   REV. 0.3, MAR. 30, 2001

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5.1.13 PCI POWER MANAGEMENT COMMAND AND STATUS REGISTER (PPMCSR) (4Bh-48h)
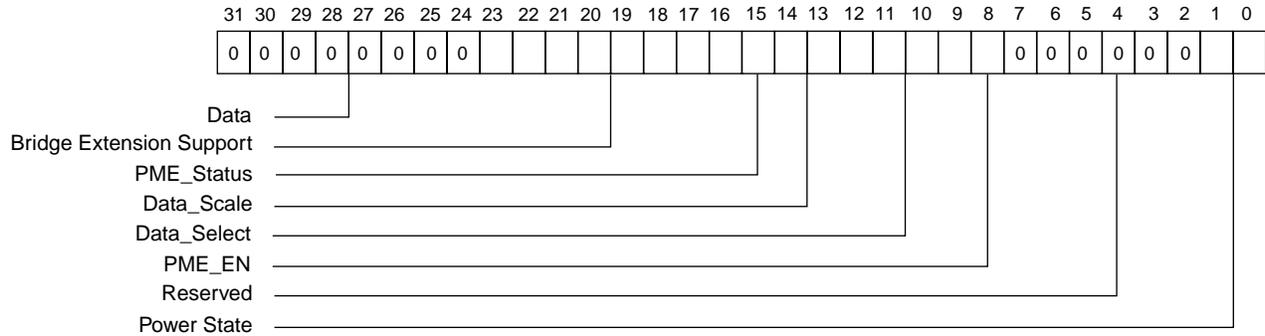
bit 1-0 : Power_State, read/write, D0 mode is 00, D1 mode is 01, D2 mode is 10, D3 hot mode is 11.

bit7-2 : all 0. Reserved.

bit8 : PME_EN, set 1 to enable PMEB and LANWAKE pins. Set 0 to disable PMEB and LANWAKE assertion.

bit 12-9 : Data_Select for report in the Data register located at bit 31:24. Not supported, reset to 0.

bit 14-13 : Data_Scale, read only, not supported, reset to 0.

bit 15 : PME_Status independent of the state of PME_EN. Cleared during power up.

When set, indicates a PME event.

Write 1 to clear the PMEB and LANWAKE assertion, PME-Status become 0. Write 0, no effect.

bit 21-16 : Reserved.

bit 22 : B2_B3# = 0, BPCC_EN = 1, read only, not support.

bit 23 : BPCC_EN = 0, Bus Power/Clock Control Enable, read only, not support.

bit 31-24 : Data = 0, read only, not support.

5.2 HOST INTERFACE REGISTERS

MX98L715BEC CSRs are located in the host I/O or memory address space. The CSRs are double word aligned and 32 bits long. Definitions and address for all CSRs are as follows :
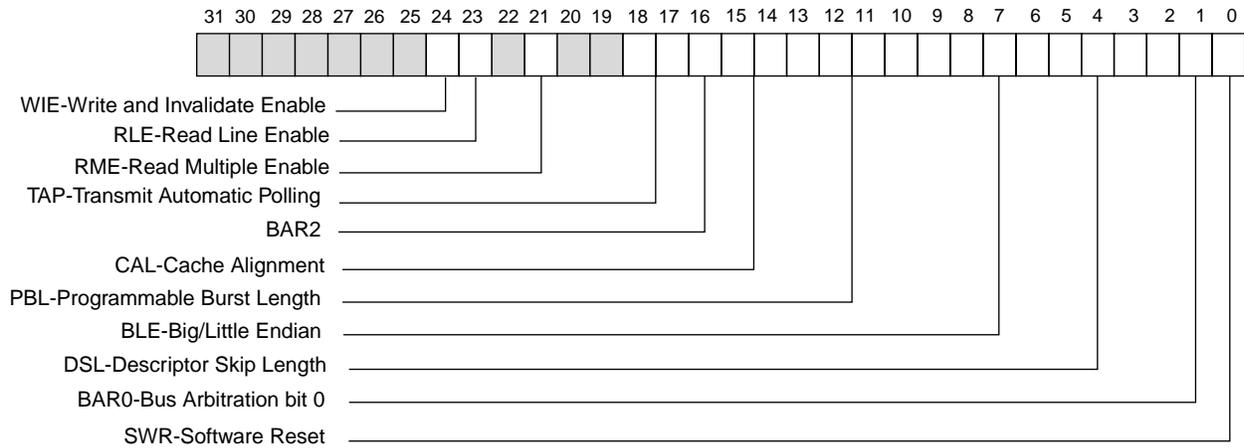
CSR Mapping

Register	Meaning	Offset from CSR Base Address (PBIO and PBMA)
CSR0	Bus mode	00
CSR1	Transmit poll demand	08h
CSR2	Receive poll demand	10h
CSR3	Receive list base address	18h
CSR4	Transmit list base address	20h
CSR5	Interrupt status	28h
CSR6	Operation mode	30h
CSR7	Interrupt enable	38h
CSR8	Missed frame counter	40h
CSR9	Serial ROM and MII management	48h
CSR10	Flash Memory Address Register	50h
CSR11	General Purpose timer	58h
CSR12	10 Base-T status port	60h
CSR13	SIA Reset Register	68h
CSR14	10 Base-T control port	70h
CSR15	Watchdog timer	78h
CSR16	(Reserved) Test Operation port	80h
CSR17	(Reserved) IC Test Port-1	88h
CSR18	(Reserved) IC Test Port-2	90h
CSR19	(Reserved) IC test Port-3	98h
CSR20	Auto compensation	A0h
CSR21	Flow control Register	A4h
CSR22	MAC ID Byte 3-0	A8h
CSR23	Magic ID 5, 4 / MAC ID Byte 5, 4	ACh
CSR24	Magic ID Byte 3-0	B0h
CSR25	Filter 0 Byte Mask	B4h
CSR26	Filter 1 Byte Mask	B8h
CSR27	Filter 2 Byte Mask	BCh
CSR28	Filter 3 Byte mask	C0h
CRS29	Filter Offset	C4h
CSR30	Filter 1&0 CRC-16	C8h
CSR31	Filter 3&2 CRC-16	CCh

CSR32	Reserved A Register 1	D0h
CSR33	Reserved A Register 2	D4h
CSR34	Reserved A Register 3	D8h
CSR35	Reserved A Register 4	DCh
CSR36	Reserved A Register 5	E0h
CSR37	Reserved P Register	E4h
CSR38	VLAN Tag Register	E8h
CSR39	Power Management Register	ECh

5. 2.1 BUS MODE REGISTER (CSR0)

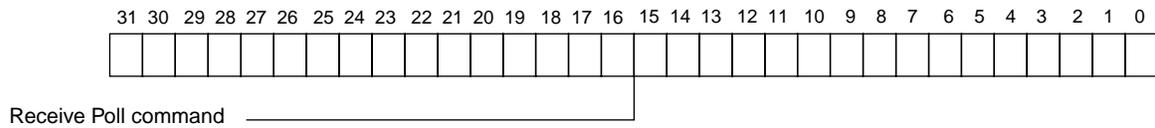| Field	Name	Description
0	SWR	Software Reset, when set, MX98L715BEC resets all internal hardware with the exception of the configuration area and port selection.
1	BAR0	Internal bus arbitration scheme between receive and transmit processes. The receive channel usually has higher priority over transmit channel when receive FIFO is partially full to a threshold. This threshold can be selected by programming this bit. Set for lower threshold, reset for normal threshold.
6:2	DSL	Descriptor Skip Length, specifies the number of longwords to skip between two descriptors.
7	BLE	Big/Little Ending, set for big ending byte ordering mode, reset for little ending byte ordering mode, this option only applies to data buffers
13:8	PBL	Programmable Burst Length, specifies the maximum number of longwords to be transferred in one DMA transaction. default is 0 which means unlimited burst length, possible values can be 1,2,4,8,16,32 and unlimited .
15:14	CAL	Cache Alignment, programmable address boundaries of data burst stop, MX98L715BEC can handle non-cache- aligned fragment as well as cache-aligned fragment efficiently.
16	BAR2	Reset to use RX dominate arbitration. Set to use TX dominant arbitration in fast forward mode or round Robin in store/forward mode. Must be reset to zero for normal operation.
18:17	TAP	Transmit Auto-Polling time interval, defines the time interval for MX98L715BEC to performs transmit poll command automatically at transmit suspended state.
21	RME	PCI Memory Read Multiple command enable, indicates bus master may intend to fetch more than one cache lines disconnecting.
23	RLE	PCI Memory Read Line command enable, indicating bus master intends to fetch a complete cache line.
24	WIE	PCI Memory Write and Invalidate command enable, guarantees a minimum transfer of one complete cache.

TABLE 5.2.0 TRANSMIT AUTO POLLING BITS

CSR<18:17>	Time Interval
00	No transmit auto-polling, a write to CSR1 is required to poll
01	auto-poll every 200 us
10	auto-poll every 800 us
11	auto-poll every 1.6 ms

5.2.2 TRANSMIT POLL COMMAND (CSR1)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Transmit Poll command
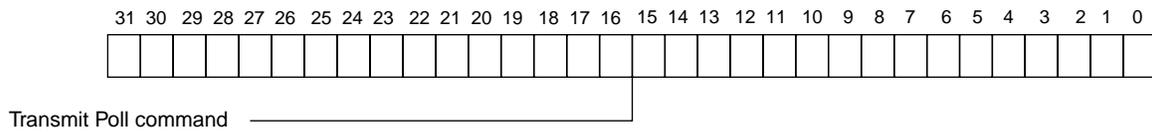
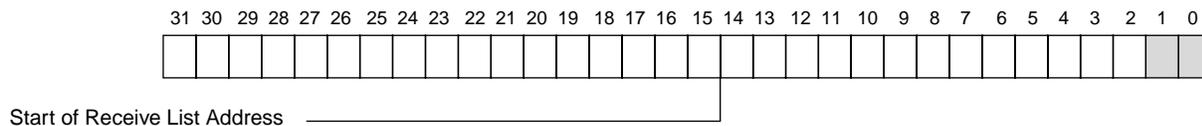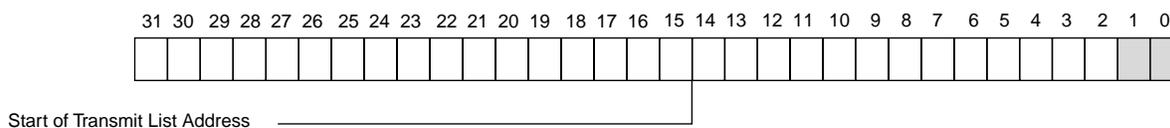| Field	Name	Description
31:0	TPC	Write only, when written with any value, MX98L715BEC read transmit descriptor list in host memory pointed by CSR4 and processes the list.

5.2.3 RECEIVE POLL COMMAND (CSR2)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Receive Poll command

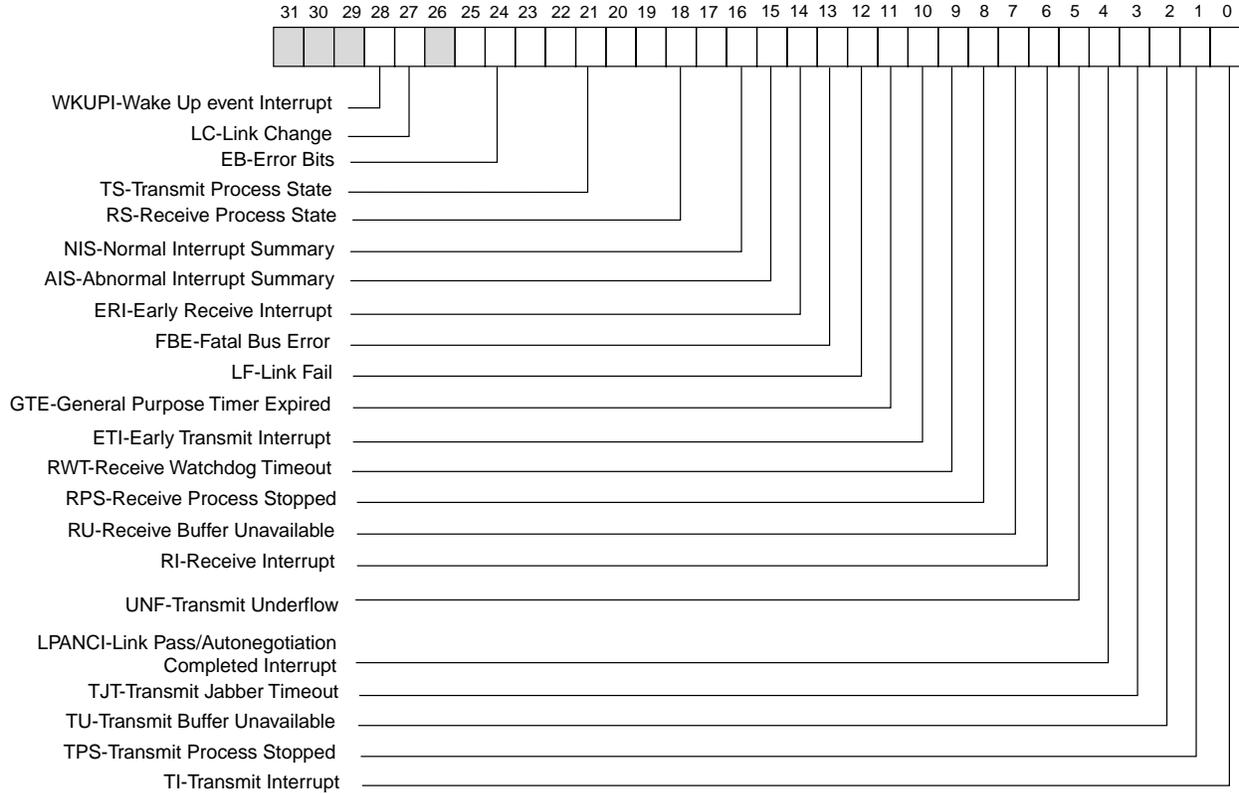| Field	Name	Description
31:0	RPC	Write only, when written with any value, MX98L715BEC read receive descriptor list in host memory pointed by CSR3 and processes the list.

5.2.4 DESCRIPTOR LIST ADDRESS (CSR3, CSR4)

CSR3 Receive List Base Address

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Start of Receive List Address

CSR4 Transmit List Base Address

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Start of Transmit List Address

5.2.5 INTERRUPT STATUS REGISTER (CSR5)

Field	Name	Description
28	WKUPI	Wake Up event interrupt. Set if wake-up event occurs in power-down mode.
27	LC	100 Base-TX link status has changed either from pass to fail or fail to pass. Read CSR12<1> for 100 Base-TX link status.
25:23	EB	Error Bits, read only, indicating the type of error that caused fatal bus error.
22:20	TS	Transmit Process State, read only bits indicating the state of transmit process.
19:17	RS	Receive Process State, read only bits indicating the state of receive process.
16	NIS	Normal Interrupt Summary, is the logical OR of CSR5<0>, CSR5<2> and CSR5<6> and CSR5<28>.
15	AIS	Abnormal Interrupt Summary, is the logical OR of CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CAR5<10>, CSR5<11> and CSR5<13>, CSR5<27>.
14	ERI	Early receive interrupt, indicating the first buffer has been filled in ring mode, or 64 bytes has been received in chain mode.
13	FBE	Fatal Bus Error, indicating a system error occurred, MX98L715BEC will disable all bus access.
12	LF	Link Fail, indicates a link fail state in 10 Base-T port. This bit is valid only when CSR6<18>=0, CSR14<8>=1, and CSR13<3>=0.

Field	Name	Description
11	GTE	General Purpose Timer Expired, indicating CSR11 counter has expired.
10	ETI	Early Transmit Interrupt, indicating the packet to be transmitted was fully transferred to internal TX FIFO. CSR5<0> will automatically clears this bit.
9	RWT	Receive Watchdog Time-out, reflects the network line status where receive watchdog timer has expired while the other node is still active on the network.
8	RPS	Write only, when written with any value, MX98L715BEC reads receive descriptor list in host memory pointed by CSR4 and processes the list.
7	RU	Receive Buffer Unavailable, the receive process is suspended due to the next descriptor in the receive list is owned by host. If no receive poll command is issued, the reception process resumes when the next recognized incoming frame is received.
6	RI	Receive Interrupt, indicating the completion of a frame reception.
5	UNF	Transmit Underflow, indicating transmit FIFO has run empty before the completion of a packet transmission.
4	LPANCI	When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10 Base-T link integrity test has completed successfully, after the link was down. This bit is also set as as a result of writing 0 to CSR14<12> (Link Test Enable). When Autonegotiation is enabled (CSR14<7> =1) , this bit indicates that the autonegotiation has completed (CSR12<14:12>=5). CSR12 should then be read for a link status report. This bit is only valid when CSR6<18>=0, i.e. 10 Base-T port is selected Link Fail interrupt (CSR5<12>) will automatically clears this bit.
3	TJT	Transmit Jabber Timeout, indicating the MX98715 has been excessively active. The transmit process is aborted and placed in the stopped state. TDES0<1> is also set.
2	TU	Transmit Buffer Unavailable, transmit process is suspended due to the next descriptor in the transmit list is owned by host.
1	TPS	Transmit Process Stopped.
0	TI	Transmit Interrupt. indicating a frame transmission was completed.

TABLE 5.2.1 FATAL BUS ERROR BITS

CSR5<25:23>	Process State
000	parity error for either SERR# or PERR#, cleared by software reset.
001	master abort
010	target abort
011	reserved
1XX	reserved

TABLE 5.2.2 TRANSMIT PROCESS STATE

CSR5<22:20>	Process State
000	Stopped- reset or transmit jabber expired.
001	Fetching transmit descriptor
010	Waiting for end of transmission
011	filling transmit FIFO
100	reserved
101	Setup packet
110	Suspended, either FIFO underflow or unavailable transmit descriptor
111	closing transmit descriptor

TABLE 5.2.3 RECEIVE PROCESS STATE

CSR5<19:17>	Process State
000	Stopped- reset or stop receive command. Fetching receive descriptor
010	checking for end of receive packet
011	Waiting for receive packet
100	Suspended, receive buffer unavailable
101	closing receive descriptor
110	Purging the current frame from the receive FIFO due to unavailable receive buffer
111	queuing the receive frame from the receive FIFO into host receive buffer

5.2.6 OPERATION MODE REGISTER (CSR6)


```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

SCR-Scrambler Mode
PCS-PCS function
TTM-Transmit Threshold Mode
SF-Store and Forward
HBD-Hearbeat Disable
PS-Port Select
COE-Collision Offset Enable
TR-Threshold Control Bits
ST-Start/Stop Transmission Command
FC-Force collision mode
LOM-Loopback Operation Mode
FD-Full Duplex Mode
FKD
PM-Pass All Multicast
PR-Promiscuous Mode
SB-Start/Stop Backoff Counter
IF-Inverse Filtering
PB-Pass Bad Frame
HO-Hash-Only Filtering Mode
SR-Start/Stop Receive
HP-Hash/Perfect Receive Filtering Mode

Field	Name	Description
24	SCR	Scrambler Mode, default is set to enable scrambler function. Not affected by software reset.
23	PCS	Default is set to enable PCS functions. CSR6<18> must be set in order to operate in symbol mode.
22	TTM	Transmit Threshold Mode, set for 10 Base-T and reset for 100 Base-TX.
21	SF	Store and Forward, when set, transmission starts only if a full packet is in transmit FIFO. the threshold values defined in CSR6<15:14> are ignored
19	HBD	Heartbeat Disable, set to disable SQE function in 10 Base-T mode.
18	PS	Port Select, default is 0 which is 10 Base-T mode, set for 100 Base-TX mode. A software reset does not affect this bit.
17	COE	Collision Offset Enable, set to enable a modified backoff algorithm during low collision situation, reset for normal backoff algorithm.
15:14	TR	Threshold Control Bits, these bits controls the selected threshold level for MX98L715BEC's transmit FIFO, transmission starts when frame size within the transmit FIFO is larger than the selected threshold. Full frames with a length less than the threshold are also transmitted.

Field	Name	Description
13	ST	Start/Stop Transmission Command, set to place transmission process in running state and will try to transmit current descriptor in transmit list. When reset, transmit process is placed in stop state.
12	FC	Force Collision Mode, used in collision logic test in internal loopback mode, set to force collision during next transmission attempt. This can result in excessive collision reported in TDES0<8> if 16 or more collision.
11:10	LOM	Loopback Operation Mode, see table 5.2.6.
9	FD	Full-Duplex Mode, set for simultaneous transmit and receive operation, heart beat check is disabled, TDES0<7> should be ignored, and internal loopback is not allowed. This bit controls the value of bit 6 of link code word .
8	FKD	Reserved for internal test for back off speeding up
7	PM	Pass All Multicast, set to accept all incoming frames with a multicast destination address are received. Incoming frames with physical address are filtered according to the CSR6<0> bit.
6	PR	Promiscuous Mode, any incoming valid frames are accepted, default is reset and not affected by software reset.
5	SB	Start/Stop Backoff Counter, when reset, the backoff timer is not affected by the network carrier activity. Otherwise, timer will start counting when carrier drops.
4	IF	Inverse Filtering, read only bit, set to operate in inverse filtering mode, only valid during perfect filtering mode.
3	PB	Pass Bad Frames, set to pass bad frame mode, all incoming frames passed the address filtering are accepted including runt frames, collided fragments, truncated frames caused by FIFO overflow.
2	HO	Hash-Only Filtering Mode , read only bit, set to operate in imperfect filtering mode for both physical and multicast addresses.
1	SR	Start/Stop Receive, set to place receive process in running state where descriptor acquisition is attempted from current position in the receive list. Reset to place the receive process in stop state.
0	HP	Hash/Perfect Receive Filtering Mode, read only bit, set to use hash table to filter multicast incoming frames. If CSR6<2> is also set, then the physical addresses are imperfect address filtered too. If CSR6<2> is reset, then physical addresses are perfect address filtered, according to a single physical address as specified in setup frame.

TABLE 5.2.4 TRANSMIT THRESHOLD

CSR6<21>	CSR6<15:14>	CSR6<22>=0 (for 100 Base-TX)	CSR6<22>=1 (Threshold bytes) (for 10 Base-T)
0	00	128	72
0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	(Store and Forward)	

TABLE 5.2.5 DATA PORT SELECTION

CSR14<7>	CSR6<18>	CSR6<22>	CSR6<23>	CSR6<24>	Port
1	0	X	X	X	Nway Auto-negotiation
0	0	1	X	X	10 Base-T
0	1	0	1	1	100 Base-TX

TABLE 5.2.6 LOOPBACK OPERATION MODE

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback at FIFO port
11	Internal loopback at the PHY level
10	External loopback at the PMD level

TABLE 5.2.7 FILTERING MODE

CSR6<7> PM	CSR6<6> PR	CSR6<4> IF	CSR6<2> HO	CSR6<0> HP	Filtering Mode
0	0	0	0	0	CAM 16-entry perfect filtering
0	0	0	0	1	64-bit hash (mulitcast=1) + 1perfect (entry 0) filtering. (multicast=0)
0	0	0	1	1	64-bit hash for multicast
0	0	1	X	0	Inverse filtering. Only valid with CSR6<0>=0
X	1	X	X	X	Promiscuous (Pass all kinds)
1	0	X	X	X	Pass All Multicast

5.2.7 INTERRUPT MASK REGISTER (CSR7)
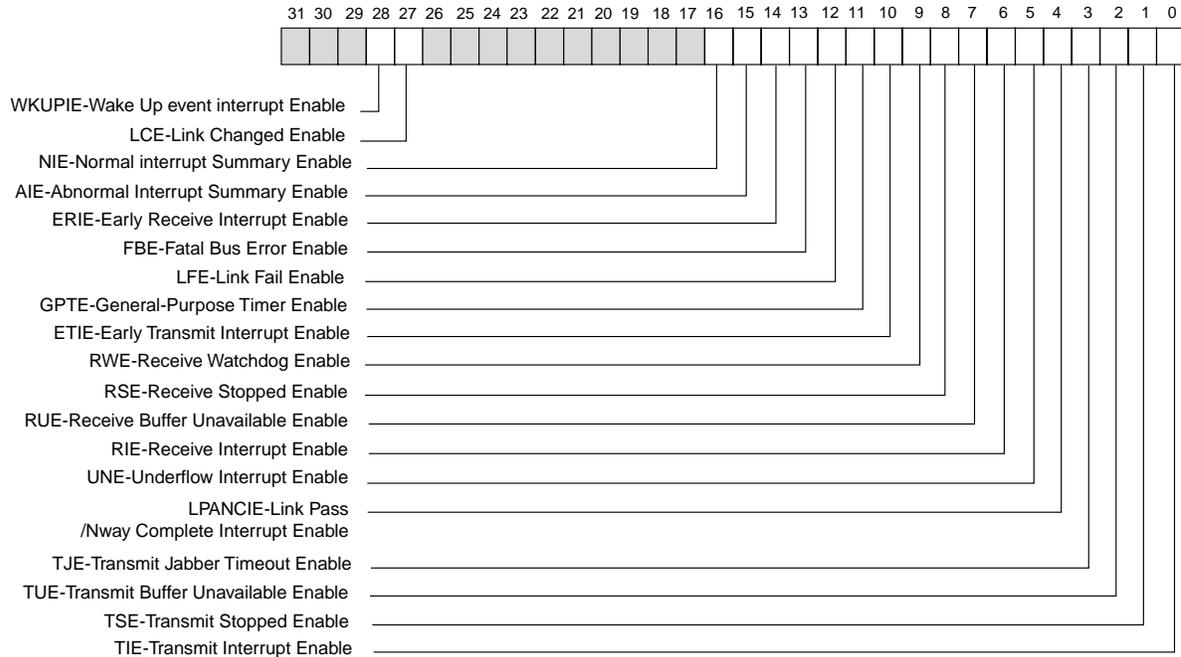
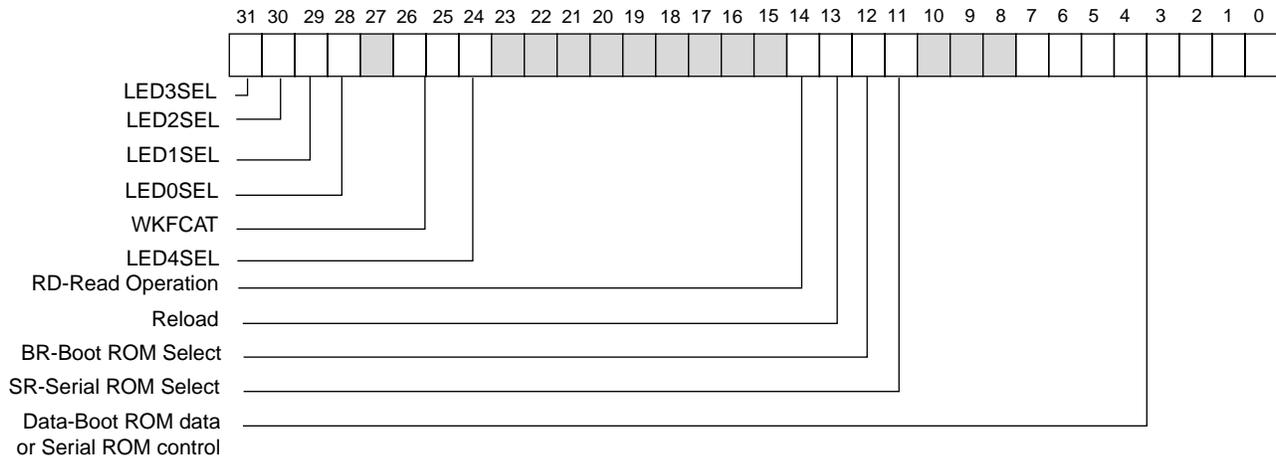| Field	Name	Description
28	WKUPIE	Wake Up Event Interrupt Enable, enables CSR5<28>.
27	LCE	Link Changed Enable, enables CSR5<27>.
16	NIE	Normal Interrupt Summary Enable, set to enable CSR5<0>, CSR5<2>, CSR5<6>.
15	AIE	Abnormal Interrupt Summary enable, set to enable CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
14	ERIE	Early Receive Interrupt Enable
13	FBE	Fatal Bus Error Enable, set together with with CSR7<15> enables CSR5<13>.
12	LFE	Link Fail Interrupt Enable, enables CSR5<12>
11	GPTE	General Purpose Timer Enable, set together with CSR7<15> enables CSR5<11>.
10	ETIE	Early Transmit Interrupt Enable, enables CSR5<10>
9	RWE	Receive Watchdog Timeout Enable, set together with CSR7<15> enables CSR5<9>.
8	RSE	Receive Stopped Enable, set together with CSR7<15> enables CSR5<8>.
7	RUE	Receive Buffer Unavailable Enable, set together with CSR7<15> enables CSR5<7>.
6	RIE	Receive Interrupt Enable, set together with CSR7<16> enables CSR5<6>.
5	UNE	Underflow Interrupt Enable, set together with CSR7<15> enables CSR5<5>.
4	LPANCIE	Link Pass/Autonegotiation Completed Interrupt Enable
3	TJE	Transmit Jabber Timeout Enable, set together with CSR7<15> enables CSR5<3>.
2	TUE	Transmit Buffer Unavailable Enable, set together with CSR7<16> enables CSR5<2>.
1	TSE	Transmit Stop Enable, set together with CSR7<15> enables CSR5<1>.
0	TIE	Transmit Interrupt Enable, set together with CSR7<16> enables CSR5<0>.

5.2.8 MISSED FRAME COUNTER (CSR8)
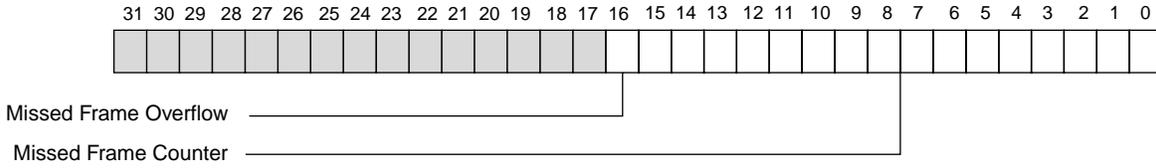
Field	Name	Description
16	MFO	Missed Frame Overflow, set when missed frame counter overflows, reset when CSR8 is read.
15:0	MFC	Missed Frame Counter, indicates the number of frames discarded because no host receive descriptors were available.

5.2.9 NONVOLATILE MEMORY CONTROL REGISTER (CSR9)

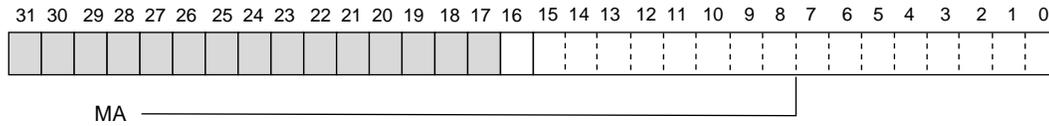| Field	Name	Description
31	LED3SEL	0:Default value. Set LED3 as RX LED.
		1:Set LED3 as F/H duplex LED.
30	LED2SEL	0: Default value. Set LED2 as SPEED LED.
		1: Set LED2 as Collision LED
29	LED1SEL	0:Default value. Set LED1 as Good Link LED.
		1: Set LED1 as Link/Activity LED.
28	LED0SEL	0:Default value. Set LED0 as Activity LED.
		1: Set LED0 as Link Speed (10/100) LED.
24	LED4SEL	0: Default value. Set LED4 as Collision LED.
		1: Set LED4 as PMEB LED.

Field	Name	Description			
26:25	WKFACT	Wake up frame catenation option bits.			
		CRS21<4>	CSR<26>	CSR<25>	Wake up event
		0	X	X	CH0+CH1+CH2+CH3
		1	0	0	(CH0*CH1)+(CH2*CH3)
		1	0	1	(CH0*CH1)+CH2+CH3
		1	1	0	(CH0*CH1*CH2)+CH3
		1	1	1	CH0*CH1*CH2*CH3
14	RD	Boot ROM/EEPROM read operation select bit			
13	WR	EEPROM reload operation select bit.			
		Operation definition:			
		RD	WR		Operation
		1	0		Boot ROM/EEPROM Read
		0	1		Boot ROM/EEPROM write
		1	1		EEPROM reload operation (bit 11, SR=1)
12	BR	Boot ROM Select, set to select boot ROM only if CSR9<11>=0.			
11	SR	Serial ROM Select, set to select serial ROM for either read or write operation.			
7:0	Data	If boot ROM is selected (CSR9<12> is set), this field contains the data to be read from and written to the boot ROM. If serial ROM is selected , CSR9<3:0> are defined as follows :			
3	SDO	Serial ROM data out from serial ROM into MX98L715BEC.			
2	SDI	Serial ROM data input to serial ROM from MX98L715BEC.			
1	SCLK	Serial clock output to serial ROM.			
0	SCS	Chip select output to serial ROM.			

Notice : CSR9<11> and CSR9<12> should be mutually exclusive for correct operations.
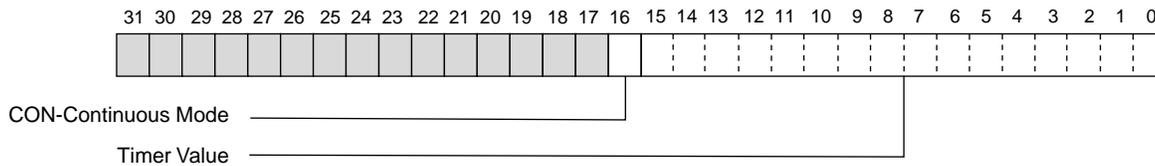
LED DISPLAY Option Summary Table

	0	1
LED0SEL	ACT	SPEED
LED1SEL	LINK	LINK/ACT
LED2SEL	SPEED	COL
LED3SEL	RX	FULL/HALF
LED4SEL*	COL	PMEB

5.2.10 FLASH MEMORY PROGRAMMING ADDRESS REGISTER (CSR10)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MA

Field	Name	Description
16:0	MA	Flash Memory Address : Address bit 16 to 0.

GENERAL PURPOSE TIMER (CSR11)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

CON-Continuous Mode

Timer Value

Field	Name	Description
16	CON	When set, the general purpose timer is in continuous operating mode. When reset, the timer is in one-shot mode.
15:0	Timer	Value contains the timer value in a cycle time of 204.8us.

5.2.11 10 BASE-T STATUS Port (CSR12)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

LPC-Link Partner's Link Code Word
LPN-Link Partner Negotiable
ANS-Autonegotiation Arbitration State
TRF-Transmit Remote Fault
APS-Autopolarity State
LS10B-Link Status of 10 Base-T
LS100B-Link Status of 100 Base-TX
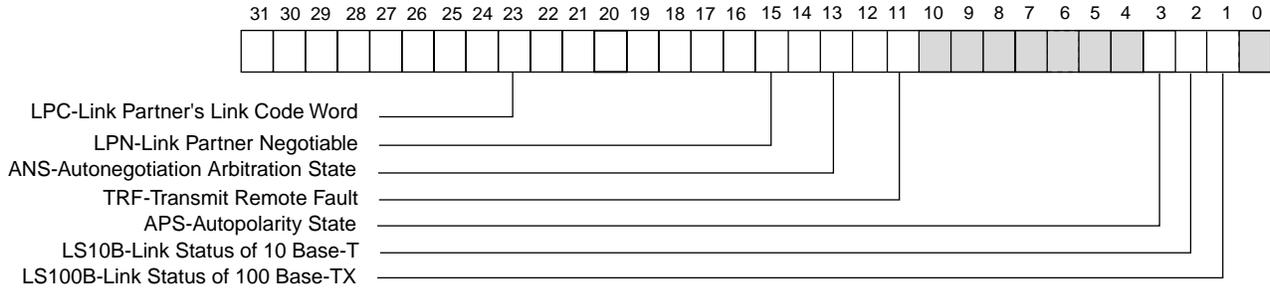
*Software reset has no effect on this register

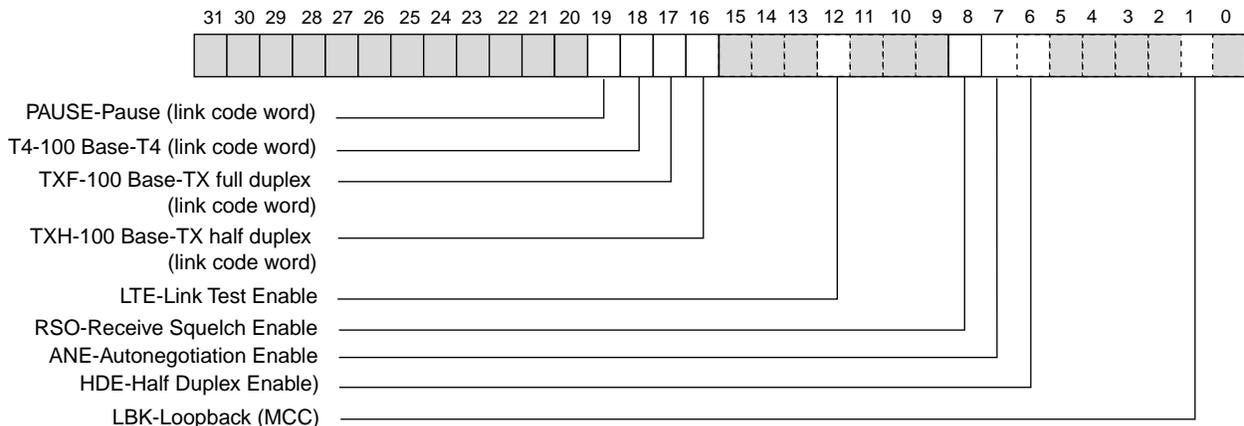| Field	Name	Description
31:16	LPC	Link Partner's Link Code Word, where bit 16 is S0 (selector field bit 0) and bit31 is NP (Next Page). Effective only when CSR12<15> is read as a logical 1.
15	LPN	Link Partner Negotiable, set when link partner support NWAY algorithm and CSR14<7> is set.
14:12	ANS	Autonegotiation Arbitration State, arbitration states are defined 000 = Autonegotiation disable 001 = Transmit disable 010 = ability detect 011 = Acknowledge detect 100 = Complete acknowledge detect 101 = FLP link good; autonegotiation complete 110 = Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated, write 001 into this field can restart the autonegotiation sequence if CSR14<7> is set. Otherwise, these bits should be 0.
11	TRF	Transmit Remote Fault
3	APS	Autopolarity State, set when polarity is positive. When reset, the 10 Base-T polarity is negative. The received bit stream is inverted by the receiver.
2	LS10B	Set when link status of 10 Base-T port link test fail. Reset when 10 Base-T link test is in pass state.
1	LS100B	Link state of 100 Base-TX, this bit reflects the state of SD pin, effective only when CSR6<23>= 1 (PCS is set). Set to indicate a fail condition .i.e. SD=0.

5.2.12 VLAN & HomeLAN Register (CSR13)
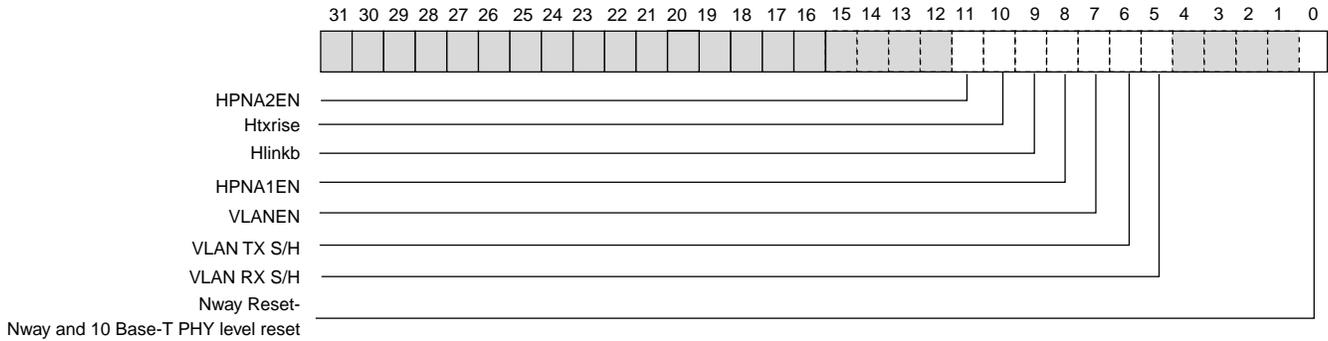
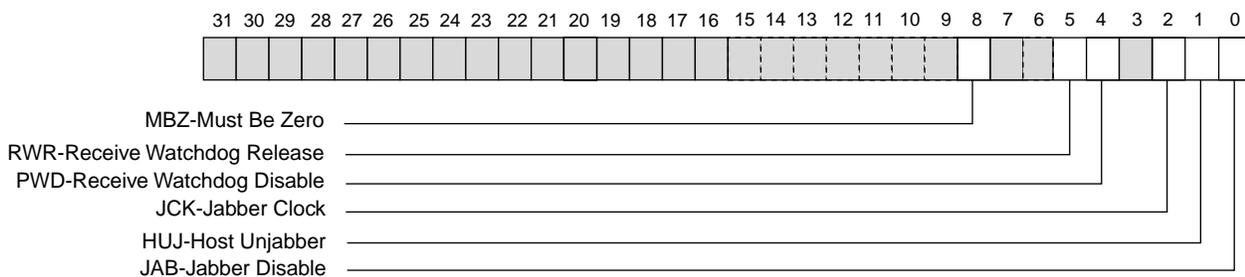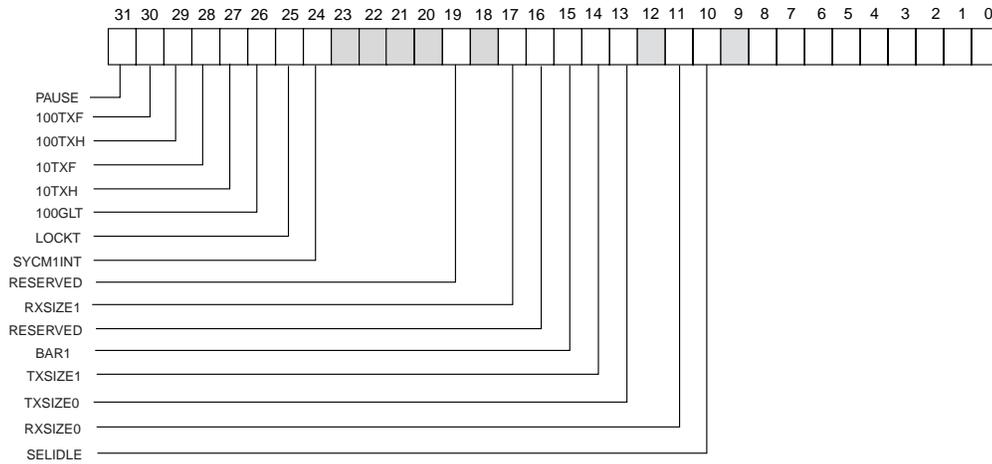| Field	Name	Description
11	HPNA2EN	Home PNA 2.0 MII Interface Enable, default=0
10	Htxrise	Reset to send signal in rising edge, set to send signal in falling edge, default=0.
9	Hlinkb	Home PNA Link status, low is good link, high is bad link, default=0.
8	HPNA1EN	Home PNA 1.0 7-wire interface enable, default=0
7	VLANEN	Set to enable VLAN function, reset to disable VLAN function, default=0.
6	VLAN TX S/H	While VLANEN=1, reset this bit for software VLAN TX function, set this bit for hardware VLAN TX function, default=0.
5	VLAN RX S/H	While VLANEN=1, reset this bit for software VLAN RX function, set this bit for hardware VLAN RX function, default=0.
0	Nway Reset	While writing 0 to this bit, resets the CSR12 & CSR14, default=0.

5.2.13 10 Base-T Control PORT (CSR14)

*The software reset bit (bit0 of CSR0) has no effect to this register.

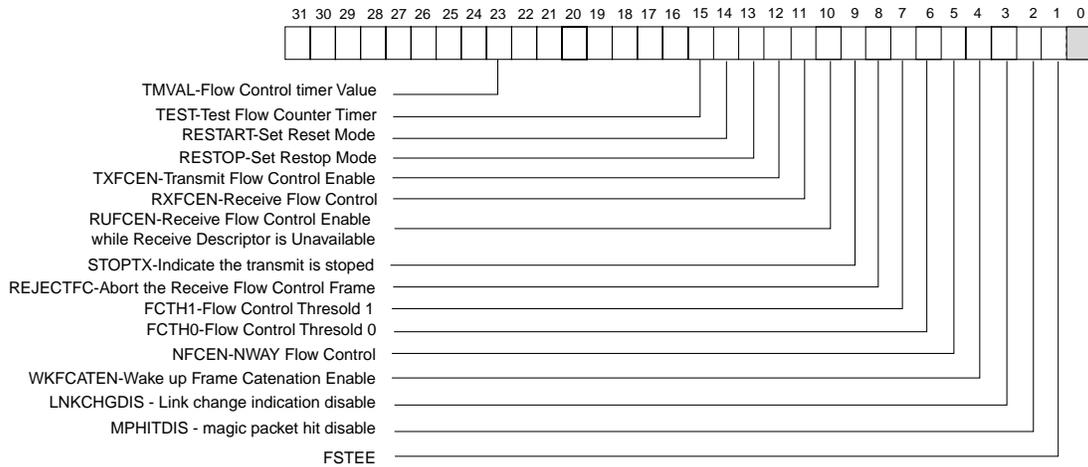| Field	Name	Description
19	PAUSE	Bit 10 of link code word for 100 Base-TX pause mode.
18	T4	Bit 9 of link code word for T4 mode. (allways 0 after reset)
17	TXF	Bit 8 of link code word for 100 Base-TX full duplex mode.
16	TXH	Bit 7 of link code word for 100 Base-TX half duplex mode. Meaningful only when CSR14<7> (ANE) is set.
12	LTE	Link Test Enable, when set the 10 Base-T port link test function is enabled.
8	RSQ	Receive Squelch Enable for 10 Base-T port. Set to enable.
7	ANE	Autonegotiation Enable, .
6	HDE	Half-Duplex Enable, this is the bit 5 of link code word, only meaningful when CSR14<7> is set.
1	LBK	Loop back enable for 10 Base-T MCC.

5.2.14 WATCHDOG TIMER (CSR15)

Field	Name	Description
8	FJT	Internal test for jabber timer. Must be zero. Default = 0
5	RWR	Defines the time interval no carrier from receive watchdog expiration until re-enabling the receive channel. When set, the receive watchdog is release 40-48 bit times from the last carrier desertion. When reset, the receive watchdog is released 16 to 24 bit times from the last carrier desertion.
4	RWD	When set, the receive watchdog counter is disable. When reset, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog counter to time out. Packets shorter than 2048 bytes are guaranteed to pass.
2	JCK	When set, transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted, When reset, transmission for the 10 Base-T port is cut off after a range of 26 ms to 33ms. When reset, transmission for the 100 Base-TX port is cut off after a range of 2.6ms to 3.3ms.
1	HUJ	Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the jabber is released 365ms to 420 ms after jabber expiration for 10 Base-T port. When reset, the jabber is released 36.5ms to 42ms after the jabber exploration for 100 Base-TX port.
0	JBD	Jabber Disable, set to disable transmit jabber function.

5.2.15 NWAY Status Internal test Register (CSR20)

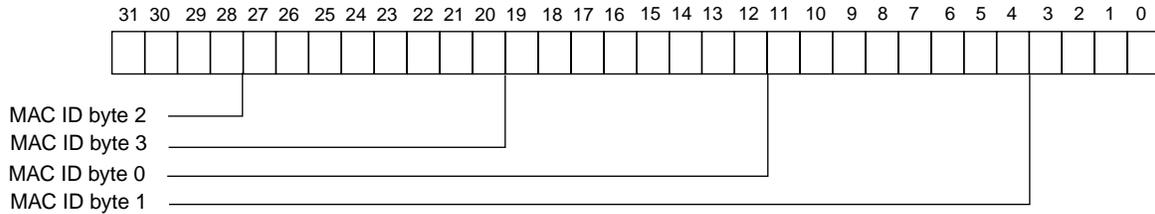| Field	Name	Description
31	PAUSE	Flow Control PAUSE mode is accepted, read only.
30	100TXF	100 base-T full duplex mode selection indication : After NWAY autonegotiation , a 1 in this bit indicate the IC has settled down in this mode. Otherwise 0.
29	100TXH	100 base-T half duplex mode selection indication : After NWAY autonegotiation , a 1 in this bit indicate the IC has settled down in this mode. Otherwise 0.
28	10TXF	10 base-T full duplex mode selection indication : After NWAY autonegotiation , a 1 in this bit indicate the IC has settled down in this mode. Otherwise 0.
27	10TXH	10 base-T half duplex mode selection indication : After NWAY autonegotiation , a 1 in this bit indicate the IC has settled down in this mode. Otherwise 0.
26	100GLT	100 TX NWAY good link test speed option, set for fast, reset for normal.
25	LOCKT	Descrambler lock speed test, set for fast, reset for normal
24	SYNM1INT	Sync. modem function 1 Interrupt
19	RESERVED	Fixed to 1 by chip
17	RXSIZE1	Must be 0 for normal operation
16	RESERVED	Default is 0.
15	BAR1	RX FIFO arbitration option control bit 1, together with CSR0<1> BAR0 define a internal RX almost full threshold, definition as followed BAR0　　BAR1　　RX Near full threshold 0　　　　0　　　　1K bytes 0　　　　1　　　　256 1　　　　0　　　　512 1　　　　1　　　　128 Device driver can determine these values to reduce over-flow error rate, option 00 is least likely to have overflow but would reduce TX performance, while option 11 is near round-robin type of arbitration
14	TXSIZE1	Must be zero for normal operation
13	TXSIZE0	Must be zero for normal operation
11	RXSIZE0	Must be zero for normal operation
10	SELIDLE	Set for 200-250 ns idle pulse width detection, reset for 175-225 ns idle pulse detection Default is 0.
8:0	RBCNT	RX DMA Byte Count for driver's early interrupt assertion control

5.2.16 Flow Control Register (CSR21)

Bit field diagram showing bits 31 down to 0 with the following labels:
- TMVAL-Flow Control timer Value
- TEST-Test Flow Counter Timer
- RESTART-Set Reset Mode
- RESTOP-Set Restop Mode
- TXFCEN-Transmit Flow Control Enable
- RXFCEN-Receive Flow Control
- RUFCEN-Receive Flow Control Enable while Receive Descriptor is Unavailable
- STOPTX-Indicate the transmit is stoped
- REJECTFC-Abort the Receive Flow Control Frame
- FCTH1-Flow Control Thresold 1
- FCTH0-Flow Control Thresold 0
- NFCEN-NWAY Flow Control
- WKFCATEN-Wake up Frame Catenation Enable
- LNKCHGDIS - Link change indication disable
- MPHITDIS - magic packet hit disable
- FSTEE

Field	Name	Description
31:16	TMVAL	Timer value in the flow control frame for receive flow control.
15	TEST	Test the flow control timer.
14	RESTART	Set the receive flow control into the restart mode, the RXFCEN should be asserted. The default value is 0.
13	RESTOP	Set the receive flow control into the restop mode, the RXFCEN should be asserted. The default value is 0.
12	TXFCEN	Transmit flow control enable. The default value is 1.
11	RXFCEN	Receive flow control enable. The default value is 0.
10	RUFCEN	Send flow control frame control when the receive descriptor is unavailable, the RXFCEN should be asserted. The default value is 0.
9	STOPTX	Indicate the transmit status. If the receive flow control stop the transmission, this bit is set. After recovering transmission, this bit is clear.
8	REJECTFC	Abort the receive flow control frame when set. The default value is 1.
7	RXFCTH1	Receive flow control threshold 1. Default = 0
6	RXFCTH0	Receive flow control threshold 0. Default = 1
5	NFCEN	Accept flow control from the auto-negotiation result. Default = 1
4	WKFCATEN	Enable the wake up frame concatenation feature. loadable from EEPROM offset 77h bit 3, See CSR9 for details
3	LNKCHGDIS	Set to disable link change detection in power down mode, loadable from EEPROM offset 77h bit 1
2	MPHITDIS	Set to disable magic packet address matching, loadable from EEPROM offset 77h bit 0
1	FSTEE	Set to speed up EEPROM clk for test, reset for normal EEPROM clock.

Receive Flow Control Threshold Table

FCTH1	1	1	0	0
FCTH0	1	0	1	0
Threshold Value (Byte)	512	256	128	overflow

5.2.17 MAC ID Byte 3-0 Register (CSR22)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

MAC ID byte 2
MAC ID byte 3
MAC ID byte 0
MAC ID byte 1

5.2.18 Magic ID Byte 5,4/ MAC ID Byte 5,4 (CSR23)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Magic ID byte 4
Magic ID byte 5
MAC ID byte 4
MAC ID byte 5
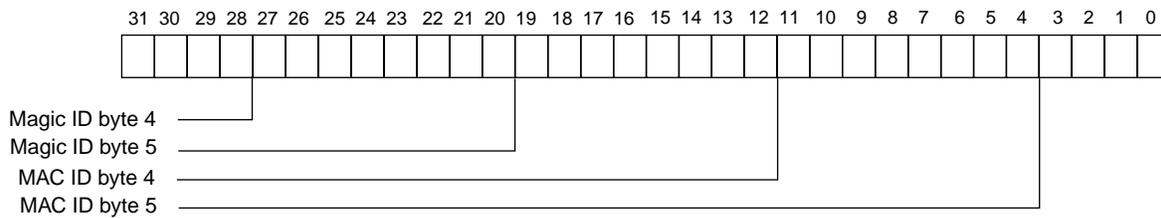
5.2.19 Magic ID Byte 3-0 (CSR24)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Magic ID byte 2
Magic ID byte 3
Magic ID byte 0
Magic ID byte 1
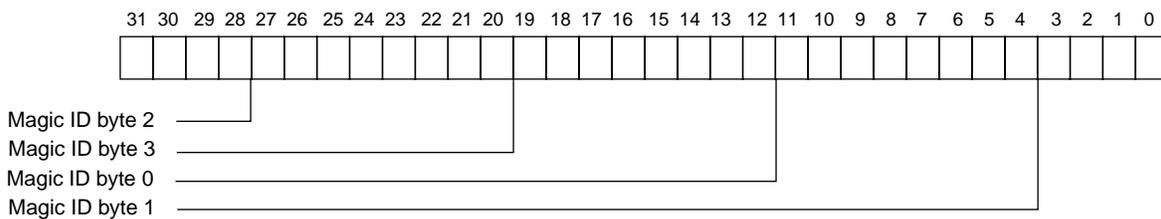
5.2.20 Filter 0 Byte Mask Register 0 (CSR25)
Filter 1 Byte Mask Register 1 (CSR26)
Filter 2 Byte Mask Register 2 (CSR27)
Filter 3 Byte Mask Register 3 (CSR28)

CSR25 to CSR28 are Filter N (N=0 to 3) Byte Mask Register N (N=0 to 3)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```
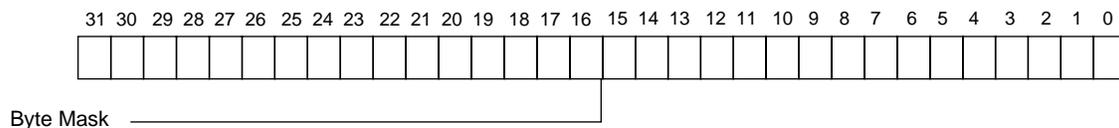
Byte Mask

Field	Name	Description
31:0	Byte Mask	If bit number j of the byte mask is set, byte number (offset+j) of the incoming frame is checked.

5.2.21 Filter Offset Register (CSR29)
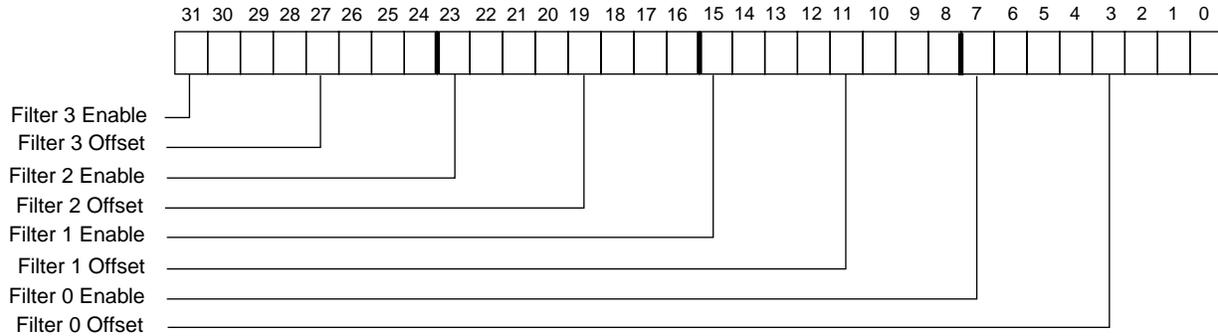
Field	Name	Description
6:0	Pattern 0 Offset	The offset defines the location of first byte that should be checked by filter 0 in the frame. Offset is always greater than 12.
7	Filter 0 Enable	This bit is set to enable the filter 0. If it is reset, filter 0 is disabled for the wake-up frame checking.
14:8	Pattern 1 Offset	The offset defines the location of first byte that should be checked by filter 1 in the frame. Offset is always greater than 12.
15	Filter 1 Enable	This bit is set to enable the filter 1. If it is reset, filter 1 is disabled for the wake-up frame checking.
22:16	Pattern 2 Offset	The offset defines the location of first byte that should be checked by Filter 2 in the frame. Offset is always greater than 12.
23	Filter 2 Enable	This bit is set to enable the filter 2. If it is reset, filter 2 is disabled for the wake-up frame checking.
30:24	Pattern 3 Offset	The offset defines the location of first byte that should be checked by Filter 3 in the frame. Offset is always greater than 12.
31	Filter 3 Enable	This bit is set to enable the filter 3. If it is reset, filter 3 is disabled for the wake-up frame checking.

5.2.22 Filter 1 and 0 CRC-16 Register (CSR30)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Filter 1 CRC-16
Filter 0 CRC-16
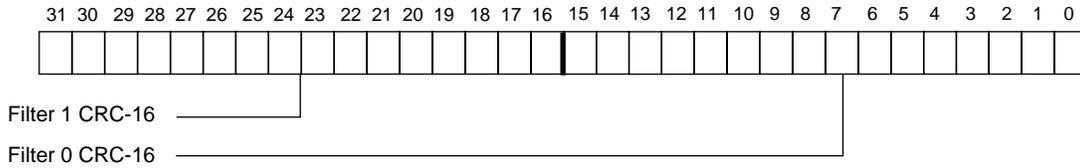
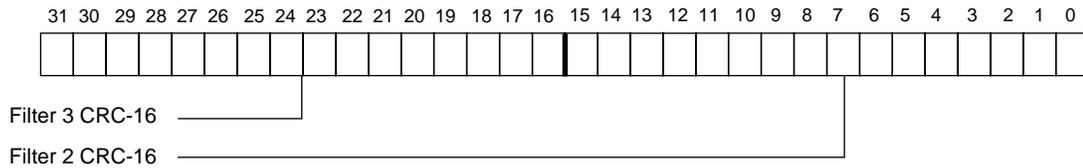| Field	Name	Description
15:0	Filter 0 CRC-16	The 16-bit CRC value is programmed by the driver to be matched against the current result from the CRC-16's remainder at the location specified by Filter 0 offset and Filter 0 Byte Mask register. if matched, the incoming frame is a wakeup frame.
31:0	Filter 1 CRC-16	Same description as Filter 0 CRC-16.

5.2.23 Filter 3 and 2 CRC-16 Register (CSR31)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Filter 3 CRC-16
Filter 2 CRC-16

Field	Name	Description
15:0	Filter 2 CRC-16	Same description as Filter 0 CRC-16.
31:0	Filter 3 CRC-16	Same description as Filter 0 CRC-16

5.2.24 PMDCTRL 1 Register (CSR32)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
 0  1  0  0  0  0  1  1  0  1  1                             0  0  1  1  0  1  0  1  0  0
```

FULLSCAL15M
FULLSCAL16M
FULLSCAL17M
PMDB40[1:0]M
PMDB60[1:0]M
PMDB100[1:0]M
PMDB120[1:0]M
PMDGS3[2:0]
PMDGS2[2:0]
PMDGS1[2:0]
PMDB2[1:0]
PMDGS4[2:0]
PMDB3[2:1]
PMDB5[2:0]
PMDPZ[1:0]
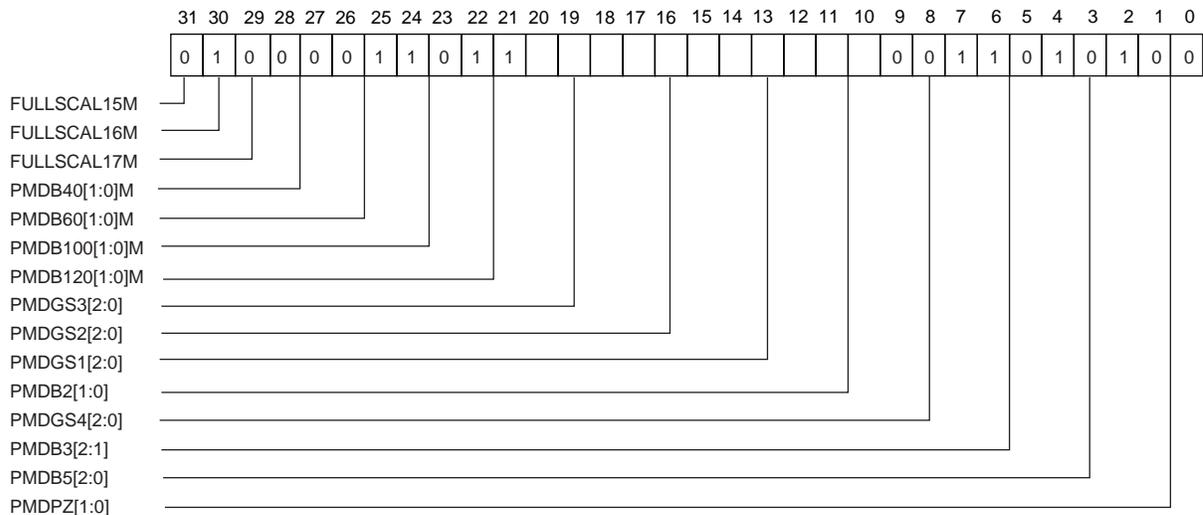
Field	Description
1:0	PMDPZ[1:0] : Pole/Zero programming bit. R/W Default=00
4:2	PMDB5[2:0] : Reference programming bits. Use PMDB5[2:0} to reference if AUTOCALB=1 Use PMDB4[2:0] to set reference if AUTOCALB=0 Default=101 R/W
6:5	PMDB3[2:1] : Reference offset setting bits. Default=10. R/W
9:7	PMDGS4[2:0] : EQ transfer curve set. Use PMDGS4[2:0] to set EQ transfer curve if AUTOCALB=1 Use PMDGS3[2:0] to set EQ transfer curve id AUTOCALB=0 Default=001 R/W
11:10	PMDB2[1:0] : PMD calibration output for reference, RO.
14:12	PMDGS1[2:0] : PMD calibration output for reference, RO.
17:15	PMDGS2[2:0] : PMD calibration output ofr reference, RO.
20:18	PMDGS3[2:0} : The modified output of PMDGS2[2:0] according to EQ gain, RO.
22:21	PMDB120[1:0]M : default=11, R/W.
24:23	PMDB100[1:0]M : default=10, R/W.
26:25	PMDB60[1:0]M : default=01, R/W.
28:27	PMDB40[1:0]M : default=00, R/W.
29	FULLSCAL17M : default=0, R/W.
30	FULLSCAL16M : default=1, R/W.
31	FULLSCAL15M : default=0, R/W.

5.2.25 PMDCTRL 2 Register (CSR33)

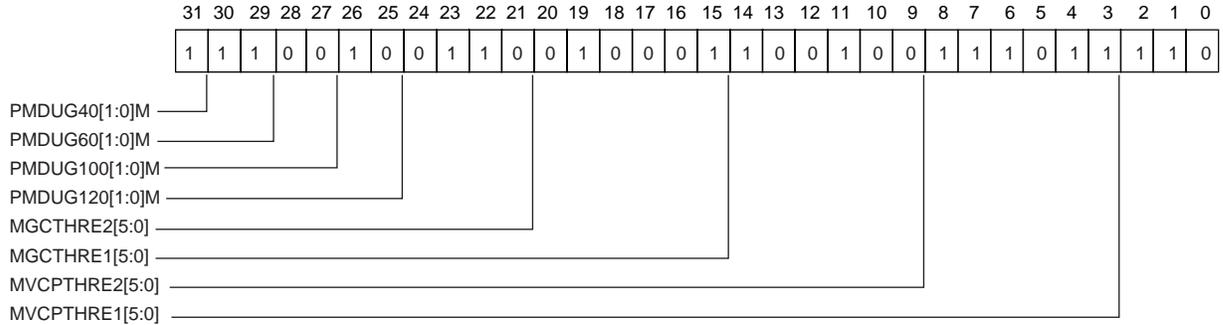| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	1	1	0	1	0	1	1	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0

PMDUG40[1:0]M
PMDUG60[1:0]M
PMDUG100[1:0]M
PMDUG120[1:0]M
MLDTHRE3[5:0]
MLDTHRE2[5:0]
MLDTHRE1[5:0]
MLENGTH[5:0]
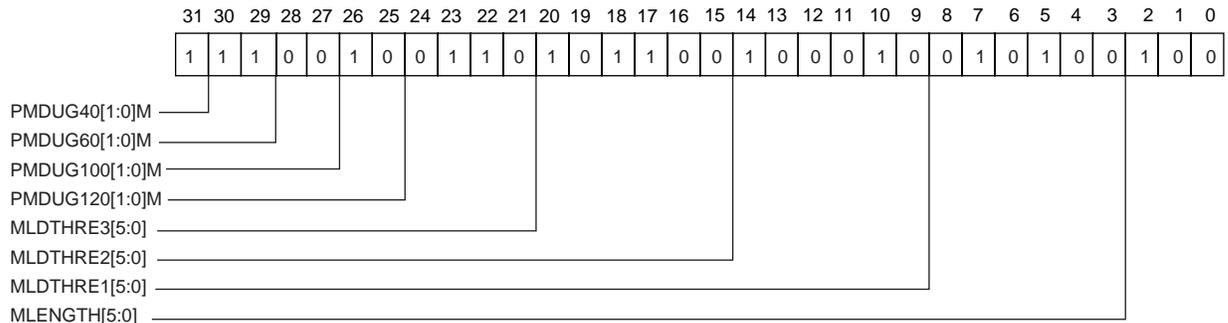
Field	Description
5:0	MLENGTH[5:0] : Length detection result. RO. Latch the data from SPPM[5:0] bus by LDREADM positive edge.
11:6	LDTHRE1[5:0] : Threshold used to dertermine length range. Loaded from EEPROM. R/W Default=010010
17:12	LDTHRE2[5:0] : Threshold used to dertermine length range. Loaded from EEPROM. R/W Default=100100
23:18	LDTHRE3[5:0] : Threshold used to dertermine length range. Loaded from EEPROM. R/W Default=110101
25:24	PMDUG120[1:0]M : default=00, R/W.
27:26	PMDUG100[1:0]M : default=01, R/W.
29:28	PMDUG60[1:0]M : default=10, R/W.
31:30	PMDUG40[1:0]M : default=11, R/W.

5.2.26 PMDCTRL 3 Register (CSR34)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1	1	1	0	1	1	1	1	0

PMDUG40[1:0]M
PMDUG60[1:0]M
PMDUG100[1:0]M
PMDUG120[1:0]M
MGCTHRE2[5:0]
MGCTHRE1[5:0]
MVCPTHRE2[5:0]
MVCPTHRE1[5:0]

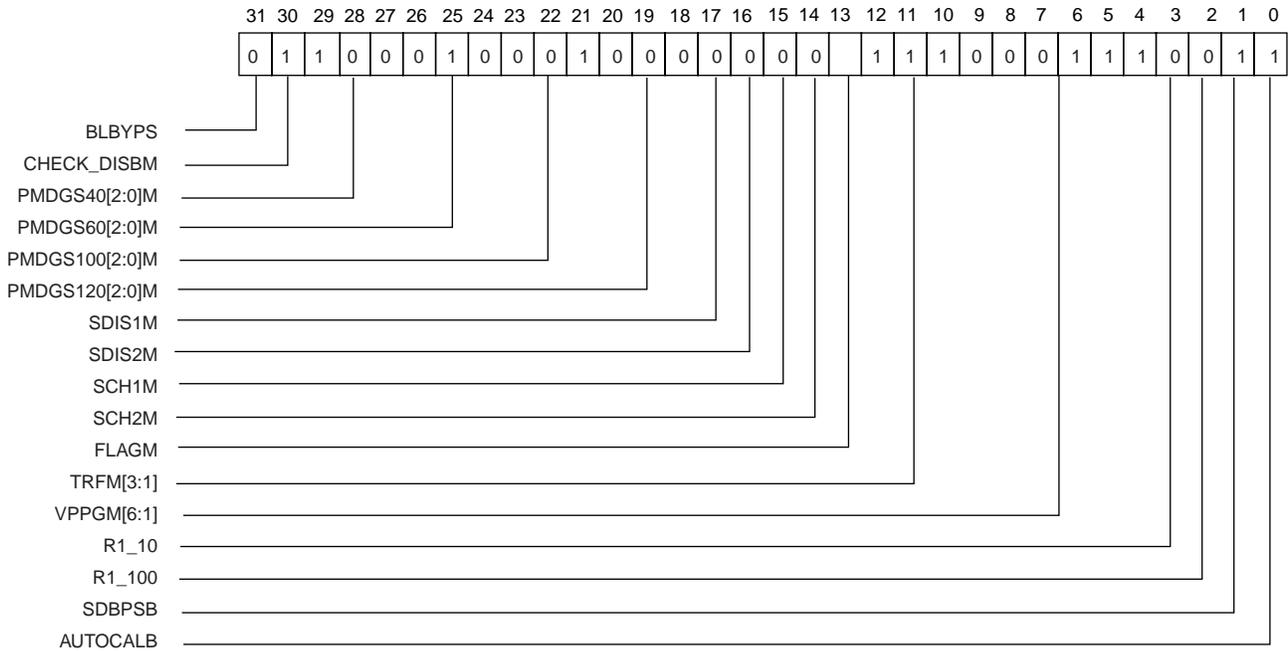| Field	Description
5:0	MVCPTHRE1[5:0] : Threshold used to identify process coner. Loaded from EEPROM. R/W Default=011110
11:6	MVCPTHRE2[5:0] : Threshold used to identify process coner. Loaded from EEPROM. R/W Default=100111
17:12	MGCTHRE1[5:0] : Threshold used to identify EQ gain. Loaded from EEPROM. R/W Default=011110
23:18	MGCTHRE2[5:0] : Threshold used to identify EQ gain. Loaded from EEPROM. R/W Default=110010
25:24	PMDIR120[1:0]M : default=00, R/W.
27:26	PMDIR100[1:0]M : default=01, R/W.
29:28	PMDIR60[1:0]M : default=10, R/W.
31:30	PMDIR40[1:0]M : default=11, R/W.

5.2.27 PMDCTRL 4 Register (CSR35)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	1																											

UGDFT[1:0]M
TDFT[1:0]M
PMDB[2:0]P
PMDGS[2:0]
PMDBP2:0]
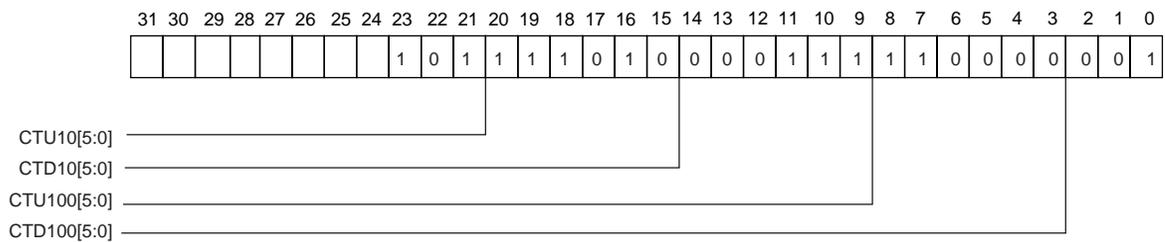MGAINCAL[5:0]
MNORMAL[5:0]
MPLLVCP[5:0]
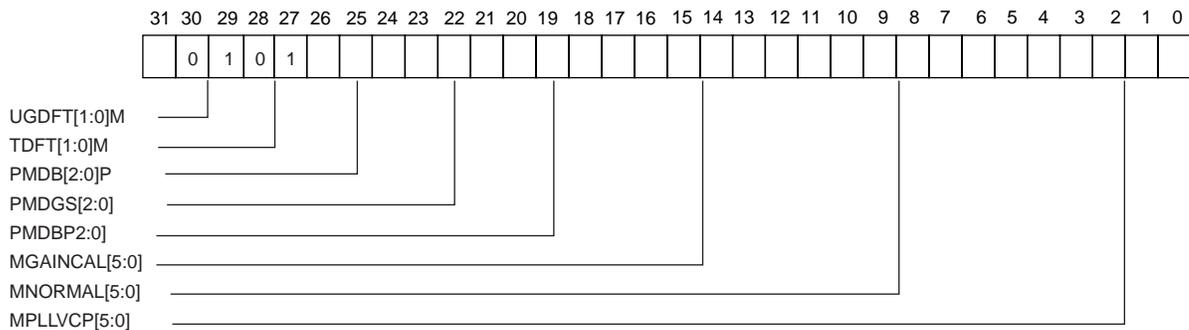
Field	Description
5:0	MVPLLVCP[5:0] : PLLVCP result. which can be used to identify process corner. RO. Latch the data from SPPM[5:0] bus by PLLVCPREADM positive edge.
11:6	MNORMAL[5:0] : EQ gain at normal operation. RO. Latch the data from MEQGAIN[6:1] bus by NORMALREADM positive edge.
17:12	MGAINCAL[5:0] : EQ gain calibration output. RO. Latch the data from MEQGAIN[6:1] bus by CALREADM positive edge.
20:18	PMDB[2:0] : PMD calibration output for reference. RO.
23:21	PDGS[2:0] : PMD calibration output for refernce. RO.
26:24	PMDB[2:0]P : RO.
28:27	TDFT[1:0]M : default=01, R/W.
30:29	UGDFT[1:0]M : default=01, R/W.

5.2.28 PMDCTRL 5 Register (CSR36)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0		1	1	1	0	0	0	1	1	1	0	0	1	1

BLBYPS
CHECK_DISBM
PMDGS40[2:0]M
PMDGS60[2:0]M
PMDGS100[2:0]M
PMDGS120[2:0]M
SDIS1M
SDIS2M
SCH1M
SCH2M
FLAGM
TRFM[3:1]
VPPGM[6:1]
R1_10
R1_100
SDBPSB
AUTOCALB

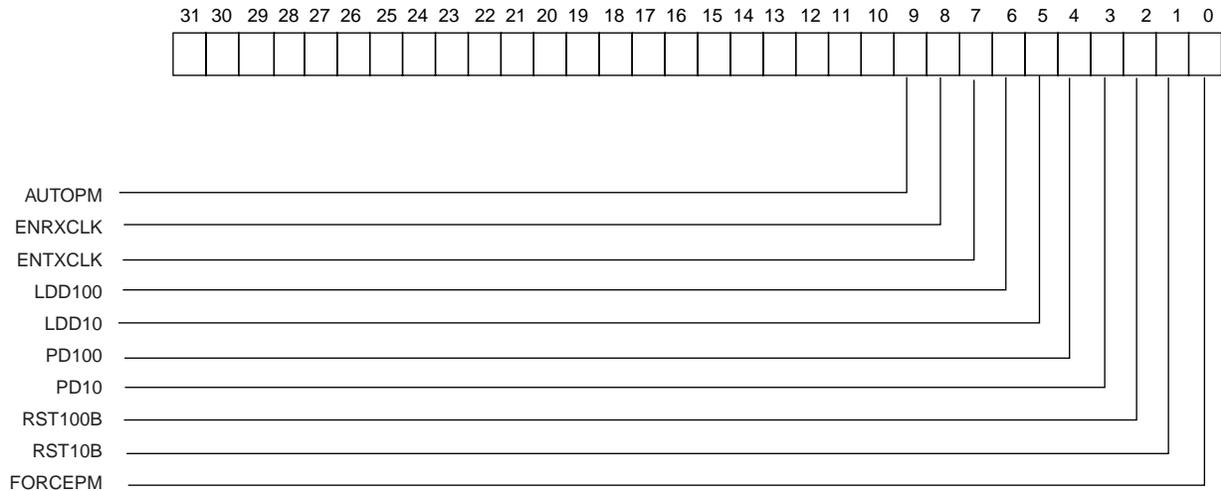| Field	Description
0	AUTOCALB : If AUTOCALB=0, PMDGS[2:0] and PMDB[2:0] are determined automatically.
	If AUTOCALB=1, PMDGS[2:0] and PMDB[2:0] are determined by driver. R/W. Default=1
1	SDBPSB : If SDBPSB=0, bypass signal detection. R/W. Default=1.
2	R1_100 : 100BT loop filter option. R/W. Default=0
3	R1_10 : 10BT loop filter option. R/W. Default=0
9:4	VPPGM[6:1] : AOI programming bits. R/W. Default=000111.
12:10	TRFM[3:1] : AOI programming bits. R/W. Default=111.
13	FLAGM : PHY output for reference, RO.
14	SCH2M : PMD programing bit. R/W. Default=0
15	SCH1M : PMD programing bit. R/W. Default=0
16	SDIS2M : PMD programing bit. R/W. Default=0
17	SDIS1M : PMD programing bit. R/W. Default=0
20:18	PMDGS120[2:0]M : default=000, R/W.
23:21	PMDGS100[2:0]M : default=001, R/W.
26:24	PMDGS60[2:0]M : default=010, R/W.
29:27	PMDGS40[2:0]M : default=100, R/W.
30	CHECK_DISBM : default=1, R/W.
31	BLBYPS:default=0, R/W

5.2.29 PLLCTRL 5 Register (CSR37)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1

CTU10[5:0]
CTD10[5:0]
CTU100[5:0]
CTD100[5:0]

Field	Description
5:0	CTD100[5:0] : 100BT RXDLL down counter threshold. R/W. Default=000001.
11:6	CTD100[5:0] : 100BT RXDLL up counter threshold. R/W. Default=111110.
17:12	CTD10[5:0] : 10BT RXDLL down counter threshold. R/W. Default=010000.
23:18	CTD10[5:0] : 10BT RXDLL up counter threshold. R/W. Default=101111.

5.2.30 VLan Tag Register (CSR38)
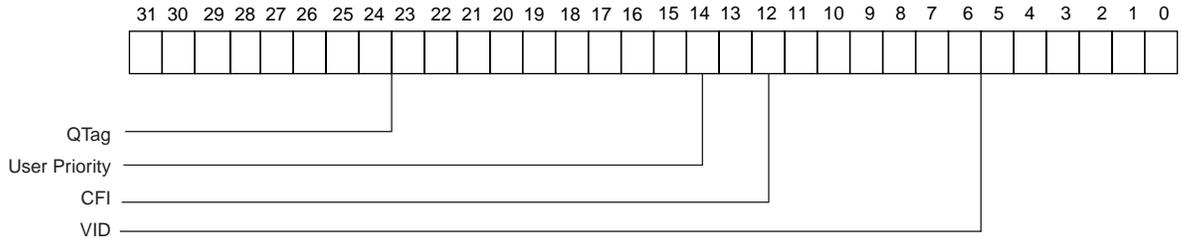
Field	Name	Description
31:16	QTag	802.1Q QTag header which is used in insertion of VLan Tag in TX packet, default value is 8100h.
15:13	Priority	Q0S Priority bit, 000 to 111
12	CFI	Counonical format Indicator, default=0
11:0	VID	VLan ID, default value is 0h.

5.2.31 Power Management Register (CSR39)

Field	Name	Description
0	FORCEPM	Default is 0 after host hardware reset, which means NWAY autonegotiation is enabled. Set this bit to 1 will enable manual controls (bit 8 :1) over chip power saving features.
1	RST10B	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 and write 0 followed by write 1 to RST10B will reset 10 base-T analog module.
2	RST100B	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 and write 0 followed by write 1 to RST100B will reset 100 base-TX analog module.
3	PD10	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 and write 1 to PD10 will power down 10 base-T analog module's core except the 10 base-T line drivers.
4	PD100	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 and write 1 to PD100 will power down 100 base-TX analog module's core except the 100 base-TX line drivers.
5	LDD10	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 and write 1 to LDD10 will power down 10 base-TX analog module's line drivers.
6	LDD100	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 then write 1 in LD100 will power down 100 base-TX analog module's line drivers.
7	ENTXCLK	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 then write 0 in ENTXCLK will stop TXC 25/2.5 MHz clock in the MAC core.
8	ENRXCLK	Default is 0 after host hardware reset, this bit is meaningful only if bit 0 (FORCEPM) is set to 1. When FORCEPM=1 then write 0 in ENRXCLK will stop RXC 25/2.5 MHz clock in the MAC core.
9	AUTOPM	Default is 0 after host hardware reset, which means NWAY autonegotiation is enabled. Set this bit high will enable automatic power saving mode which depends on the status of PCI configuration's D0 - D3cold bits and will result in different level of power saving.

5.3 ACPI Power Management Support

The Advanced Configuration and Power Interface (ACPI) Specification defines a flexible and abstract hardware interface for a wide variety of PC systems to implement power and thermal management functions. This chip is fully compliant with the OnNow Network Device Class Power Management spec. rev.1.0, the PCI power management interface spec. rev.1.1 and the ACPI spec. rev.1.1.

Four power states defined for a PCI function are:
* D0-Fully On.
    The device is completely active and responsive.
* D1-Light Sleep.
    Save a little power than D0 state. The PCI clock is running.
* D2-Deeper Sleep:
    Save more power than D1 state. The PCI clock can be stopped.
* D3$_{hot}$-Deepest Sleep:
    Save more power than D2 state. The PCI clock is stopped.
* D3$_{cold}$-Power Down:
    In this state, the main system power is removed from the chip but will preserve their PME context when transition from the D3$_{cold}$ to the D0 state. Such function requires an auxiliary power source other than main system power plane.

This chip also supports the OnNow Network Device Class Specification based on the ACPI specification defines the power management requirements of a network device. It defines the following wake-up events:

* Reception of a Magic Packet.
* Reception of a Network wake-up frame.
* Detection of change in the network link state.

To put MX98L715BEC into the sleep mode and enable the wake-up events detection are done as following:

1. Write 1 to PPMCSR[8] to enable power management feature.
2. Write the value to PPMCSR[1:0] to determine which power state to enter.

If D1, D2 or D3$_{hot}$ state is set, the PC is still turned on and is commonly called entering the Remote Wake-up mode. Otherwise if the main power on a PC is totally shut off, we call that it is in the D3$_{cold}$ state or Remote Power-On mode. To sustain the operation of the LAN card, a 3.3V standby power is required. Once the PC is turned on, MX98L715BEC loads the Magic ID from EEPROM and set it up automatically. No registers is needed to be programmed. After then, simply turn of PC to enter D3$_{cold}$ state. In either Remote Wake-up mode or Remote Power-On mode. The transceiver and the RX block are still alive to monitor the network activity. If one of the three wake-up events occurred, the following status is changed:

1. PPMCSR[15] (PME status) is set to 1.
2. CRS5[28] (WKUPI) is set to 1.
3. PCI interrupt pin INTA# is asserted low.
4. PMEB pin is asserted low.
5. In MX98L715BEC, LANWAKE are also asserted.

5.3.1 Magic Packet

The Magic Packet$^{(TM)}$ technology, proposed by AMD, is used to remotely wake up a sleeping or powered off PC on a network. This is accomplished by sending a specific packet, called Magic Packet, to a node on the network. When a NIC capable of recognizing the specific frame goes to sleep (entering D1, D2 or D3 state), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh. For example, if the IEEE address for a particular node on the network was 11h 22h 33h 44h 55h 66h, then the Magic Packet for this node would be:

DA SA MISC. FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 MISC. CRC.

This chip can automatically loads the IEEE address into the internal registers from EEPROM while booting up. the magic packet detection scheme is not active while chip is in normal running state (D0). After entering into the sleep mode(D1, D2, D3) by host, the chip begins to scan the incoming packet but does not load the packet into RX FIFO. If a magic packet is detected, the PMEB is asserted to notify the host.

Magic packet event occurs when the following conditions are approved:

    * The destination address of the received packet matches.
    * The PMEN bit (PPMCSR[8]) is set to 1.
    * Not in D0 state.
    * The magic packet pattern matches, i.e., 6*FFh + 16* Destination ID.

<Note>: The CRC value is not checked during magic packet detection.

5.3.2 Wake-up Frames

A network wake-up frame is typically a frame that is sent by existing network protocols, such as ARP requests or IP frames addressed to the machine. Before putting the network adapter into the wake-up state, the system passes to the adapter's driver a list of sample frames and corresponding byte masks. Each sample frame is an example of a frame that should wake up the system. Each byte mask defines which bytes of the incoming frames should be compared with corresponding sample frame in order to determine whether or not to accept the incoming frame as a wake-up event.

The on-chip Wake-up logic provides four programmable filters that allow support of many different receive packet patterns. Specifically, these filters allow support of IP and IPX protocols which currently are the only protocols targeted to be power manageable. Each filter relates to 32 contiguous bytes in the incoming frame.

When a frame is received from the network, the chip examines its content to determine whether the pattern matches to a wake-up frame. To know which byte of the frame should be checked, a programmable byte-mask and a programmable pattern offset are used for each one of the four supported filters. The pattern offset defines the location of the first byte in the frame that should be checked. Beginning with the pattern offset, if bit j in the byte mask is set, byte offset+j in the frame is checked.

The chip implements imperfect pattern matching by calculating a CRC-16 on all bytes of the received frame that where specified by the pattern's offset and the byte mask and comparing to a programmable pre-calculated CRC-16 remainder value. The CRC calculation uses the following polynomial:

$$G(X)=X^{16} + X^{15} + X^2 +1$$

The calculated CRC-16 value is compared with four possible CRC-16 values stored in CSR30 and CSR31. if the result matches any one and the enable bit of the corresponding filter also set, then we call a Wakeup frame received.

Table1 shows the wake-up frame register block. This block is accessed through CSR registers mapping.

Filter 0 Byte Mask				CSR25
Filter 1 Byte Mask				CSR26
Filter 2 Byte Mask				CSR27
Filter 3 Byte Mask				CSR28
Filter 3	Filter 2	Filter 1	Filter 0	CSR29
Filter 1 CRC-16		Filter 0 CRC-16		CSR30
Filter 3 CRC-16		Filter 2 CRC-16		CSR31

The four filters can operate independently to match four 32-byte wake up frames. They also can be programmed to catenate each other to support longer wake up frames, ranging from 32 bytes up to 128 bytes. The following table shows the possible combination.

CSR21.4	CSR9.26	CSR9.25	Wake up event
WKFCATEN	WKFCAT1	WKFCAT0	
0	X	X	CH0+CH1+CH2+CH3
1	0	0	(CH0*CH1)+(CH2*CH3)
1	0	1	(CH0*CH1)+CH2+CH3
1	1	0	(CH0*CH1*CH2)+CH3
1	1	1	CH0*CH1*CH2*CH3

If WAKCATEN (CSR21.4) is not set, the four filters are independent and simultaneous to match the incoming frame. When WKFCATEN is set, the catenation options are determined by WKFCAT<1:0> (CSR<26:25>). For example, if WKFCAT<1:0>=00, wake up event is occurred only if either both of channel 0 and channel 1 match or both of channel 2 and channel 3 match. If the

driver sets filter 0 and filter 1 be contiguous and also sets filter 2 and filter 3 be contiguous by adjusting the offsets, then two 64-byte wake up frames are supported. Another example is that if WKFCAT<1:0>=11 and the driver sets filter 0,1,2,3 as contiguous, a 128-byte wake up frame is supported.

Wakeup Frames event occurs when following conditions are met:

* Not in D0 state.
* The destination address of the received wakeup frame matches.
* No CRC-32 error is detected in the wakeup frame.
* The PMEN bit (PPMCSR[8]) is set to 1.
* The enable bit in the wakeup frame register block must be set.
* The CRC value calculated from the bytes in the pre-designated locations equals to the respectively stored CRC-16 value.
* If catenation must be met. enable bit WKFCATEN is set, the condition in table 2.

5.3.3 Link Change

Link change wakeup event occurs when the following conditions are met:

* Not in D0 state.
* The PMEN bit (PMCSR[8]) is set to 1.
* The cable is reconnected.

The Remote Power-on (RPO) feature is a mechanism can be used to remotely power up a sleeping station. When the PC turned on, MX98L715BEC loads the network ID from serial ROM automatically. Once the PC is turned off, MX98L715BEC enters the RPO mode. MX98L715BEC monitors the network for receipt of a wakeup packet. If a magic packet or wake up frame is received, it asserts LANWAKE, signal to wake up the system. After main power is on, LANWAKE is deserted by PCI RSTB signal. After the desertion, MX98L715BEC can enter RPO mode again if the main power is switched off.

6. AC/DC CHARACTERISTICS

6.1 BOOT ROM READ TIMING
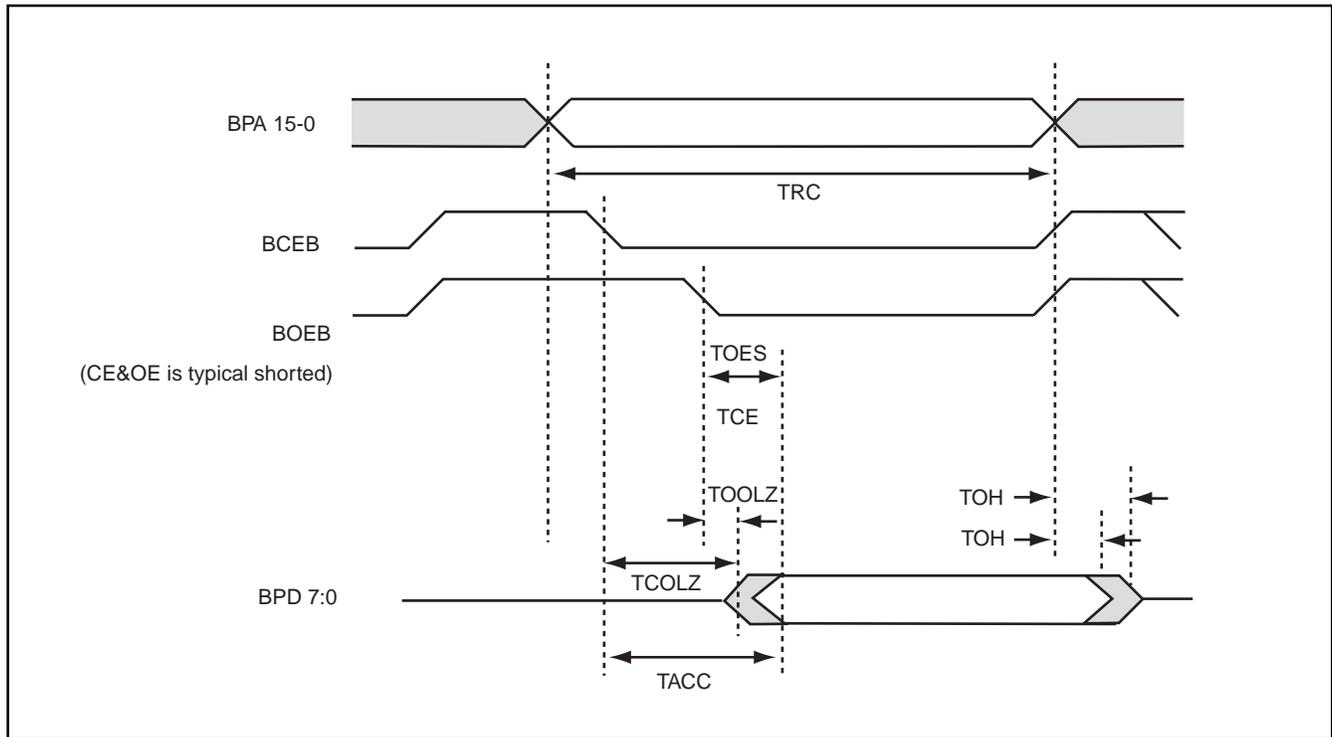
6.2 AC CHARACTERISTICS

SYMBOL	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
TRC	Read Cycle	8	-	-	PCI Cycle
TCE	Chip Enable Access Time	-	-	7	PCI Cycle
TACC	Address Access Time	-	-	7	PCI Cycle
TOES	Output Enable Access Time	-	-	7	PCI Cycl
TOH	Output Hold from Address, CEB, or OEB	0	-	-	ns

PCI cycle range:66ns (16MHz)~30ns (33MHz)

6.3 ABSOLUTE OPERATION CONDITION
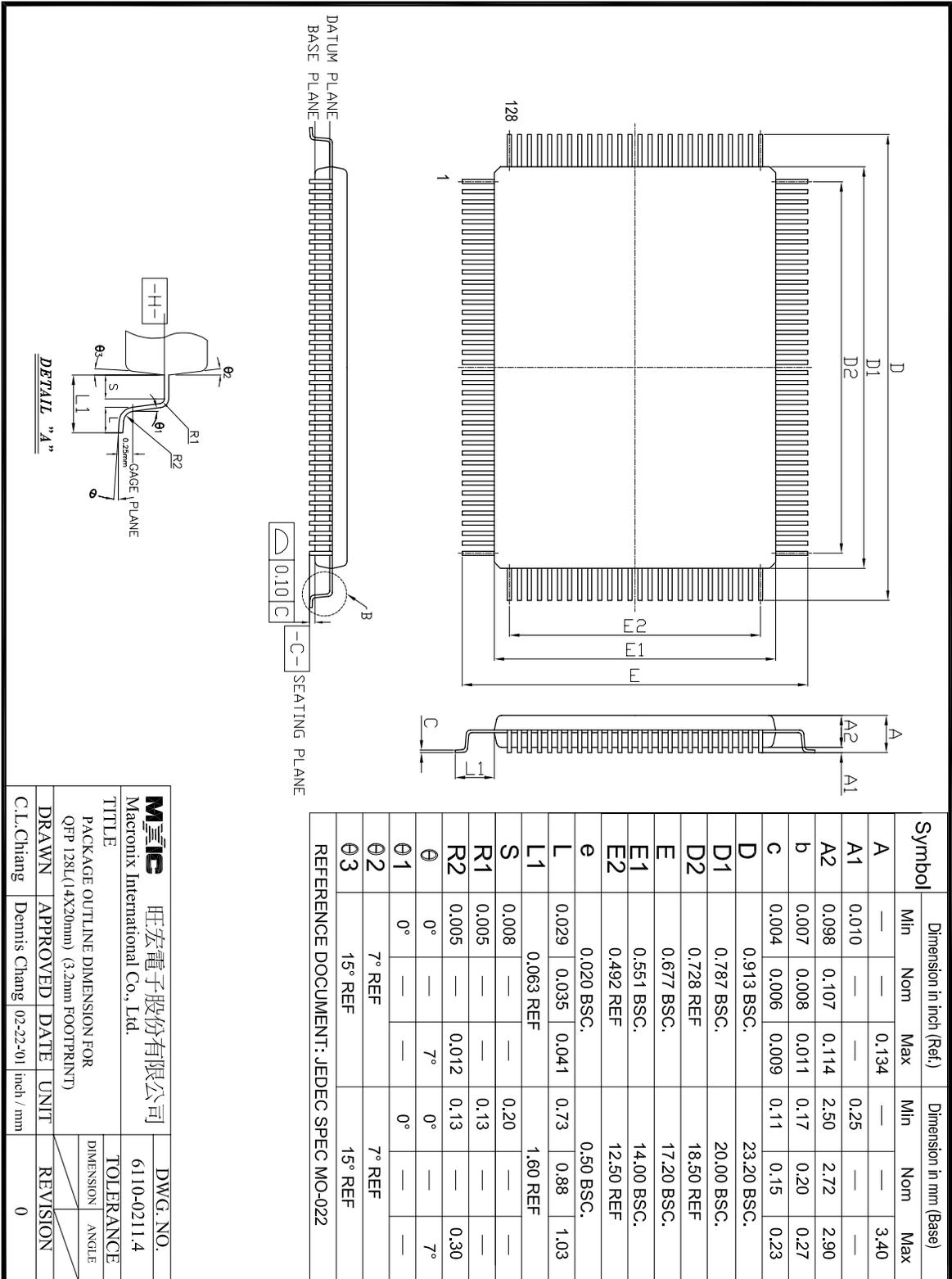
Supply Voltage (VCC)	-0.5V to +7.0V
DC Input Voltage (Vin)	3.15 V to 3.45 V
DC Output Voltage (Vout)	-0.5V to VCC + 0.5V
Storage Temperature Range (Tstg)	-55°C to +150°C
Operating Temperature Range	0°C to 70°C
Operating Surface Temperature(25°C)	48 °C(TYP)
Power Dissipation (PD)	750 mW (Typ.)
Lead Temp. (TL) (Soldering, 10 sec)	260°C
ESD Rating (Rzap = 1.5k, Czap = 100pF)	3kV
Clamp Diode Current	20mA

6.4 DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
TTL/PCI Input/Output					
Voh	Minimum High Level Output Voltage	Ioh = -3mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol = +6mA		0.4	V
Vih	Minimum High Level Input Voltage (3.3V/5V tolerant)			2.0	V
Vil	Maximum Low Level Input Voltage (3.3V/5V tolerant)			0.8	V
Iin	Input Current	Vi = VCC or GND	- 1.0	+ 1.0	uA
Ioz	Minimum TRI-STATE Output Leakage Current	Vout = VCC or GND	-10	+10	uA
LED output Driver					
Vlol	LED turn on Output Voltage	Iol = 16mA		0.4	V
Supply					
Idd	Average Supply Current	CKREF =25MHz			
		PCICLK = 33MHz			
		D0 (100Mbps)		85.5	mA
		D1 (100Mbps)		84	
		D2 (100Mbps)		53	
		D3 (100Mbps)		22	
		D0 (10Mbps)		120	
		D1 (10Mbps)		119	
		D2 (10Mbps)		31	
		D3 (10Mbps)		22	
Vdd	Average Supply Voltage		3.3V	5% tolerant	

7.0 PACKAGE INFORMATION

128-Pin Plastic Quad Flat Pack

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A1	0.010	—	—	0.25	—	—
A2	0.098	0.107	0.114	2.50	2.72	2.90
b	0.007	0.008	0.011	0.17	0.20	0.27
C	0.004	0.006	0.009	0.11	0.15	0.23
D	0.913 BSC.			23.20 BSC.		
D1	0.787 BSC.			20.00 BSC.		
D2	0.728 REF			18.50 REF		
E	0.677 BSC.			17.20 BSC.		
E1	0.551 BSC.			14.00 BSC.		
E2	0.492 REF			12.50 REF		
e	0.020 BSC.			0.50 BSC.		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 REF			1.60 REF		
S	0.008	—	—	0.20	—	—
R1	0.005	—	—	0.13	—	—
R2	0.005	—	0.012	0.13	—	0.30
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	7° REF			7° REF		
θ3	15° REF			15° REF		

REFERENCE DOCUMENT: JEDEC SPEC MO-022

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
0.3	Insert "L" in parts NO. to distinguish this parts is an 3.3V parts		MAR/30/2001

TOP SIDE MARKING

MX98L715BEC	line 1 : MX98L715B is MXIC parts No. "E" : PQFP "C" : commercial grade
C9930	line 2 : Assembly Date Code.
TA777001	line 3 : Wafer Lot No.
TAIWAN	line 4 : State

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