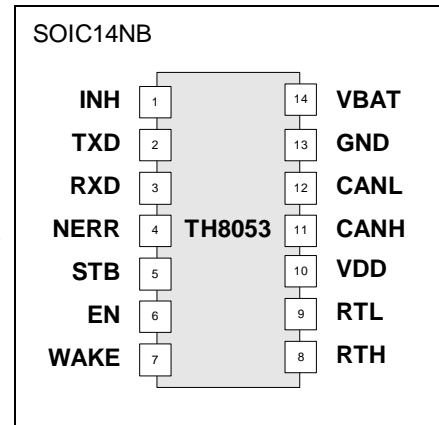


Fault Tolerant Low Speed CAN Transceiver

Features and Benefits

- Baud rate up to 125k Baud
- Up to 40 nodes can be connected
- Automotive temperature range from -40°C...125°C
- Very low standby current
- Short circuit protection of bus lines to V_{DD} , ground and battery
- Wake up capability from bus line or wake up pin
- Supports unshielded bus wire
- Integrated receiver filters
- Permanent dominant monitoring of transmit data input
- Automatic switching to single wire mode in case of bus failures and automatic reset to differential mode if bus failure disappeared
- One wire transmission mode with ground offset up to 1.5V possible
- Very low RFI due internal slope control of bus drivers
- Good immunity to EMC
- Thermal protection of bus line drivers

Pin Diagram



Ordering Information

Part No.	Temperature Range	Package
TH8053.2	-40°C...125°C	SOIC14, 150mil

General Description

The TH8053 is a fault tolerant CAN-Transceiver which works as an interface between the CAN protocol controller and the physical CAN bus. It is designed to connect up to 40 control nodes in passenger cars with an overall cable length of up to 80m enabling data transmission/reception rates up to 125 kBaud using unshielded bus wires.

In normal operation mode the device supports the high security differential transmit capability of the differential CAN bus. In the recessive state data coming from the bus is filtered and after converting to a single-ended sig-

nal fed to the RXD output pin that is to be connected to the CAN controller (reception of data). In the dominant state data send from the controller to pin TXD drives the CAN bus lines.

The device automatically switches to an appropriate single ended mode in the case of a bus failure ensuring further function of the I network. If the failure gets removed the TH8053 automatically resets itself to normal operation. Furthermore it enables single ended transmission on wires with a ground shift up to 1.5V. The TH8053 also ensures the data transfer if the system contains a single

General Description (continued)

unpowered node (e.g. a missing termination resistor). Another feature added is the monitoring of the TXD-input to prevent the controller from obstructing the CAN bus by sending a permanent dominant state. The presence of any of these errors is indicated by a LOW-signal at the NERR-pin.

Standby and sleep modes enable low current consumption if no transmit capability is needed or if the supply voltages drop under a specified level. A wake-up function recalls the normal operation mode whenever a slope is detected at the WAKE-Pin or transmission of data on the bus occurs.

Other important features within passenger cars are the low RF-interference due to a limitation of rise and fall slopes as well as the insensitiveness to RF-radiation achieved by integrated receiver filters.

A thermal shut-down circuit prevents the TH8053 from any damage caused by increased power consumption of the CAN output stages while all other parts of the circuit remain working. Furthermore the TH8053's bus connections (CANH, CANL) are short-circuit proof to battery and ground voltage as well as any pin is protected against ESD-Events.

Functional Diagram

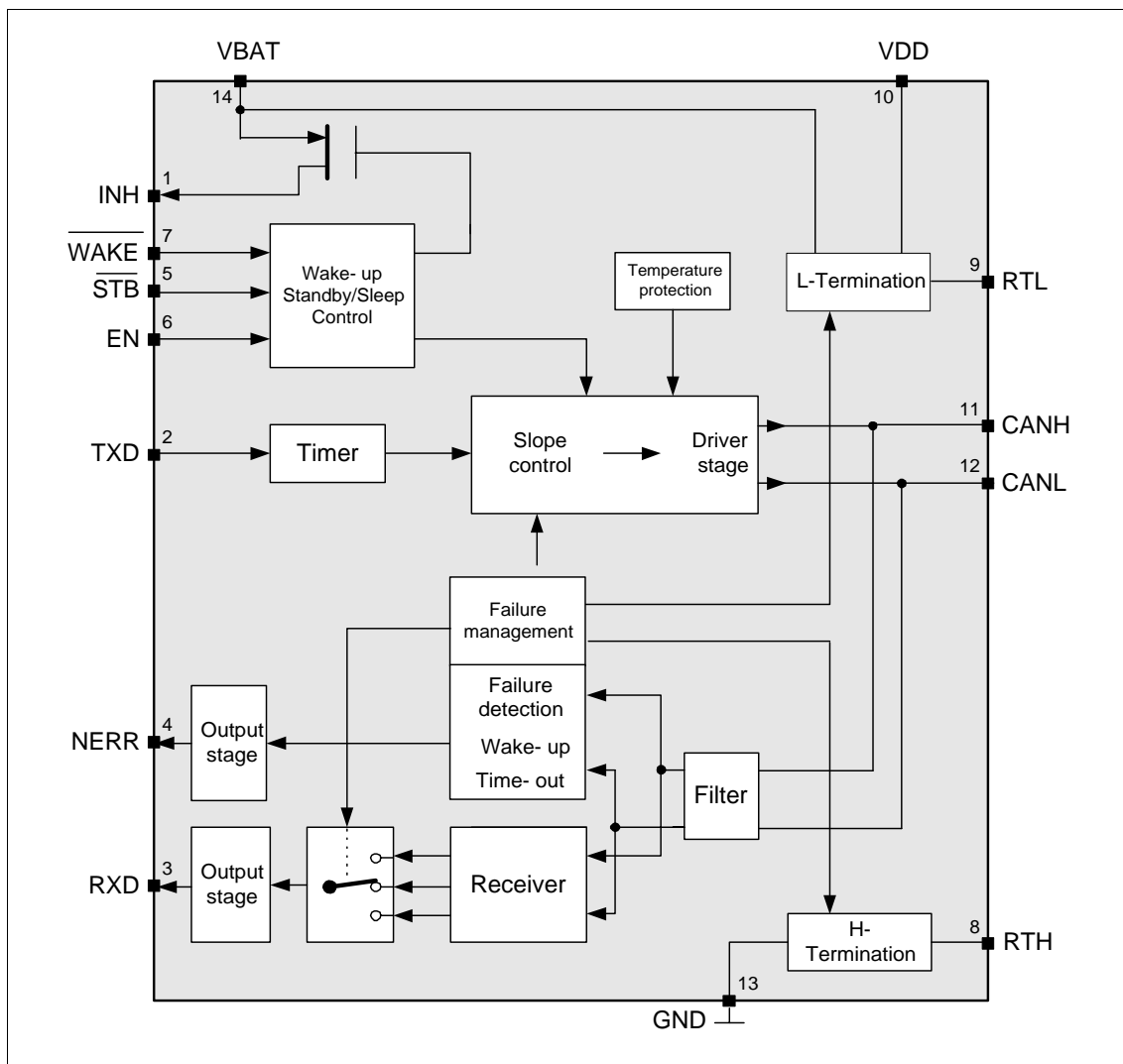


Figure 1 - Block Diagram

Functional Description (continued)

The signal coming from the differential CAN bus is fed to a filter stage to inhibit high frequencies that interfere the bus line from disturbing the evaluation of the incoming bus data. The cut-off frequency of the filters has to be regarded as a trade-off between RF-suppression and propagation delay.

The failure detection circuit determines whether one of the failures described in Table 1, "CAN bus failures, exists and indicates a present error as an active LOW at the NERR output. Furthermore the information of the kind of failure is given to the failure management block which takes the appropriate measures to ensure transmission and reception of data. This includes the control of the correct termination of the CAN bus lines as well as the choice of the right derivation of the receiver signal (output to the RXD-pin) from the CANH and CANL inputs. The failure management also contains the possibility to disable one of the driver stages (e.g. in the case of failure 6 the high side driver and the RTH termination are disabled to reduce current consumption). During any kind of single-wire data transfer RF-radiation and RF-sensitivity are increased.

The failure detection consists of two detection circuits, one being active in the normal operation mode and the other one working in the standby and sleep modes. Recovery of the failures is done with a certain time-out that depends on the failure. A wake-up function that detects incoming dominant signals from the bus is also included. A wake-up command can also be generated by changing the logical voltage level at the WAKE-pin. The mode the TH8053 is running within and whether the INH-pin disables an external voltage regulator can be controlled by the EN- and STB-pins as shown in Table 3, "Mode Control, on page 4 and detailed described in "Operation Modes" on page 4

Another feature implied in this can transceiver device is

Table 1 - CAN bus failures

(Definition in accordance with ISO 11519-2)

Nr.	Failure description	Condition
1	CANL wire interrupted	
2	CANH wire interrupted	
3	CANL short-circuited to battery supply voltage	$V_{BAT} > 7.2$
3a		$1.8V < V_{BAT} < 7.2V$
4	CANH short-circuited to ground	
5	CANL short-circuited to ground	
6	CANH short-circuited to battery supply voltage	$V_{BAT} > 7.2 V$
6a		$1.8V < V_{BAT} < 7.2V$
7	CANH short-circuited to CANL	

the time-out circuit at the TXD-Input that prevents occupation of the CAN bus by a long-term dominant signal sent from the CAN controller. If no failure occurs the TXD-signal coming from the CAN controller is fed to the driver stage which includes a limitation of slopes to reduce RF-interference caused by radiation on the CAN bus.

To prevent the chip from a thermal breakdown a temperature protection circuit shuts down the driver stages which represent the biggest part of the whole power consumption. All other parts remain active thus a reception of data is still possible. After cooling down and reaching the low temperature level the transmitter will be enabled again.

Error Management

Depending on the occurring error appropriate measures have to be taken to ensure data transmission and reception. Table 2, "Error Management", lists the means to achieve this target in the normal operation mode. The comparator signal that determines the value of RXD is given in the second column, the third and fourth ones contain the information whether either one of the terminations RTH or RTL is switched off to reduce the current flowing in the termination resistances. The last two columns display if one of the transmitter drivers is deactivated.

If an interrupt of the CANH or CANL wire between two ECUs is detected (failures 1 and 2) there is no need to disable the corresponding high or low side driver because differential transmission towards other ECUs may still be useful.

Table 2 - Error Management

Errors 1 and 3a as well as errors 2 and 4 can't be distinguished by the receiver.

Error	Output to RXD	Termination ¹		Driver	
		RTH	RTL	CANH	CANL
1	D	on	on	on	on
2	D	on	on	on	on
3	H	on	off	on	off ²
3a	D	on	on	on	on
4	D	on	on	on	on
5	H	on	off	on	off
6	L	off	on	on	on
6a	L	off	on	on	on
7	H	on	off	on	off

¹ If the termination is switched off, a current of 75µA is supplied at the RTH -or- RTL-pin.

² Low side driver is switched off after two unsuccessful attempts of reaching dominant level.

Operation Modes

The different operation modes can be selected by the signals provided at the EN- and STB-pins. There are three operation modes which enable reduced power consumption: the sleep mode, the V_{BAT} -standby mode and the V_{DD} -standby mode.

The sleep mode (STB=0, EN=0) is the one with the lowest power consumption because the whole chip and even the external voltage regulator get disabled. This mode can only be reached if an intermediate mode (STB=0, EN=1) is entered which is interpreted as a "go-to-sleep"-command. Otherwise the chip switches to the V_{BAT} -standby mode (STB=0, EN=0) where the external voltage regulator remains further active. In these modes (go-to-sleep, sleep, V_{BAT} -standby) the RTL-pin is switched to V_{BAT} .

If the external inhibitable voltage regulator is not the one that provides the V_{DD} -supply voltage or if the device is operating in the V_{BAT} -standby mode (external voltage regulator is active) a wake-up request from either the WAKE-pin or the CAN bus line is visible as an active LOW at the NERR and RXD outputs. If V_{DD} has been switched off in the sleep mode the wake-up request will cause the TH8053 to enter the V_{BAT} -standby mode as an intermediate state in which the V_{DD} -supply is present again and so the wake-up can be observed at the NERR- and RXD-pins as well.

Another mode is the V_{DD} -standby mode (STB=1, EN=0). Similar to the normal operation mode the RTL-pin is switched to V_{DD} . The appearance of a wake-up condition in this mode is only displayed at the RXD output as an active LOW. The NERR output is used to indicate the drop of V_{BAT} below 1V. This warn flag is necessary to show that V_{BAT} was missing and that a reinitialisation has to be done. It is reset to HIGH when the device enters the normal operation mode in which the NERR-pin is used to indicate bus failures.

During the low power modes (sleep, V_{BAT} - and V_{DD} -standby) the detection of errors is reduced to the monitoring of the appearance of failures 5, 6 and 7. A complete deactivation of the detection circuit is not sensible because the occurrence of failures 5, 6 and 7 would result in an increased power consumption.

The TH8053 switches itself to the V_{BAT} -standby mode if V_{DD} is missing or below the thresh-old. If V_{DD} is missing the EN and STB inputs will be held internally at LOW level to prevent the chip from entering an inappropriate mode (fail safe functionality). In all standby modes the TH8053 is able to receive interrupts. During the first time of the go-to-sleep command and the specified time after switching from the normal operation mode to the standby modes the device ignores an interrupt.

Table 3 -Mode Control

/STB	EN	Mode	INH	NERR	RXD	RTL
0	0	V_{BAT} -standby ¹	high V_{BAT}	active LOW wake-up interrupt signal if V_{DD} is present		switched to V_{BAT}
0	0	sleep ²	floating			switched to V_{BAT}
0	1	go-to-sleep command	floating			switched to V_{BAT}
1	0	V_{DD} -standby ³	high/ V_{BAT}	active LOW missing V_{BAT} flag	active LOW wake-up interrupt	switched to V_{DD}
1	1	normal operation	high/ V_{BAT}	active LOW error flag flag	HIGH = recessive bus; LOW = dominant bus	switched to V_{DD}

Power-on Procedure

The chip automatically enters the V_{BAT} -standby mode because of its fail safe functionality. In the V_{BAT} -standby mode the INH output will become HIGH and therefore the voltage regulator will provide V_{DD} -supply. The CAN transceiver will remain in the V_{BAT} -standby mode until the CAN controller sets it to another mode. The controller should first enter V_{DD} -standby Mode. This way the CAN controller will be shown by the power-on

flag that it has to reinitialize the ECU (e.g. after exchanging the complete CAN unit or after a battery voltage breakdown).

Through entering the normal mode the V_{BAT} low flag will be reset. Due to special output stages the CAN bus is not loaded if $V_{BAT} = 0V$ which ensures data transmission on the CAN bus even if some ECUs are unpowered.

¹ Wake-up interrupts are released when the normal operation mode is entered

² Sleep mode will be entered instead of V_{BAT} -standby mode if the go-to-sleep command was applied before. (EN may turn LOW as V_{DD} drops without affecting internal functions because of fail safe functionality.)

³ The "missing V_{BAT} " flag will be reset to HIGH when the normal operation mode is entered

Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do

so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8053 is only specified within the limits shown in "Operating conditions"

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Notes
DC supply voltage	V_{CC}	-0.3	+6.0	V	
Battery voltage	V_{Bat}	-0.3	+27	V	1
			40		
DC Input voltage at pins 2 to 6	V_{2-6}	-0.3	$V_{CC} + 0.3$	V	
CANH, CANL input voltage	$V_{CANH,L}$	-10	27	V	2
		-40	40		3
CANH, CANL transient input voltage	$V_{CANH, L, tran}$	-150	100	V	
Termination resistance at pins 8 and 9	R_{TH}, R_{TL}	500	16000	Ω	
DC input voltage at pin 1, 8, 9	$V_{1,8,9}$	-0.3	$V_{BAT}+0.3$	V	
DC input voltage at pin 7	V_{WAKE}		$V_{BAT}+0.3$	V	
DC input current at pin 7	I_{WAKE}	-15		mA	
Maximum latch-up free current at any pin	$I_{Latch-up}$	-500	+500	mA	
Electrostatic discharge voltage at any pin	V_{ESD}	-2000	+2000	V	4
Storage temperature range	T_{STG}	-55	+150	$^{\circ}C$	
Junction temperature	T_{Junc}	-40	+150	$^{\circ}C$	6
Thermal Resistance from junction to ambient	R_{Th}		120	K/W	

Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
DC supply voltage	V_{DD}	4.75	5.25	V	
Battery voltage	V_{BAT}	6	27	V	
Operating ambient temperature	T_{amb}	-40	+125	$^{\circ}C$	
Junction temperature	T_{junc}	-40	+150	$^{\circ}C$	6

¹ $t < 500ms$; load dump

² $V_{DD}=0$ to 5.5V; $V_{BAT}>0$ V; $t<0.1$; no time limit

³ $V_{DD}=0$ to 5.5V; $V_{BAT}>0$ V; $t<0.1$ ms; load dump

⁴ For a human body model (equivalent to discharging 100pF with 1.5k Ω).

⁵ For a human body model (equivalent to discharging 100pF with 1.5k Ω).

⁶ Junction temperature is defined in IEC 747-1

Static Characteristics

$V_{DD} = 4.75$ to $5.25V$, $V_{Bat} = 6$ to $27V$, $T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$, $V_{STB} = V_{DD}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply						
Supply current	I_{DD}	recessive, normal operation mode, $TXD = V_{DD}$		4	8	mA
		dominant, normal operation mode, no load, $TXD = 0V$		6	10	mA
Supply current	I_{BAT}	sleep mode, $V_{DD} = 0V$, $V_{BAT} = 12V$		25	50	μA
Supply current	$I_{DD} + I_{BAT}$	V_{DD} -standby mode, $V_{DD} = 5V$, $V_{BAT} = 12V$		100	200	μA
		V_{BAT} -standby mode, $V_{DD} = 5V$, $V_{BAT} = 12V$		35	95	μA
Battery voltage for setting power-on flag	$V_{BAT, pwon}$	standby and sleep modes			1	V
Supply voltage	V_{DD}	fail safe forced V_{BAT} standby mode	2.75		4.5	V
CANH, CANL						
Differential receiver threshold voltage recessive to dominant	V_{diffRX}	no bus failure and bus failure 1,2, 4	-2.9	-2.5	-2.2	V
Differential receiver threshold voltage dominant to recessive			-3.2	-2.9	-2.5	V
Single-ended receiver threshold of CANL	V_{CANLse}	bus failures 4, 6, 6a	2.8	3.1	3.4	V
Single-ended receiver threshold of CANH	V_{CANHse}	bus failures 3, 5, 7	1.5	1.85	2.2	V
CANH recessive output voltage	$V_{CANHrec}$	$TXD = V_{DD}$, $R_{TH} < 4k$	0.1	0.2	0.3	V
CANL recessive output voltage	$V_{CANLrec}$	$TXD = V_{DD}$, $R_{TL} < 4k$	$V_{DD} - 0.2$			
CANH dominant output voltage	$V_{CANHdom}$	$TXD = 0V$, normal operation mode, $I_{CANH} = -40mA$	$V_{DD} - 1.4$		V_{DD}	V
CANL dominant output voltage	$V_{CANLdom}$	$TXD = 0V$, normal operation mode, $I_{CAN} = 40mA$		1.1	1.4	V
CANH output current	I_{CANH}	$V_{CANH} = 0V$, $TXD = 0V$	-120	-80	-50	mA
		sleep mode, $V_{CANH} = 12V$		0		μA

Static Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CANL output current	I_{CANL}	$V_{CANL}=12V, TXD=0V$	75	140	180	mA
		$V_{CANL}=5V, TXD=0V$	50	80	120	mA
		sleep mode $V_{CANH}=0V, V_{BAT}=12V$	-5	0	5	μA
Threshold for detection of short circuit between CANH or CANL and battery	$V_{HLBATdet}$	normal operation mode	6.5	7.3	8.0	V
Threshold for detection of short-circuit between CANH and battery	$V_{HBATdet}$	standby and sleep modes	$V_{BAT}-2.5$	$V_{BAT}-2$	$V_{BAT}-1$	V
CANH wake-up voltage	V_{Hwu}	standby and sleep modes	1.2	1.9	2.7	V
CANL wake-up voltage	V_{Lwu}	standby and sleep modes	2.4	3.1	3.8	V
difference of wake-up thresholds	$V_{Lwu}-V_{Hwu}$	standby and sleep modes	0.2			V
CANH leakage current	$I_{CANHleak}$	$V_{DD}=0V, V_{BAT}=0V,$ $V_{CANL}=13.5V,$ $R_{TL}=100, T_{junc}<85^{\circ}C$	-5	0	5	μA
CANL leakage current	$I_{CANLleak}$	$V_{DD}=0V, V_{BAT}=0V, V_{CANH}=5V,$ $R_{TL}=100, T_{junc}<85^{\circ}C$	-5	0	5	μA
RTH, RTL						
RTL to V_{DD} switch -on resistance	R_{RTL}	normal operation mode, $I_0 = -10mA$		43	95	
RTL to V_{BAT} switch-on resistance		V_{BAT} standby or sleep mode	8	12.5	23	k
RTH to ground switch -on resistance	R_{RTH}	normal operation mode, $I_0=10mA$		43	95	
RTH output voltage	V_{RTH}	standby and sleep modes, $I_0<1mA$		0.7	1	V
RTL output voltage	V_{RTL}	V_{DD} -standby mode, $I_0<1mA$	$V_{DD}-1$	$V_{DD}-0.7$		V
RTL pull-down current	I_{RTLpd}	normal operation mode, bus failures 3, 3a, 5, 7; $V_{RTH}=1.5V$	45	75	135	μA
RTL pull-up current	I_{RTLpu}	normal operation mode, bus failures 3, 3a, 5, 7; $V_{RTL}=3.4V$	-40	-75	-110	μA
RTH leakage current	$I_{RTHleak}$	$V_{DD}=0V, V_{BAT}=0V, V_{CANH}=5V,$ $R_{TL}=100, T_{junc}<85^{\circ}C$	-5	0	5	μA
RTL leakage current	$I_{RTLleak}$	$V_{DD}=0V, V_{BAT}=0V,$ $V_{CANL}=13.5V, R_{TL}=100,$ $T_{junc}<85^{\circ}C$	-5	0	5	μA

Static Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
/STB, EN, TXD						
HIGH level input voltage	V_{INhigh}	rising edge (input with Schmitt-Trigger)	$0.7 V_{DD}$		$V_{DD}+0.3$	V
LOW level input voltage	V_{INlow}	falling edge (input with Schmitt-Trigger)	-0.3		$0.3 V_{DD}$	V
HIGH level input current at pins /STB and EN	I_{INhigh}	$V_{INhigh}=4V$		9	20	μA
LOW-level input current at pins /STB and EN	$I_{IN, low}$	$V_{INlow}=1V$	4	8		μA
HIGH level input current at pin TXD	I_{INhigh}	$V_{INhigh}=4V$	-200	-50	-25	μA
LOW level input current at pin TXD	I_{INlow}	$V_{INlow}=1V$	-800	-250	-100	μA
RXD, NERR						
HIGH level output voltage	$V_{OUThigh}$	$I_O = -100\mu A$ (NERR)	$V_{DD} - 0.9$		V_{DD}	V
		$I_O = -250\mu A$ (RXD)				
LOW level output voltage	V_{OUTlow}	$I_O = -1.25mA$	0		0.9	V
/WAKE						
Threshold for wake up	V_{WAKE}	$V_{/STB}=0V$	2.4	3.1	4.0	V
input current	I_{WAKE}	$V_{/STB}=0V$	-3	1	-0.3	μA
INH						
HIGH level voltage drop $V_{drophigh} = V_{BAT} - V_{INH}$	$V_{drophigh}$	$I_{INH} = -0.18mA$		0.5	0.8	V
Leakage current	$I_{leaklow}$	sleep mode, $V_{INH}=0V$	-5.0		5.0	μA
Thermal Protection						
Junction temperature to shut down the CANH, CANL drivers	T_{juncsd}		150	165	180	$^{\circ}C$

Dynamic Characteristics

The devices R1, C1 and C2 which values are given in the column "Condition" of the table below refer to the test-schematic shown in Figure 4, "Test Circuit for Dynamic Characteristics"
 For the definition of propagation delay and transitions times see Figure. 2 - TH8053 Timing Diagram

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transition time of CANH and CANL from recessive to dominant	$t_{\text{rec-dom}}$	10% to 90%, $C_1=10\text{nF}$, $C_2=0$, $R_1=100$	0.6	1	2.2	μs
Transition time of CANH and CANL from dominant to recessive	$t_{\text{dom-rec}}$	10% to 90%, $C_1=1\text{nF}$, $C_2=0$, $R_1=100$	0.2	0.3		μs
Propagation delay from TXD to RXD for H-L-transitions (recessive to dominant)	$t_{\text{TXRXH-L}}$	$C_1=100\text{pF}$, $C_2=0$, $R_1=100$, no bus failures and bus failures 1, 2, 3a, 4		0.8	1.5	μs
		$C_1=C_2=3.3\text{nF}$, $R_1=100$, no bus failures and bus failures 1, 2, 3a, 4		1.2	1.8	μs
		$C_1=100\text{pF}$, $C_2=0$, $R_1=100$, bus failures 3, 5, 6, 6a, 7		0.8	1.5	μs
		$C_1=C_2=3.3\text{nF}$, $R_1=100$, bus failures 3, 5, 6, 6a, 7		1.2	1.8	μs
Propagation delay from TXD to RXD for L-H-transitions (dominant to recessive)	$t_{\text{TXRXL-H}}$	$C_1=100\text{pF}$, $C_2=0$, $R_1=100$, no bus failures and bus failures 1, 2, 3a, 4		1.5	2.0	μs
		$C_1=C_2=3.3\text{nF}$, $R_1=100$, no bus failures and bus failures 1, 2, 3a, 4		2.2	3.2	μs
		$C_1=100\text{pF}$, $C_2=0$, $R_1=100$, bus failures 3, 5, 6, 6a, 7		0.9	1.5	μs
		$C_1=C_2=3.3\text{nF}$, $R_1=100$, bus failures 3, 5, 6, 7		1.4	2.1	μs
CANH or CANL minimum dominant time for wake-up	t_{CANHLwu}	standby or sleep modes, $V_{\text{BAT}}=12\text{V}$	8	20	35	μs
Minimum change time of /WAKE for wake up	t_{WAKEmin}	standby or sleep modes, $V_{\text{BAT}}=12\text{V}$	8	20	35	μs
Disable time of permanent dominant TXD timer	t_{TXDdis}	normal operation mode and all bus failures	1	2.5	4.0	ms
Low time of missing battery voltage for setting power-on flag	t_{pwon}	standby and sleep modes		0.2	1	ms
Minimum hold time for go-to-sleep command	t_{go2sleep}		4	20	35	
Difference of edge count between CANH and CANL for detection of failures 1, 2, 3a, 4	$\Delta\text{ec}_{\text{fail}}$	normal operation mode		4		
Difference of edge count between CANH and CANL for recovery of failures 1, 2, 3a, 4	$\Delta\text{ec}_{\text{rec}}$	normal operation mode		2		

Dynamic Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Detection time of failure 3, 6	$t_{fail,det}$	normal operation mode	20		85	μs
6a			2	5	8	ms
5, 7			0.75	2	4.0	ms
5, 6, 6a, 7		standby and sleep, modes, $V_{BAT}=12V$	0.8	4	8.0	ms
recovery time of failure 3	$t_{fail,rec}$	normal operation mode	150	400	750	μs
5, 6, 6a, 7			20		85	μs
5, 6, 6a, 7		standby & sleep modes, $V_{BAT}=12 V$		4	80	μs
Time for settling the normal operation mode from any other mode	$t_{nm,sett}$	$V_{BAT}=12V$		40		μs
Time for leaving the normal operation mode to any other mode	$t_{nm,leave}$	$V_{BAT}=12V$		80		μs

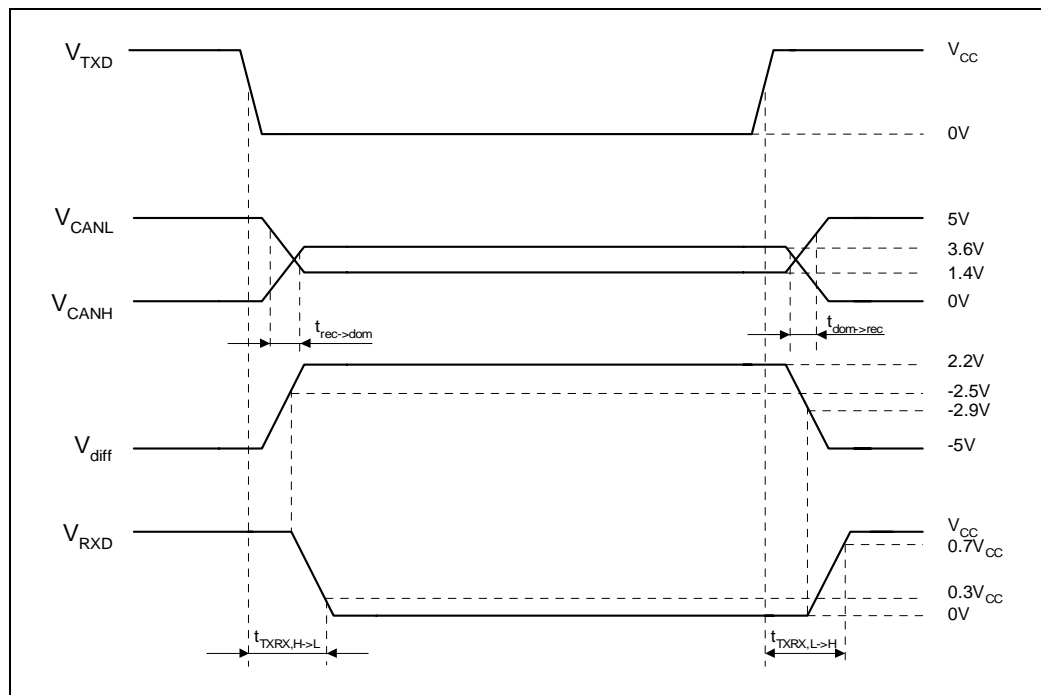


Figure 2 - Timing Diagram

Circuit Examples

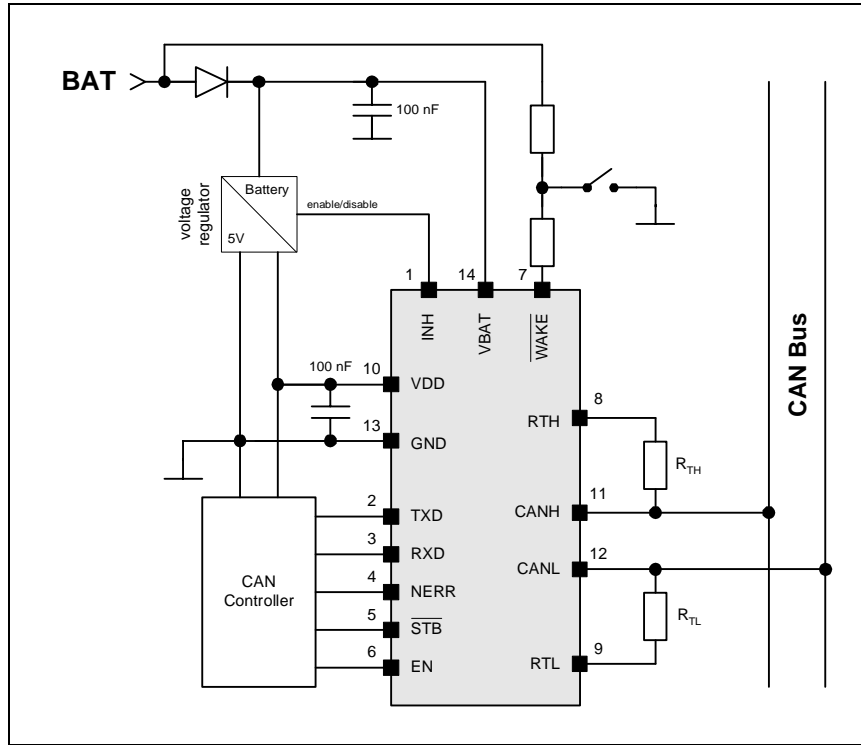


Figure 3 - Application Circuit

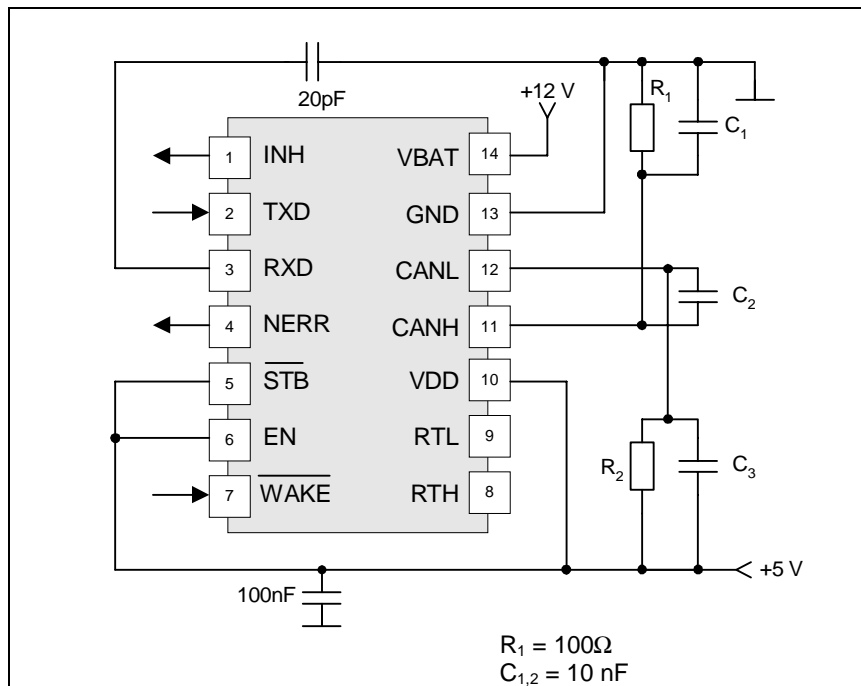
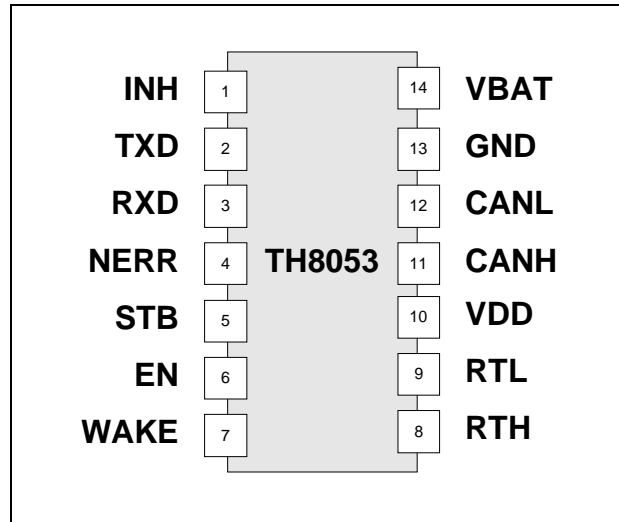


Figure 4 - Test circuit for dynamic characteristics

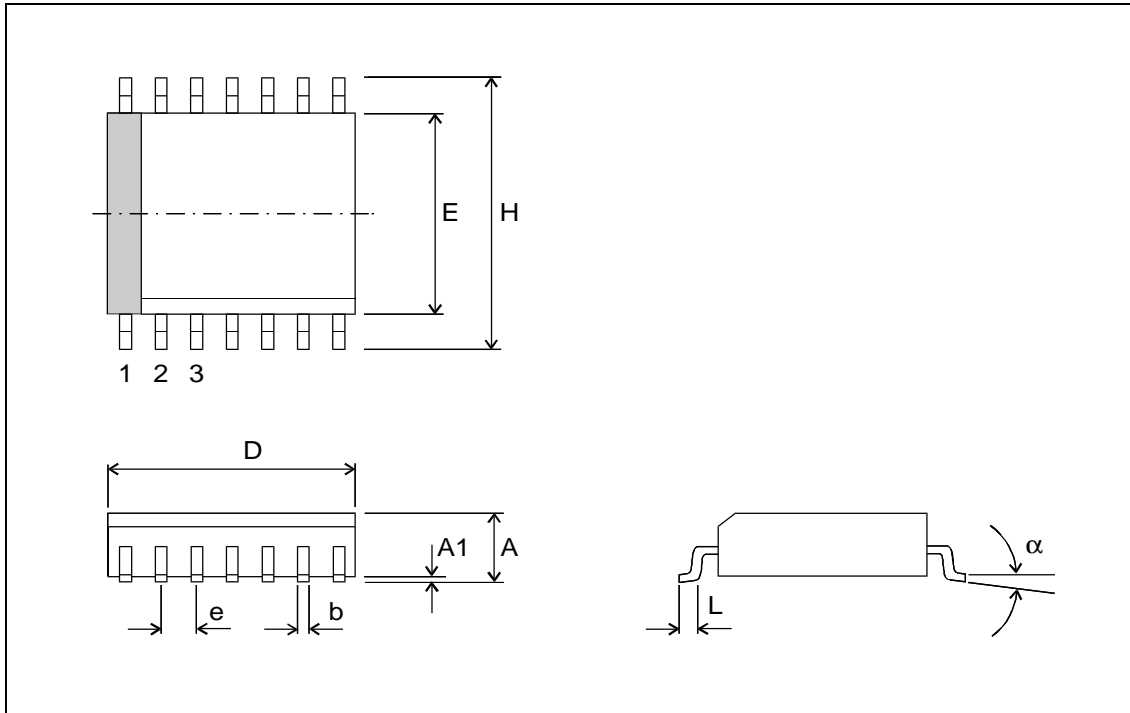
Pin Description



Pin	Name	I/O	Function
1	INH	O	inhibit output for switching external 5V regulator
2	TXD	I	transmit data input
3	RXD	O	receive data output
4	NERR	O	error output pin
5	STB	I	not standby digital control input
6	EN	I	enable digital control input
7	WAKE	I	not wake input signal
8	RTH		termination resistor for CANH
9	RTL		termination resistor for CANL
10	VDD		supply voltage (+5)
11	CANH	I/O	high signal bus line
12	CANL	I/O	low signal bus line
13	GND		ground
14	VBAT		battery voltage

Mechanical Specifications

SOIC14 Package Dimensions



Small Outline Integrated Circuit (SOIC), SOIC 14, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	E	H	A	A1	e	b	L	α
min	8.55	3.80	5.80	1.35	0.10	1.27	0.33	0.40	0°
max	8.75	4.00	6.20	1.75	0.25		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004"									
min	0.337	0.150	0.228	0.053	0.004	0.050	0.013	0.016	0°
max	0.334	0.157	0.224	0.069	0.010		0.020	0.050	8°

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