

### Features and Benefits

- “Soft Start” Eliminates Current Surges
- Integrated Design Eliminates External Components
- Drives Virtually Any Resistive or Inductive Load
- Built-in Thermal Protection
- Digital Design For Stable Triac Control
- Immune to Lifetime and Thermal Drift
- Low Power Consumption
- 50Hz/60Hz Operation

### Applications

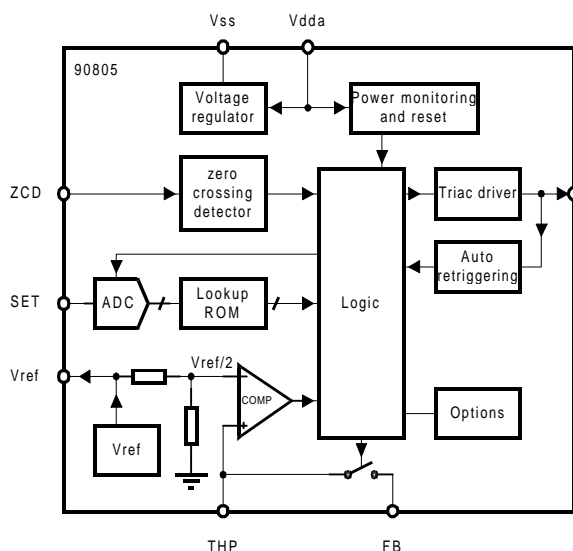
- AC Light Dimmer
- Soft-Start AC Motor Controller
- Variable-Speed AC Motor Controller

### Ordering Information

Part No.	Temperature Suffix	Package	version	Temperature Range
MLX90805	S	A	-x	0C to 85C
MLX90805	S	L	-x	0C to 85C

The customer specific version code (defining the options) is indicated with 1 character at the end of the ordering number.

### Functional Diagram



### Description

The MLX90805 is a power control IC ideally suited for control of any resistive or inductive load regulated by a triac.

The chip was designed primarily for starting and speed control of AC motors, but will work equally well with any Inductive or resistive load such as Incandescent lights.

The chip's primary purpose is to provide a “soft start” for a motor, preventing current inrush. The triac is controlled by a linear “ramp” from minimum to maximum power. Start rate can be varied from 0.5 sec. to 3 sec, by changing the option bits.

The secondary function of the 90805 is proper ignition of the triac for inductive and resistive loads, while keeping the triac's current consumption to a minimum.

Added features include a frequency locked loop for stable ignition point.

### Description of Block Diagram

#### Voltage Regulator

The chip is supplied from the AC line voltage, by a half wave rectifier. The voltage at pin VDDA is limited to ~ 15.5V. The digital part and some of the peripheral blocks are supplied by internally generated VDD ~ 5V.

#### Analog Power on Reset

This block tracks the voltage at VDDA, and permits generation of firing pulses for the triac only if VDDA > ~13V. It is considered otherwise that the motor is not properly supplied by the mains.

#### Oscillator

There is an on chip oscillator. All timing constraints inside the chip are derived from this clock.

#### FLL

A frequency locked loop circuit is implemented to obtain a clock frequency from a current controlled oscillator, by using the mains frequency as a reference. A successive approximation algorithm is used at start up to minimize the time for the oscillator adjustment.

#### Reference Voltage

This voltage is used to supply the external potentiometer for the definition of different speed settings.

#### ADC

The analog signal from the potentiometer, which defines the speed setting, is transferred into digital by a 4-bit ADC. The reference for the converter is the voltage used to supply the potentiometer.

#### ROM

The digital words from the ADC act as the address of a ROM table in which the different firing angles are programmed. This means that 16 different firing angles can be selected.

#### Zero Cross

This block detects the moments when mains voltage crosses zero level. An accurate detection allows good synchronization, so firing pulses driving the triac can be generated at the right moment.

#### Logic

This block performs all control functions to realize time synchronization, smooth soft start, and proper triac firing, so that motor runs at a defined speed.

#### Triac Driver

This output is able to drive directly a triac. It defines the triac gate current and operates as current generator. There is no need of external resistor for current limitation.

#### Auto Retriggering

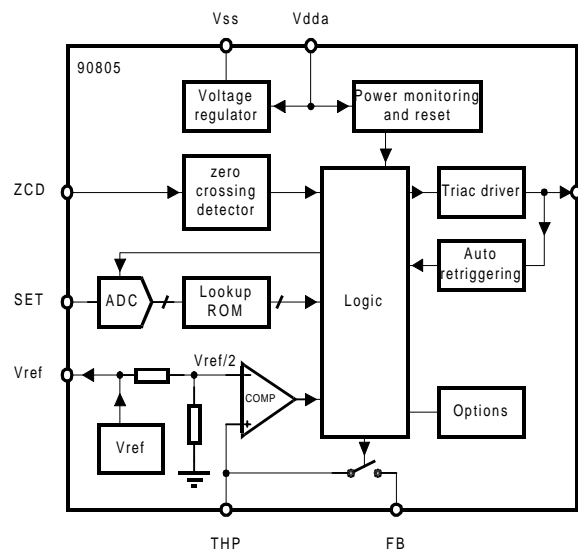
This block tracks if the triac is on after each firing pulse. If the triac is off 20us after a firing pulse, a new pulse is generated.

#### Thermal Protection

The chip is able to supply an external protection circuitry, typically an NTC resistor with reference resistor, to track the ambient temperature. If the voltage at THP equals Vref/2 the protection is activated and the chip sets the firing angle defined by the value in ROM address 1. A resistor connected to pin FB can introduce hysteresis in the detection level.

#### Options

This block defines different modes of the chip operation.



### MLX90805 Electrical Specifications

#### Environmental Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
Tamb	Ambient temperature	0		85	°C	
Tch	Maximum chip temperature			150	°C	
Rth	Thermal resistance		110		°C/Ω	DIP8 or SOP8 package
IDDAm	Maximum allowed source supply current			10	mA	Drivers off, all the current flows in the chip

#### Analog Features

##### Power Supply

High voltage supply should be applied between VDDA and VSS.

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDA	Voltage applied at the supply pin	14	16	18	V	IDDA = 5mA
VDD	Internal 5V supply	4.6	5.0	5.4	V	
IDDA	Current consumption		3		mA	VDDA = 14V
VREF	For external circuitry	4.6	5	5.4	V	IREF = 8mA

##### Power On Reset

This block ensures a correct start of the digital part.

The reset signal goes up for  $VDD > Vdporh$  and down for  $VDD < Vdporl$ .

Symbol	Description	Min	Typ	Max	Unit	Conditions
Vdporh	High level threshold		2.5		V	
Vdporl	Low level threshold		2.0		V	
Vdphyst	Hysteresis		0.5		V	

Symbol	Description	Min	Typ	Max	Unit	Condition
Vaporh	High level threshold	12	13	14	V	
Vaporl	Low level threshold	9	10	11	V	
Vaphyst	Hysteresis	2	3	4	V	

### Zero Cross Detector

This detector contains two comparators with hysteresis. The first comparator has its reference at VDDA. The reference of the second one is VDDA-1V.

Symbol	Description	Min	Typ	Max	Unit	Conditions
Vzc1h	High level threshold 1		VDDA +0.5		V	
Vzc1l	Low level threshold 1		VDDA -0.5		V	
Vzc2h	High level threshold 2		VDDA -1.5		V	
Vzc2l	Low level threshold 2		VDDA -2.5		V	
Rzc	External resistor		470		kΩ	Vline = 230VAC typ

### Triac (Ignition) Driver

This driver operates as a current generator to fire the triac ON.

Symbol	Description	Min	Typ	Max	Unit	Conditions
ITRG	Triac gate current	30	60	90	mA	VDDA > Vaporh

### ADC

Symbol	Description	Min	Typ	Max	Unit	Conditions
	Resolution		4		bits	
VREF	Reference voltage	4.6	5	5.4	V	

## Digital Features

### Debounce of ADC

The result from the potentiometer reading must not jump from one position to the other, therefore a special debouncing is designed. The debounce circuit compares the current value from the ADC with the previous one. The new value is accepted only if the absolute difference between the new and the previous value is greater than 1 LSB.

### Power Settings (ROM table)

The ADC output data is applied after debouncing at the address bus of the ROM and the corresponding power settings are available at its data output SETP [9:0]. The content of the ROM can be defined freely: it does not need to be linearly or continuous. When the potentiometer setting is changed from one position to the other, the phase angle is moved to the new position via the soft start procedure, avoiding abrupt changes.

For programming the different speed settings in the ROM table, following formula can be used, given  $t_i$  (in msec) is the delay from the previous zero crossing to the moment of ignition:

$$ROM_i[9:0] = t_i \cdot 2 \cdot F_{mains} - 10$$

f.e.: for a phase angle of 50%,  $t_i = 5\text{msec}$  for a 50Hz mains, and thus:

$$ROM_i [9:0] = 5 \cdot 2 \cdot 50 - 10 = 490$$

### Note:

The value should not be negative: very small values can not be programmed.

### Soft Start

The soft start is initiated after the supply voltage has been built up. This behavior guarantees a gentle start-up for the motor and automatically ensures the optimum run-up time. The motor is fired initially with a very small phase angle, i.e. a delay time very close to half the mains period. The phase angle is then increasing up to the phase angle defined by the potentiometer setting. The rate of increase is defined by the option ATN[4:0]. This option defines the time to increase the phase angle from minimum to maximum. If the phase angle, selected by the potentiometer, is not the maximum phase angle then the soft start run-up time is decreased proportionally.

### Firing

The soft start circuit generates a predefined set of values for the ignition angle IGN. These values are compared with the value of a down counter, which is clocked by  $DCLK = 100\text{kHz}$  (the resolution is 10 us) and is cleared at beginning of every half period of mains. When the counter value becomes equal to IGN the firing circuit produces an ignition pulse GATE with duration 20us, 40us, 80us or 320us. This duration can be chosen with option DUTS[1:0]. The retriggering circuit checks whether the triac is ON, if not additional firing pulses are generated every 20us (with respect to the end of the previous firing pulse) until firing of the triac.

### Thermal Protection

An external circuitry supplied by VREF defines the voltage at pin THP. This voltage is proportional to  $T_{amb}$ . It is tracked by an internal comparator referred to  $VREF/2$ . The tracking process is sampled. When the switch is ON (see block diagram), the chip checks if  $T_{amb}$  is greater than a predefined value. If yes, the motor is driven to operate at the speed defined at the first ROM address. During the time when the switch is OFF, the chip checks what kind of mode is defined by the external elements: 2-wire or 3-wire potentiometer connection. A reconnection of the elements used for thermal protection is needed only to define the active mode of operation.

The temperatures for which thermal protection becomes active or not are defined by the external elements, keeping in mind that comparator is referred to  $VREF/2$ .

In the case when thermal protection is not used, pin THP should be connected to pin FB, which is connected either to  $V_{ss}$  or to  $V_{ref}$ , depending on the mode.

2-wire mode, if  $V(\text{FB}) = V_{REF}$

3-wire mode, if  $V(\text{FB}) = V_{SS}$

### Pinout

Standard package is 8-pin dual inline package. (Known as DIP-8, PDIP-8, DIL-8 and PDIL-8)

Pin	Name	Type	Description
1	SET	Input	Potentiometer input
2	THP	Input	Thermal protection
3	FB	Input	Feed back to create hysteresis for thermal protection
4	ZC	Input	Zero cross input
5	TRG	Output	Triac driver output
6	VSS	Supply	Ground
7	VDDA	Supply	Supply, high level
8	VREF	Output	Reference voltage

### Precautions

#### Disturbance Immunity

According to pr EN 55014-2

#### ESD

All I/O pins must withstand the normalized ESD pulses up to 2kV (100pF / 1.5 kΩ). The pins will be stressed in both polarities, with respect to the combination of all supply pins.

### Options

The following options are available:

#### Firing angle definition

The firing angles, and corresponding motor speeds, can be defined in ROMi[9:0]. This is the ROM table which is addressed by the ADC reading the potentiometer setting. The ROM contains 16 words of 10 bits. For programming the different speed settings in the ROM table, following formula can be used, given ti (in msec) is the delay from the previous zero crossing to the moment of ignition:

$$ROMi [9 : 0] = ti \cdot 2 \cdot Fmains - 10$$

With: Fmains = frequency of the mains (in Hz)

#### Note:

The value should not be negative: very small values can not be programmed.

The content of the ROM can be defined freely: it does not need to be linear or continuous. However for a proper softstart generation under all conditions, the value with minimum firing angle (thus maximum speed) must be in the highest ROM address.

Default values:

Rom address	Value
0	590
1	567
2	544
3	522
4	500
5	477
6	456
7	434
8	411
9	387
10	362
11	335
12	305
13	273
14	231
15	112

### Maximum phase angle

Independent of the phase angle definitions in the ROM table, a maximum phase angle can be defined. This is the phase angle that will be applied immediately after the power on sequence, and is therefore the first phase angle in the soft start sequence. This maximum phase angle is defined in MIN[9:0] with the formula:

$$\text{MIN}[9:0] = \text{Tini} * 2 * \text{Fmains} - 10$$

With:

Tini = the initial phase angle (in msec)

Fmains = frequency of the mains (in Hz)

Default value:

Tini = 7 msec and Fmains = 50Hz, thus MIN[9:0] is 690.

### Soft start time duration

There are 5 bits ATN[4:0] used to define the duration of the soft start time. The bits can be calculated with following formula:

$$\text{Ts} = ((\text{Tini} - \text{Tmin}) * \text{ATTN}) / 62.5$$

With:

Ts = the duration of the soft start (in sec.)

Tini = the initial phase angle defined by MIN[9:0] (in msec)

Tmin = the phase angle corresponding to the value in the highest ROM address (in msec)

ATTN =  $\text{bin2dec}(\text{ATN}[4:0]+1)$ , a value between 2 and 32.

Default value:

Tini = 8msec, Tmin = 1.84 msec, ATTN = 32, thus Ts = 3.15 sec.

### Firing pulse duration

The duration of the firing pulses can be defined by the bits DUTS[1:0] according to following table.

The default value is 20 usec.

DUTS1	DUTS0	Duration in $\mu\text{S}$
0	0	320
0	1	80
1	0	40
1	1	20

### Enable Retriggering

With bit RTRIG set to 1, triac retriggering is enabled. The retriggering circuit checks whether the triac is ON, if not additional firing pulses are generated every 20us (with respect to the end of the previous firing pulse) until firing of the triac.

With bit RTRIG set to 0, triac retriggering is disabled. For each triac firing two pulses are generated with a delay of 20 usec (with respect to the end of the previous firing pulse).

The default value is triggering enabled.

### Retriggering Mask

With the option MINA[3:0] it is possible to define a zone at the end of each half cycle of the mains voltage, where it is impossible to generate retriggering pulses. This has two purposes:

With some (non inductive) loads the current can become quite small at the end of each half cycle. This can eventually activate the retriggering circuit which will unnecessarily generate additional pulses thus increasing the current consumption.

When generating a retriggering pulse just before the zero crossing, this pulse could overlap to the next half period. With some (non inductive) loads this can lead to false triggering at full power and must be avoided.

The bits MINA[3:0] are defined according to the following formula:

$$\text{Tmina} * 2 * \text{Fmains} = \text{MINA}[3:0] * 64$$

With:

Tmina = the phase angle from which retriggering is prohibited (in msec)

Fmains = frequency of the mains (in Hz)

Default value:

MINA[3:0]=1101'b=13'd and Fmain = 50Hz, this means that retriggering is prohibited at 8.32ms.

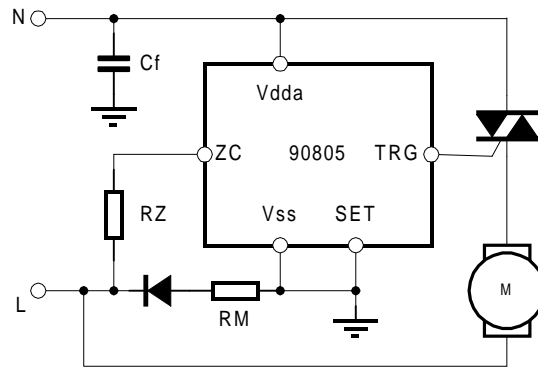
### Soft start only Function regulator

See page 8

### 2-wire or 3-wire potentiometer connection.

See pages 9 and 10

**Applications Example - Soft Start Only**

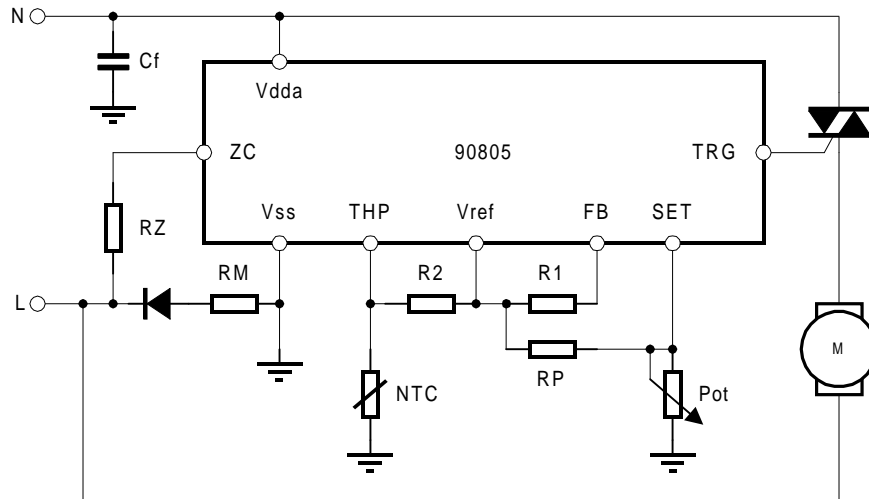


**Soft Start Only**

The chip is used to perform smooth soft start of an electrical motor. It detects when the mains voltage is applied and generates firing pulses for the triac. The motor starts running, and the maximum speed (motor operating at full power) is reached after a predefined time. This application is defined by fixing  $V(\text{SET}) = V_{\text{ref}}$ . This means, after soft start generation, always the maximum speed (corresponding to the highest ROM address) is selected.



**Applications Example - Soft Start with 2-Wire Setting**



**Soft Start With 2-Wire Setting**

The speed control is performed in addition to the soft start in this application. A potentiometer in 2-wire connection is used to define different speed settings. An additional resistor RP with value equal to the potentiometer is used to keep the ADC input to be ratiometric. In this case, the input signal for the ADC varies between 0 and VREF/2.

The minimum speed corresponds to a potentiometer set to its minimum value (i.e. Rpot = 0). Maximum speed corresponds to a potentiometer set to its maximum value. When the mains voltage is applied to the system, the motor starts running at a speed defined by the potentiometer, as soon as the soft start time has finished.

The disadvantage of the 2-wire application is that, at maximum speed setting, the tolerance on the absolute value of the potentiometer defines the tolerance of the voltage at the SET input, resulting in a less accurate selection of the maximum speed setting. This can be avoided when using the 3-wire application.

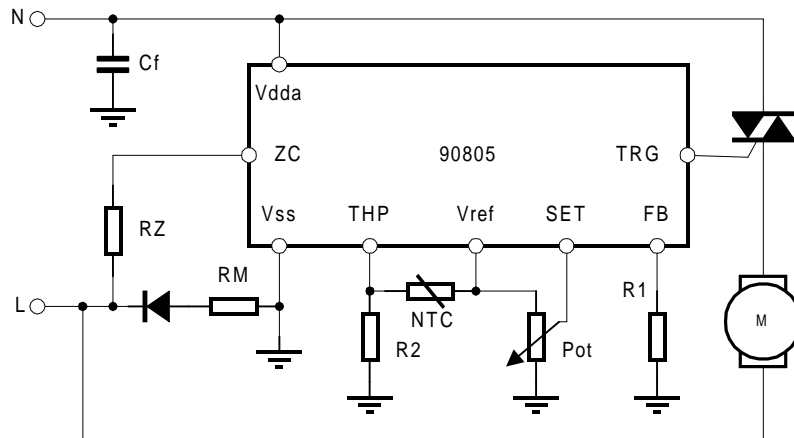
The voltage at SET is transferred to a 4 bit value to address a ROM table in which the different phase angles are defined with a 10 bit resolution.

The 2-wire mode is selected by connecting VFB to VREF (eventually via a resistor).

**Note:**

R1, R2 and NTC are only needed for thermal protection, and can be left out otherwise

**Applications Example - Soft Start with 3-Wire Setting**



**Soft Start With 3-Wire Setting**

The speed control is performed in addition to the soft start in this application. A potentiometer in 3-wire connection is used to define different speed settings. The input signal for the ADC varies between 0 and VREF.

The minimum speed corresponds to a maximum voltage at SET. Maximum speed corresponds to a minimum voltage at SET. When the mains voltage is applied to the system, the motor starts running at a speed defined by the potentiometer, as soon as the soft start time has finished.

The voltage at SET is transferred to a 4 bit value to address a ROM table in which the different phase angles are defined with a 10 bit resolution.

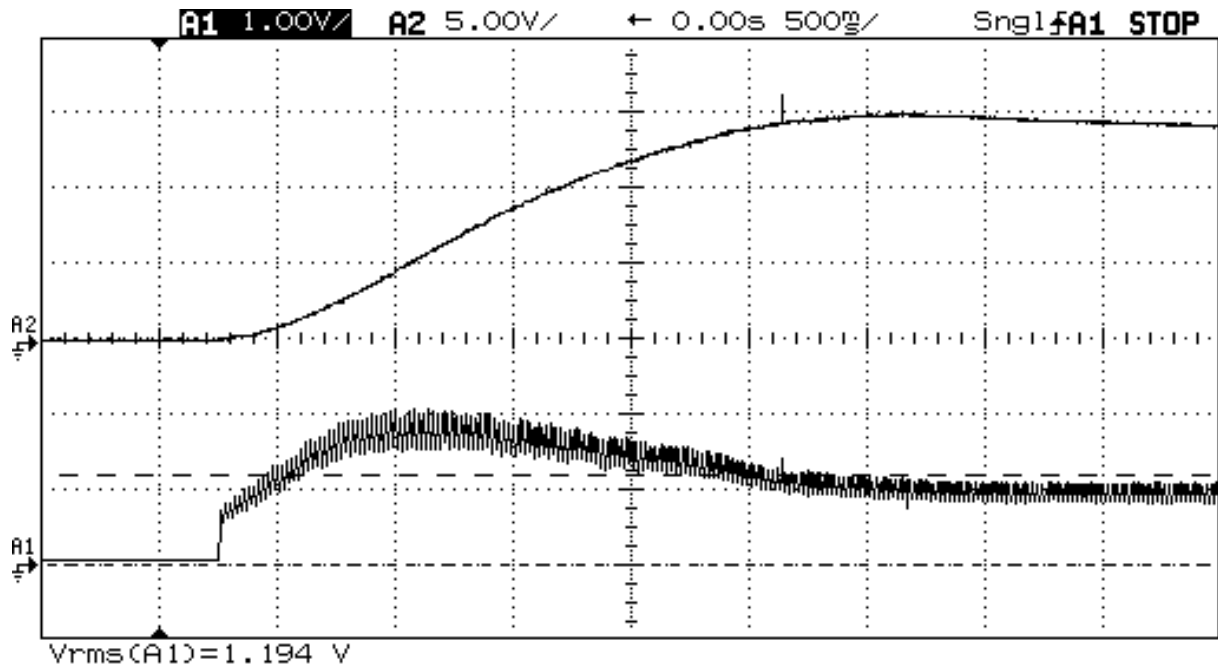
The 3-wire mode is selected by connecting VFB to VSS (eventually via a resistor).

**Note:**

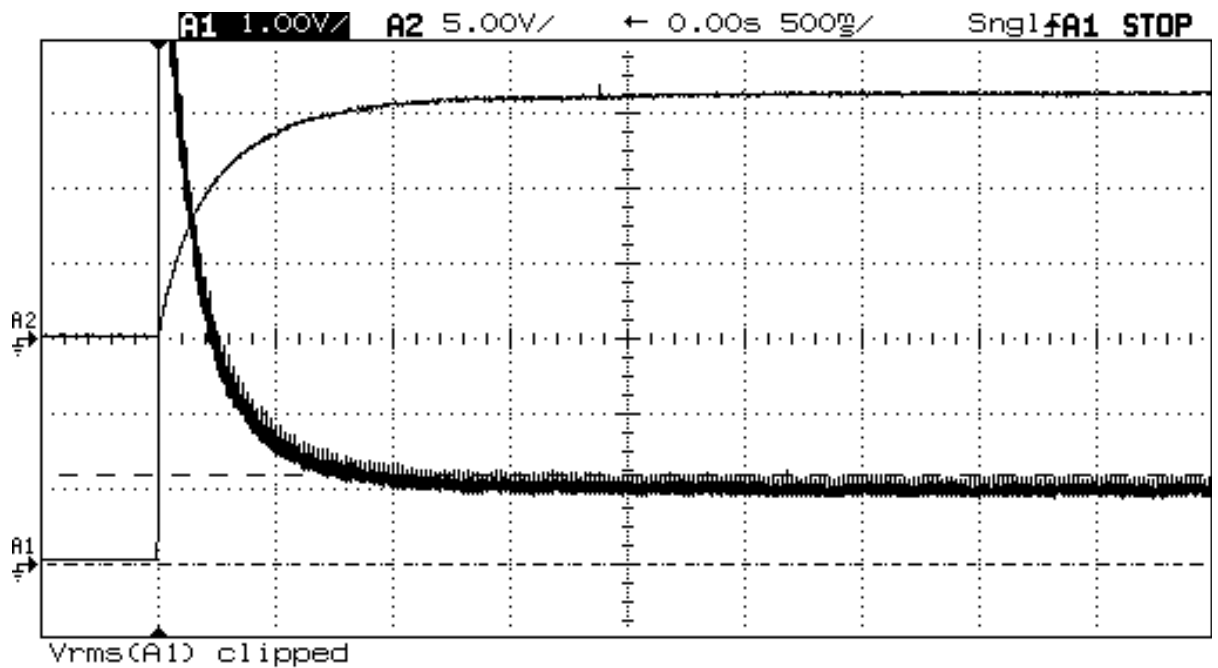
R1, R2 and NTC are only needed for thermal protection, and can be left out otherwise

### Performance of Soft Start Mechanism.

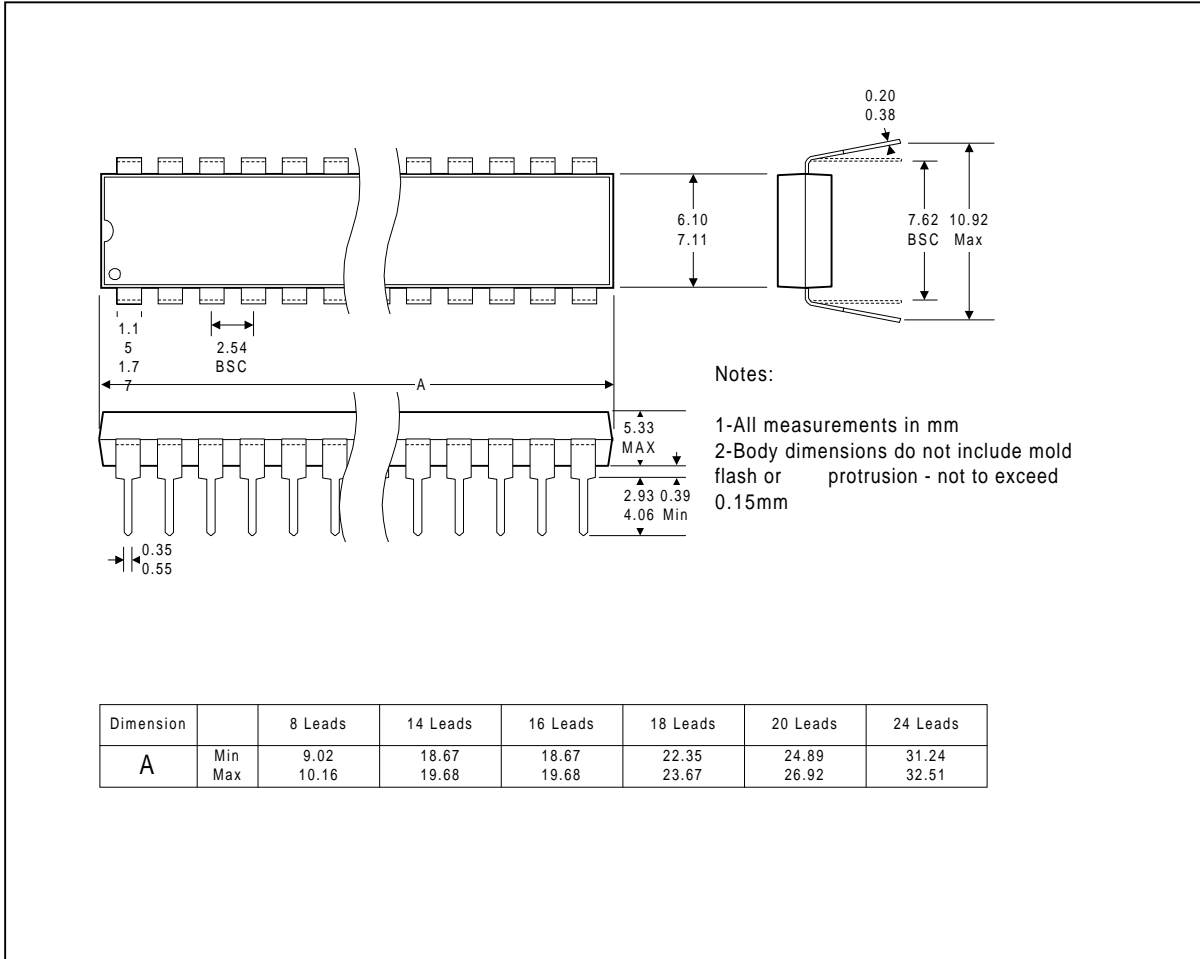
The plots are a measurement of motor current (signal A1) and speed (signal A2) during startup for a particular motor.  
In the first plot we have a soft start of approx. 3 seconds.



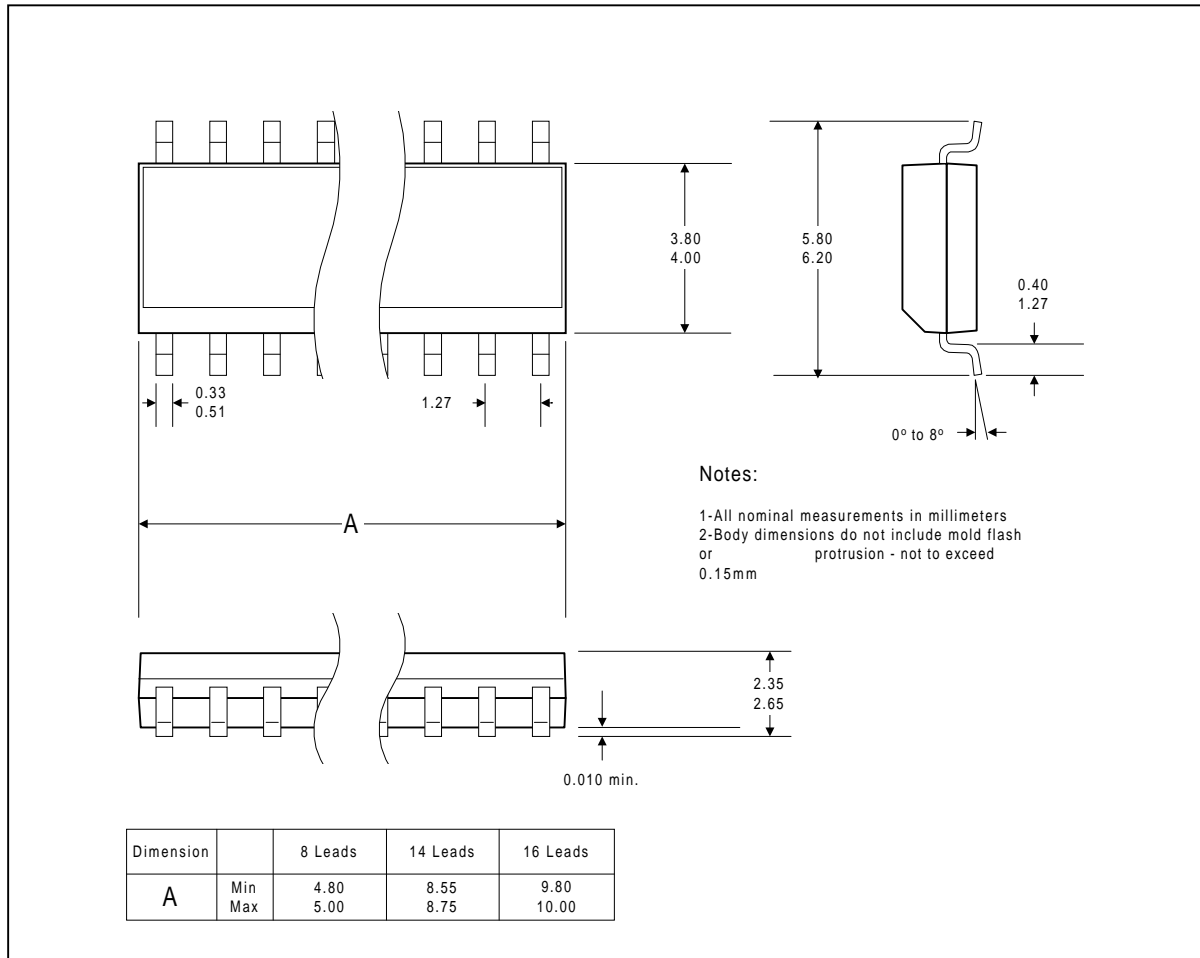
In the second plot we directly connect the same motor to the line voltage:



**“A” Package Dimensions**



### “SO” Package Dimensions



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