MIC2550

Universal Serial Bus Transceiver

Advance Information

General Description

The MIC2550 is a single-chip transceiver that complies with the physical layer specifications for Universal Serial Bus (USB).

The MIC2550 supports full-speed (12Mb/s) dual supply voltage operation (patent pending) and low-speed (1.5Mb/s) operation.

A unique dual supply voltage operation allows the MIC2550 to reference the system I/F I/O signals to a supply voltage down to 2.5V while independently powered by the USB V_{BUS}. This allows the system interface to operate at its core voltage without addition of buffering logic and also reduce system operating current.

Features

- Compliant to *USB Specification Revision 1.1*
- Operation down to 2.5V
- Dual supply voltage operation
- Supports full-speed (12Mb/s) and low-speed (1.5Mb/s) operation
- Speed-select termination supply
- Very low power consumption meets USB suspend-current requirements
- Small 14-pin TSSOP

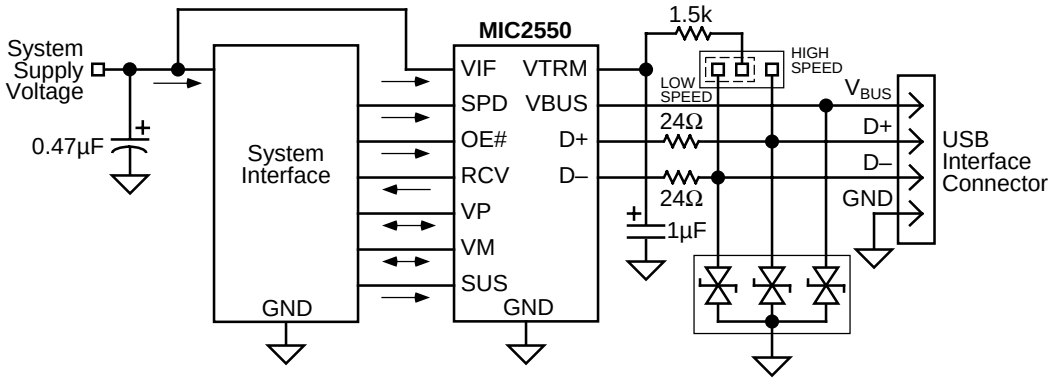
Applications

- Personal digital assistants (PDA)
- Palmtop computers
- Cellular telephones

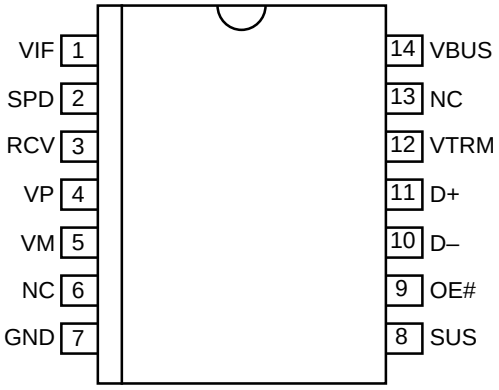
Ordering Information

Part Number	Junction Temp. Range	Package
MIC2550BTS	–40°C to +85°C	14-Pin TSSOP

System Diagram



Pin Configuration



14-Pin TSSOP (TM)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIF	System Interface Supply Voltage (Input): Determines logic voltage levels for system interface signaling to logic controller.
2	SPD	Speed (Input): Edge rate control. Logic high selects full-speed edge rates. Logic low selects low-speed edge rates.
3	RCV	Receive Data (Output): System interface receive data interface to logic controller.
4	VP	Plus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VP is a receiver output (+); If OE# is logic 0, VP is a driver input (+).
5	VM	Minus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VM is a receiver output (–); If OE# is logic 0, VM is a driver input (–).
6, 13	NC	not internally connected
7	GND	Ground: Power supply return and signal reference.
8	SUS	Suspend (Input): Logic high turns off internal circuits to reduce supply current.
9	OE#	Output Enable (Input): Active-low system interface input signal from from logic controller. Logic low causes transceiver to transmit data onto the bus. Logic high causes the transceiver to receive data from the bus.
10	D–	USB Differential Data Line – (Input/Output)
11	D+	USB Differential Data Line + (Input/Output)
12	VTRM	Termination Supply (Output): 3.3V speed termination resistor supply output.
14	VBUS	USB Supply Voltage (Input): Transceiver supply.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{IF}) ..... +6.5V
Input Voltage (V_{BUS}) ..... –0.5V(min)/5.5V(max)
Output Current (I_{D+}, $I_{D–}$) ..... ±50mA
Output Current (all others) ..... ±15mA
Input Current ..... ±50mA
Power Dissipation (P_D) ..... TBD
Storage Temperature (T_S) ..... –65° to +150°C
ESD, **Note 3**

Operating Ratings (Note 2)

Supply Voltage (V_{BUS}) ..... 4.0V to 5.25V
Temperature Range (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... 160°C
Package Thermal Resistance
TSSOP (θ_{JA}) ..... 100°C/W

Electrical Characteristics

T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; typical values at V_{BUS} = 5.0V, V_{IF} = 3.0V; minimum and maximum values at V_{BUS} = 4.0V to 5.25V, V_{IF} = 2.5V to 3.6V; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
System and USB Interface DC Characteristics						
V_{BUS}	USB Supply Voltage		4.0		5.25	V
V_{IF}	System I/F Supply voltage		2.5		5.25	V
V_{IL}	Low-Level Input Voltage, **Note 4**				$0.15V_{IF}$	V
V_{IH}	High-Level Input Voltage, **Note 4**		$0.85V_{IF}$			V
V_{OH}	High-Level Output Voltage, **Note 4**	I_{OH} = 20µA	$0.9V_{IF}$			V
V_{OL}	Low-Level Output Voltage, **Note 4**	I_{OL} = 20µA			0.1	V
I_{IL}	Input Leakage Current, **Note 4**				±5	µA
I_{IF}	System I/F Supply Current	D– and D+ are idle, V_{IF} = 3.6V, V_{BUS} = 5.25V SUS = 1, OE# = 1		1		µA
		D– and D+ are idle, V_{IF} = 3.6V, V_{BUS} = 5.25V SUS = 0, OE# = 1		1		µA
		D– and D+ active, C_{LOAD} = 50pF, SPD = 1, SUS = 0, V_{IF} = 3.6V, OE# = 0		2		µA
		D– and D+ active, C_{LOAD} = 600pF, SPD = 0, SUS = 0, V_{IF} = 3.6V, OE# = 0		2		µA
I_{BUS}	USB Supply Current	D– and D+ are idle, V_{BUS} = 5.25V, SPD = 0 SUS = 1, OE# = 1		140	**200**	µA
		D– and D+ are idle, V_{BUS} = 5.25V, SPD = 1 SUS = 1, OE# = 1		140	**200**	µA
		D– and D+ are idle, V_{BUS} = 5.25V, SPD = 0 SUS = 0, OE# = 0		140	**200**	µA
		D– and D+ are idle, V_{BUS} = 5.25V, SPD = 1 SUS = 0, OE# = 1		200	**350**	µA
		D– and D+ active, C_{LOAD} = 50pF, SPD = 1, SUS = 0, V_{BUS} = 5.25V				mA
		D– and D+ active, C_{LOAD} = 600pF, SPD = 0 SUS = 0, V_{BUS} = 5.25V				mA
V_{TRM}	Termination Voltage	I_{TRM} = 2.5mA	3.0		3.6	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
Transceiver DC Characteristics						
I_{LO}	Hi-Z State Data Line Leakage	0V < V_{BUS} < 3.3V, D+, D–, OE# = 1 pins only	–10		+10	µA
V_{DI}	Differential Input Sensitivity	Ω(D+) – (D–)Ω, V_{IN} = 0.8V – 2.5V	0.2			V
V_{CM}	Differential Common-Mode Range	includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis, **Note 6**			200		mV
V_{OL}	Static Output Low, **Note 5**	OE# = 0, R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	Static Output High, **Note 5**	OE# = 0, R_L = 15kΩ to GND	2.8		3.6	V
V_{CRS}	Output Signal Crossover Voltage **Note 6**		1.3		2.0	V
C_{IN}	Transceiver Capacitance, **Note 6**	pin to GND			20	pF
Z_{DRV}	Driver Output Resistance	steady state drive, **Note 6**	6		18	Ω
Low-Speed Driver Characteristics						
t_R	Transition Rise Time	C_L = 50pF C_L = 600pF	75		 300	ns ns
t_F	Transition Fall Time	C_L = 50pF C_L = 600pF	75		 300	ns ns
t_R/t_F	Rise and Fall Time Matching	$T_R \div T_F$	80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Full-Speed Driver Characteristics						
t_R	Transition Rise Time	C_L = 50pF	4		20	ns
t_F	Transition Fall Time	C_L = 50pF	4		20	ns
t_R/t_F	Rise and Fall Time Matching	$T_R \div T_F$	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended.

Note 4. Applies to the VP, VM, RCV, OE#, SPD, and SUS pins.

Note 5. Applies to D+, D–

Note 6. Not production tested. Guaranteed by design.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Transceiver Timing						
t_{PVZ}	OE# to RCVR Tristate Delay	Figure 1			15	ns
t_{PZD}	Receiver Tristate to Transmit Delay	Figure 1	15			ns
t_{PDZ}	OE# to DRVR Tristate Delay	Figure 1			15	ns
t_{PZV}	Driver Tri-state to Receiver Delay	Figure 1	15			ns
t_{PLH}	V+/V– to D+/D– Propagation Delay	Figure 4			15	ns
t_{PHL}	V+/V– to D+/D– Propagation Delay	Figure 4			15	ns
t_{PLH}	D+/D– to RCV Propagation Delay	Figure 3			15	ns
t_{PHL}	D+/D– to RCV Propagation Delay	Figure 3			15	ns
t_{PLH}	D+/D– to V+/D– Propagation Delay	Figure 3			8	ns
t_{PHL}	D+/D– to V+/D– Propagation Delay	Figure 3			8	ns

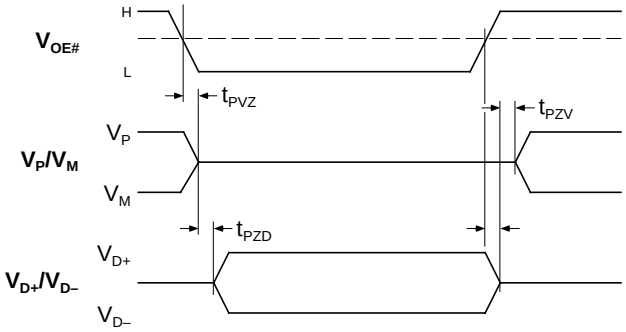


Figure 1. Enable and Disable Times

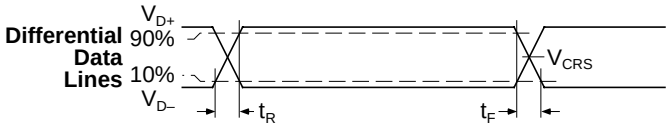


Figure 2. Rise and Fall Times

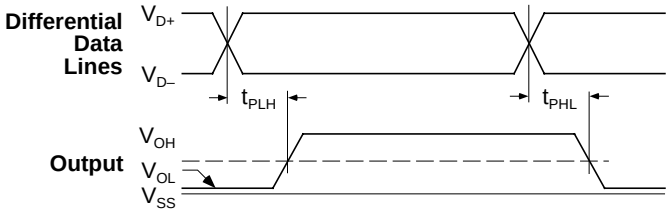


Figure 3. Receiver Propagaion Delay D+/D– to RCV, V_P, and V_M

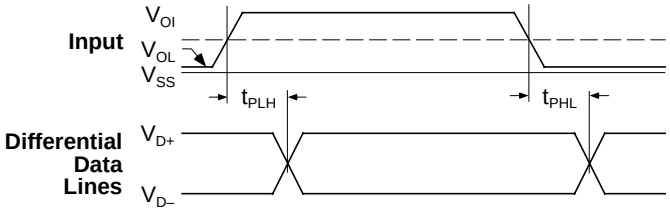
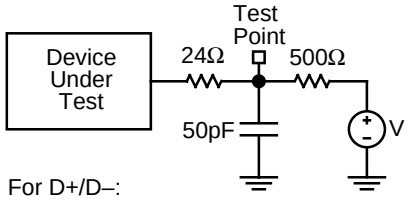


Figure 4. Driver Propagation Delay V_P and V_M to D+/D–

OE# = 0 (Transmit):					
Input		Output			
VP	VM	D+	D–	RCV	Result
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined
OE# = 1 (Receive):					
Input		Output			
D+	D–	VP	VM	RCV	Result
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

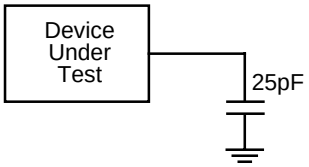
Table 1. Truth Table

Test Circuits

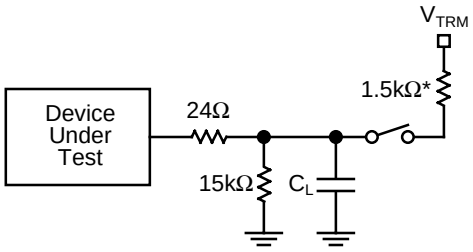


For D+/D–:
$V = 0V$ for t_{PZH} and t_{PHZ}
$V = V_{BUS}$ for t_{PZL} and t_{PLZ}

Load for Enable and Disable Time (D+/D–)



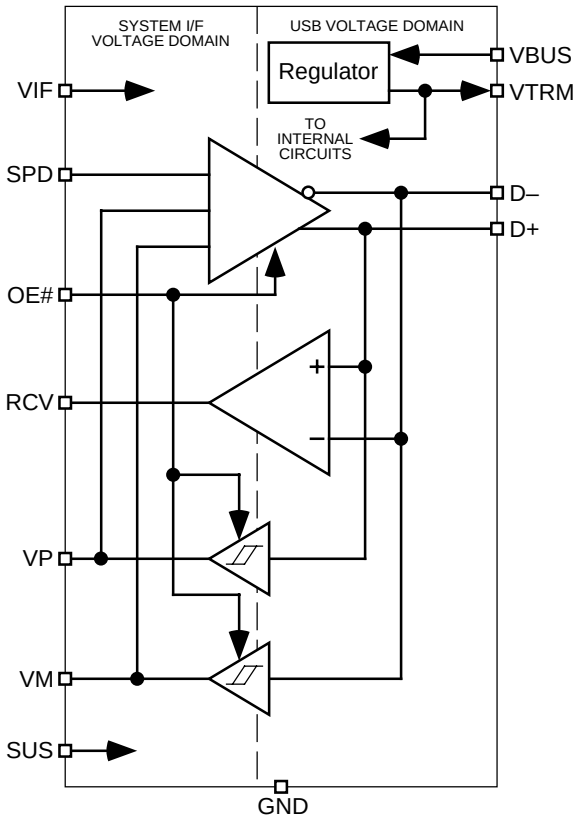
V_P, V_M, and RCV Load



C_L = 50pF, full speed
C_L = 50pF, low speed (minimum timing)
C_L = 600pF, low speed (maximum timing)
*1.5k on D– for low speed or D+ for high speed

D+ and D– Load

Block Diagram



Applications Information

The MIC2550 is designed to provide USB connectivity in mobile systems where system supply voltages are not available to satisfy USB requirements. The MIC2550 can operate down to supply voltages of 2.5V and still meet USB physical layer specifications. As shown in the system diagram, the MIC2550 takes advantage of USB's supply voltage, V_{BUS}, to operate the transceiver. The system voltage, V_{IF}, is used to set the reference voltage used by the digital I/O lines (VP, VM, RCV, OE#, SPD, and SUS pins) interfacing to the system. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the system.

In addition, a 3.3V, 10% termination supply voltage, V_{TRM}, is provided to support speed selection. A 0.47µF (minimum) capacitor from V_{TRM} to ground is required to ensure stability. A 1.5K resistor is required between this pin and the D+ or D– lines to respectively specify full-speed or low-speed operation.

Suspend

When the suspend pin (SUS) is high, power consumption is reduced to a minimum. V_{TRM} is not disabled. RCV, VP and VM are still functional to enable the device to detect USB activity. For minimal current consumption in suspend mode, it is recommended that OE# = 1.

External ESD Protection

The use of ESD transient protection devices is not required for operation, but is recommended.

Nonmultiplexed Bus

To save pin count for the USB logic controller interface, the MIC2550 was designed with V_P and V_M as bidirectional pins. To interface the MIC2550 with a nonmultiplexed data bus, resistors can be used for low cost isolation as shown in Figure 6.

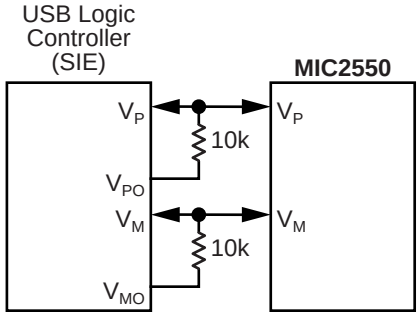
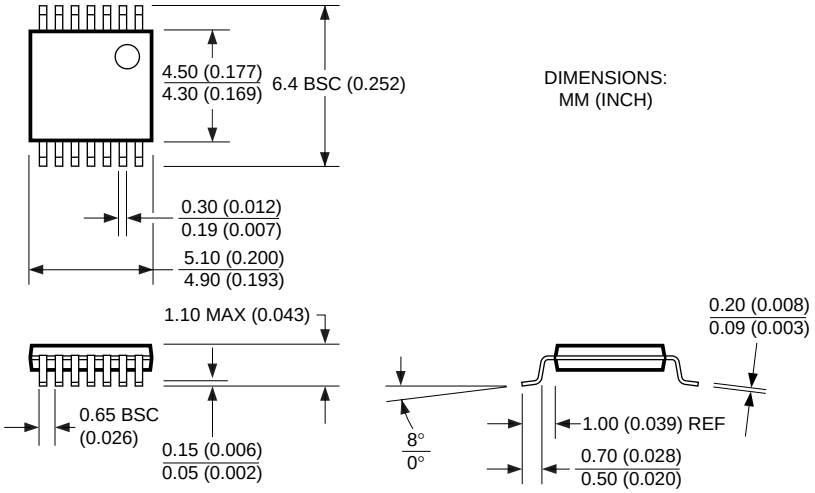


Figure 6. MIC2550 Interface to Nonmultiplexed Data Bus.

Package Information



14-Pin TSSOP (TS)

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