

**FEATURES**

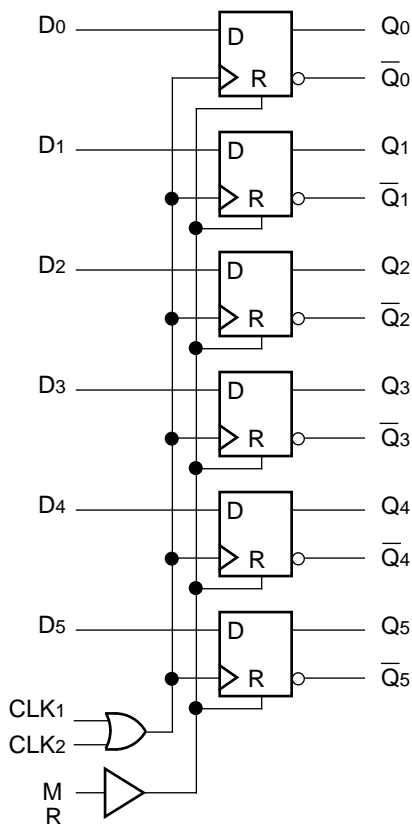
- 1100MHz toggle frequency
- Extended 100E VEE range of -4.2V to -5.46V
- Differential outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E151
- Available in 28-pin PLCC package

**DESCRIPTION**

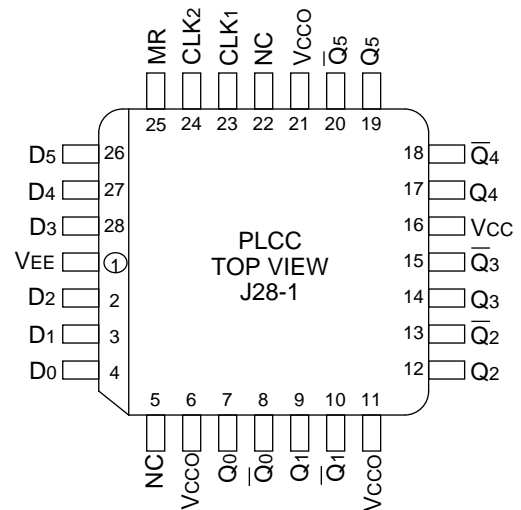
The SY10/100E151 offer 6 edge-triggered, high-speed, master-slave D-type flip-flops with differential outputs, designed for use in new, high-performance ECL systems. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as clocking control for the flip-flops. Data is clocked into the flip-flops on the rising edge of either CLK1 or CLK2 (or both). When both CLK1 and CLK2 are at a logic LOW, data enters the master and is transferred to the slave when either CLK1 or CLK2 (or both) go HIGH.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
D0-D5	Data Inputs
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q5	True Outputs
Q-bar0-Q-bar5	Inverting Outputs
VCCO	Vcc to Output

**TRUTH TABLES<sup>(1)</sup>**

**Asynchronous Operation**

Inputs				Output
Dn	CLK1	CLK2	MR	Qn(t + 1)
X	X	X	H	L

**NOTE:**

- 1. H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- t = Time before positive CLK transition
- t+1 = Time after positive CLK transition
- u = LOW-to-HIGH transition

**Synchronous Operation**

Inputs				Output
Dn	CLK1	CLK2	MR	Qn(t + 1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Qn(t)
X	u	H	L	Qn(t)
X	L	L	L	Qn(t)

**DC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—	
I <sub>EE</sub>	Power Supply Current										mA	—	
		10E	—	65	78	—	65	78	—	65			78
		100E	—	65	78	—	65	78	—	75			90

**AC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCC = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
fMAX	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
tPLH tPHL	Propagation Delay to Output CLK MR	475 475	650 650	800 850	475 475	650 650	800 850	475 475	650 650	800 850	ps	—
ts	Set-up Time, D	0	-175	—	0	-175	—	0	-175	—	ps	—
tH	Hold Time, D	350	175	—	350	175	—	350	175	—	ps	—
tRR	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
tPW	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	65	—	—	65	—	—	65	—	ps	1
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	300	450	700	300	450	700	300	450	700	ps	—

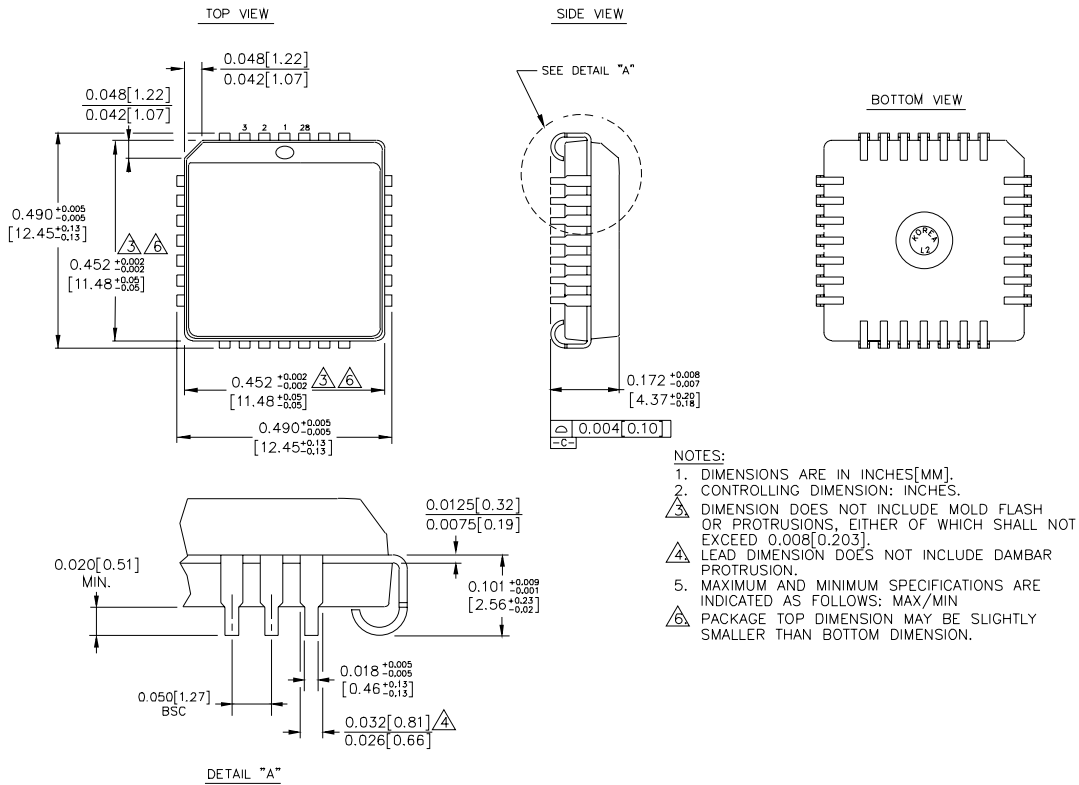
**NOTE:**

1. Within-device skew is defined as identical transitions on similar paths through a device.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10E151JC	J28-1	Commercial
SY10E151JCTR	J28-1	Commercial
SY100E151JC	J28-1	Commercial
SY100E151JCTR	J28-1	Commercial

**28 LEAD PLCC (J28-1)**



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

This information is believed to be accurate and reliable, however no responsibility is assumed by Micrel for its use nor for any infringement of patents or other rights of third parties resulting from its use. No license is granted by implication or otherwise under any patent or patent right of Micrel Inc.

© 2000 Micrel Incorporated