

FEATURES

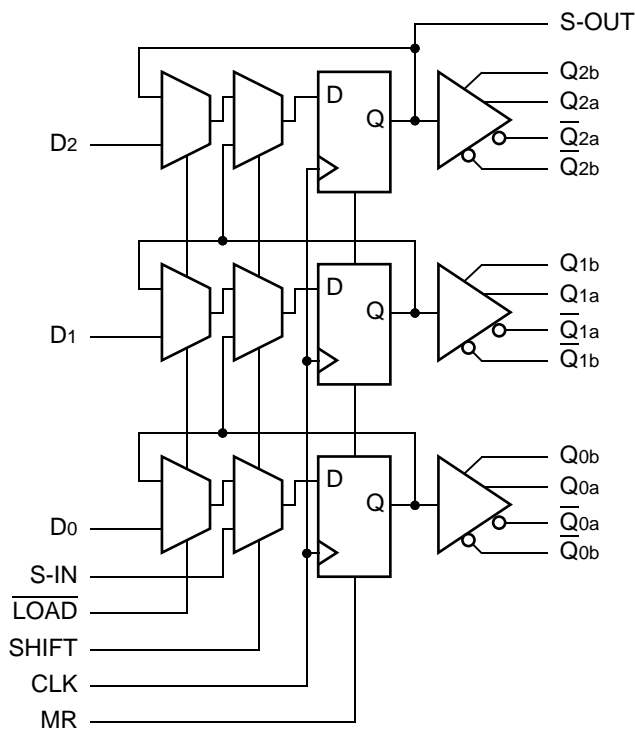
- Scannable version E112 driver
- Extended 100E VEE range of -4.2V to -5.5V
- 1025ps max. CLK to Output
- Dual differential outputs
- Master Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with industry standard 10KH, 100K ECL levels
- Fully compatible with Motorola MC10E/100E212
- Available in 28-pin PLCC package

DESCRIPTION

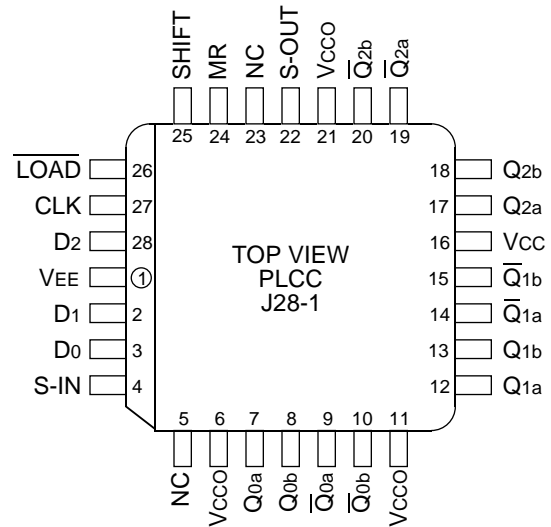
The SY10/100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0 – D2	Data Inputs
S-IN	Scan Input
LOAD	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Master Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
Q̄[0:2]a, Q̄[0:2]b	Inverting Outputs
Vcco	Vcc to Output

TRUTH TABLE

$\overline{\text{LOAD}}$	SHIFT	MR	Mode
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	10E	80	96	—	80	96	—	80	96	mA	—
		100E	80	96	—	80	96	—	92	110		

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR CLK to S-OUT	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	ps	—
t _S	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	SHIFT	150	-50	—	150	-50	—	150	-50	—		
	LOAD	225	50	—	225	50	—	225	50	—		
t _H	Hold Time										ps	—
	D	250	25	—	250	25	—	250	25	—		
	SHIFT	300	100	—	300	100	—	300	100	—		
	LOAD	225	0	—	225	0	—	225	0	—		
t _{RR}	Reset Recovery	600	350	—	600	350	—	600	350	—	ps	—
t _{skew}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	1
t _{skew}	Within-Gate Skew	—	50	—	—	50	—	—	50	—	ps	2
t _r t _f	Rise/Fall Times 20% to 80%	275	425	650	275	425	650	275	425	650	ps	—

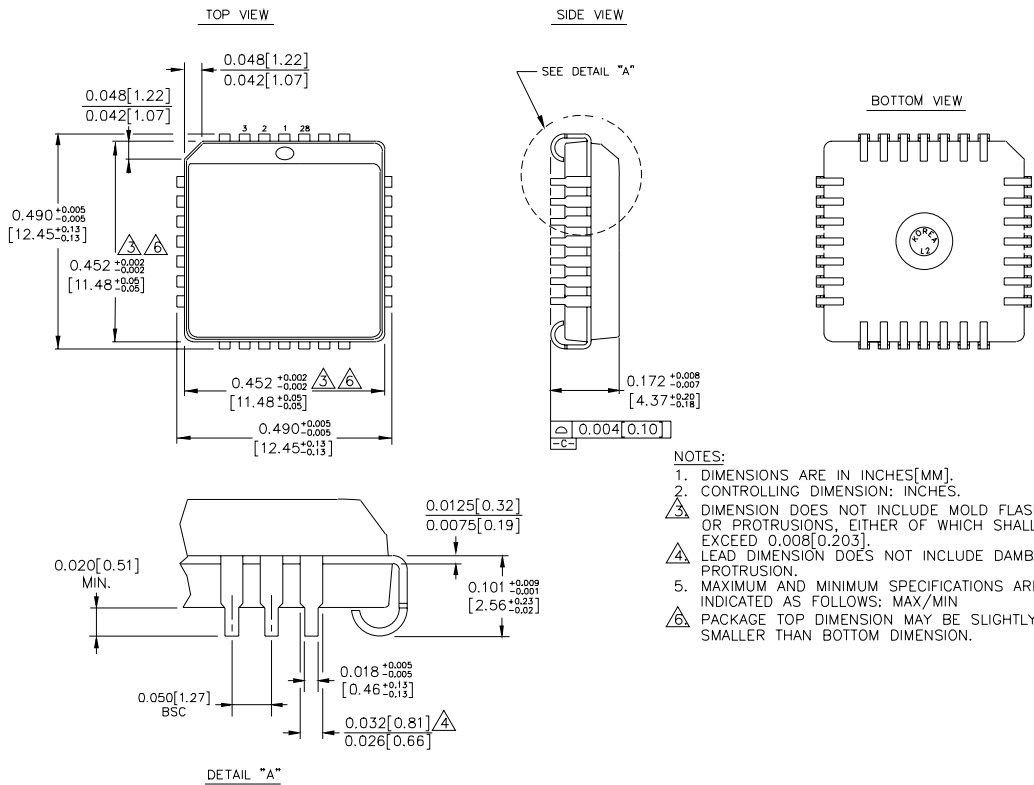
NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E212JC	J28-1	Commercial
SY10E212JCTR	J28-1	Commercial
SY100E212JC	J28-1	Commercial
SY100E212JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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