

FEATURES

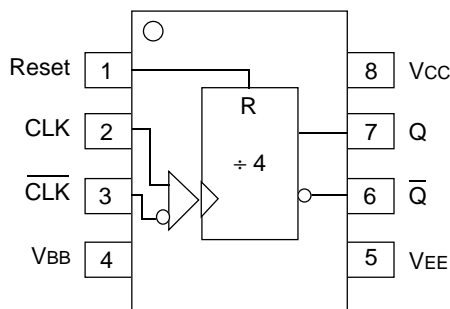
- 3.3V and 5V power supply options
- 650ps propagation delay
- 4.0GHz toggle frequency
- High bandwidth output transistions
- Internal 75KΩ input pull-down resistors
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL33/L are integrated ÷4 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL33/L only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset input allows for the synchronization of multiple EL33/Ls in a system.

PIN CONFIGURATION/BLOCK DIAGRAM

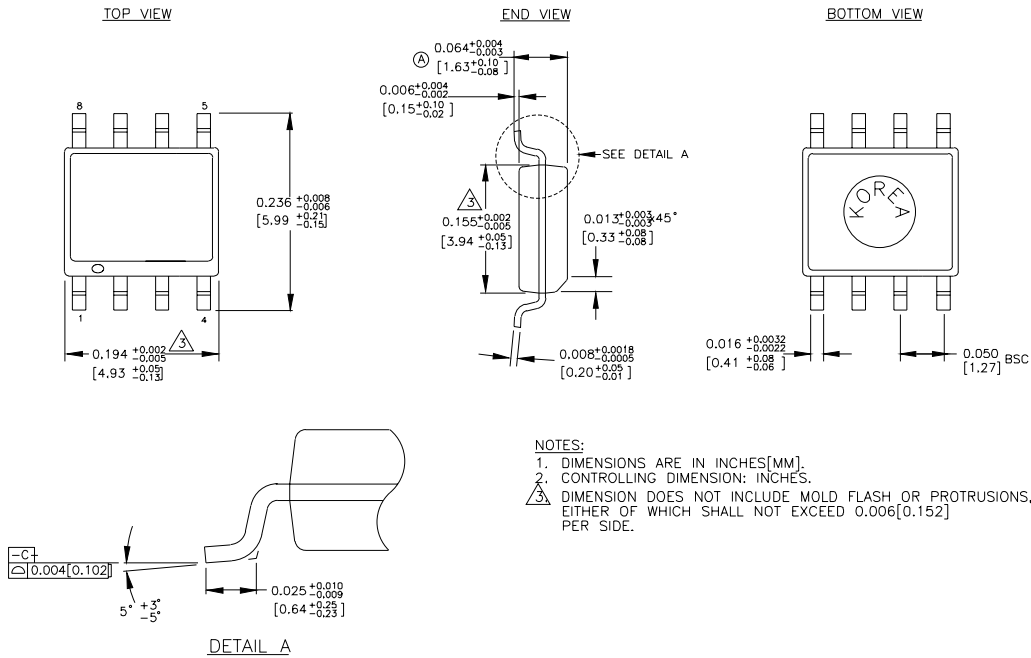


**SOIC
TOP VIEW**

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

8 LEAD SOIC .150" WIDE (Z8-1)



Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

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