SINGLE SUPPLY QUAD PECL-TO-TTL W/LATCHED OUTPUT ENABLE

FEATURES

- **Translates positive ECL to TTL (PECL-to-TTL)**
- **300ps pin-to-pin skew**
- **500ps part-to-part skew**
- **Differential internal design for increased noise immunity and stable threshold inputs**
- **V_{BB} reference output**
- **Single supply**
- **Enable input**
- **Latch enable input**
- **Extra TTL and ECL power/ground pins to reduce cross-talk/noise**
- **High drive capability: 24mA each output**
- **Fully compatible with industry standard 10K, 100K I/O levels**
- **Available in 16-pin SOIC package**

DESCRIPTION

The SY10/100H841 are single supply, low skew translating 1:4 clock drivers.

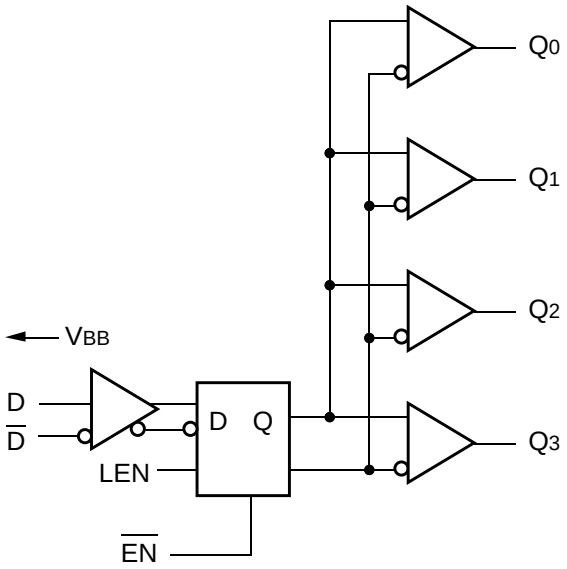
The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

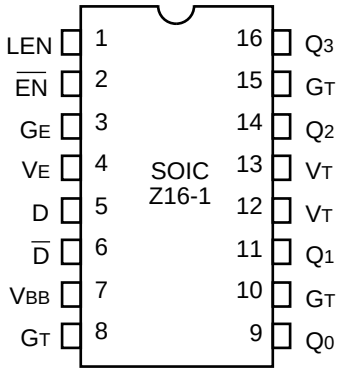
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H841 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
G_T	TTL Ground (0V)
V_T	TTL V_{CC} (+5.0V)
V_E	ECL V_{CC} (+5.0V)
G_E	ECL Ground (0V)
D, $\overline{D}$	Signal Input (PECL)
V_{BB}	V_{BB} Reference Output (PECL)
Q_0 - Q_3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (PECL)
LEN	Latch Enable Input

Rev.: F Amendment: /0
Issue Date: May, 1999

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_E (ECL) V_T (TTL)	Power Supply Voltage	–0.5 to +7.0 –0.5 to +7.0	V
V_I (ECL) V_{OUT} (TTL)	Input Voltage	0.0 to V_{EE} 0.0 to V_T	V
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{EN}$	Enable Input (PECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output (PECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

V_{CC} AND C_{LOAD}

Ranges to meet duty cycle requirement: 0°C ≤ T_A ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 40MHz	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 50MHz	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	V_{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS[1]

$V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	—
V_{IH}	Input HIGH Voltage	3.830	4.160	3.870	4.190	3.940	4.280	V	V_E = 5.0V
V_{IL}	Input LOW Voltage	3.050	3.520	3.050	3.520	3.050	3.555	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.620	3.730	3.650	3.750	3.690	3.810	V	V_E = 5.0V

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

100H ECL DC ELECTRICALCHARACTERISTICS[1]

$V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	V_E = 5.0V
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.620	3.740	3.620	3.740	3.620	3.740	V	V_E = 5.0V

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skew++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skew--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5,6)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF
—	Pulse Width	Q_0–Q_3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q_0–Q_3	1.0	—	1.0	—	1.0	—	ns	—
t_S	Set-up Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, EN	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—

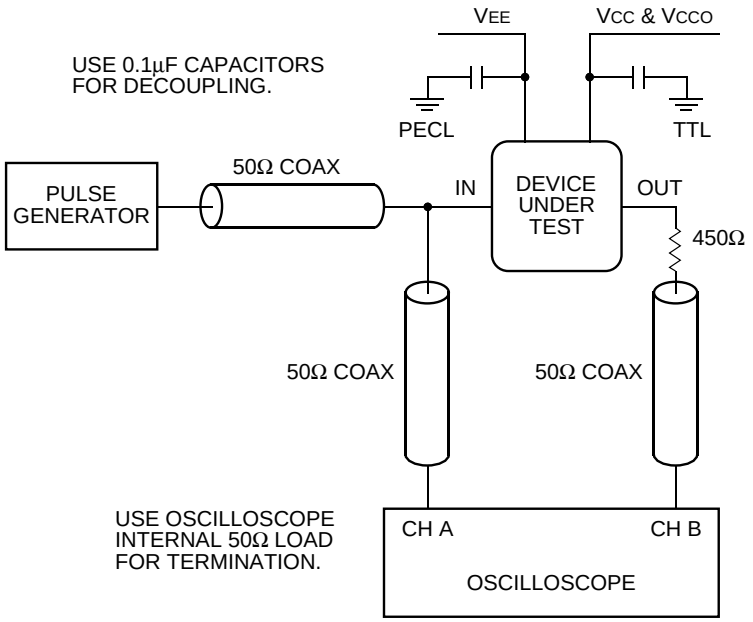
NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet at 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

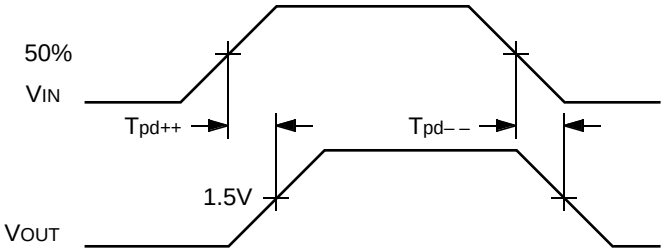
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H841ZC	Z16-1	Commercial
SY10H841ZCTR	Z16-1	Commercial
SY100H841ZC	Z16-1	Commercial
SY100H841ZCTR	Z16-1	Commercial

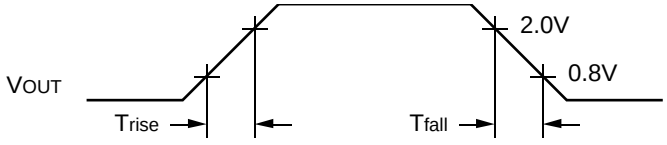
TTL SWITCHING CIRCUIT



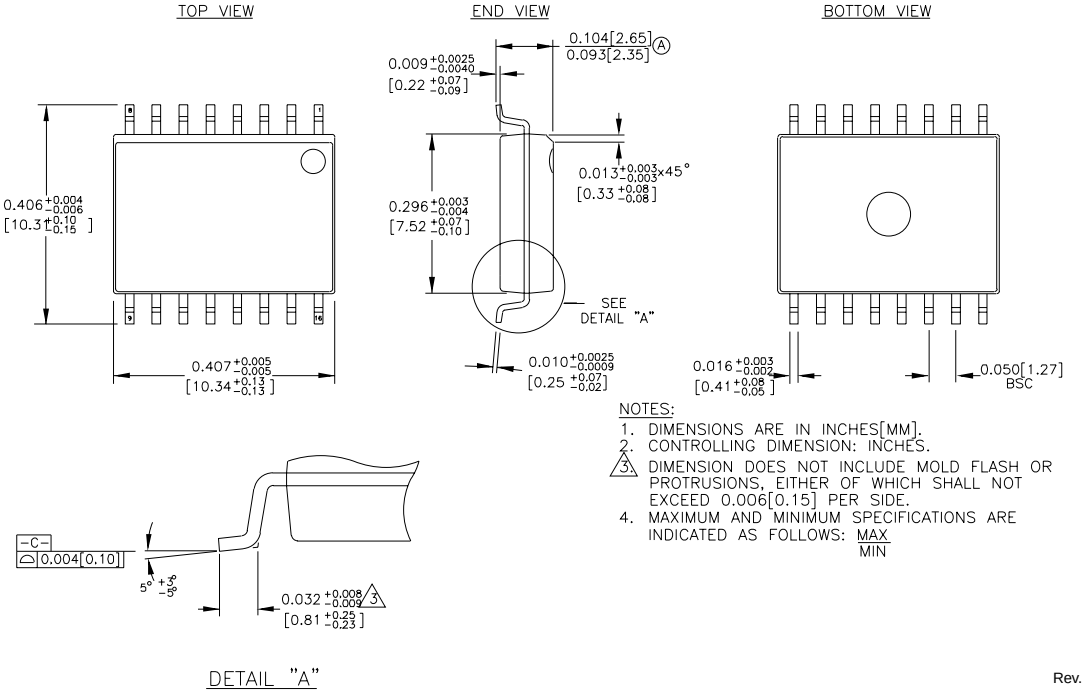
ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



16 LEAD SOIC .300" WIDE (Z16-1)



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