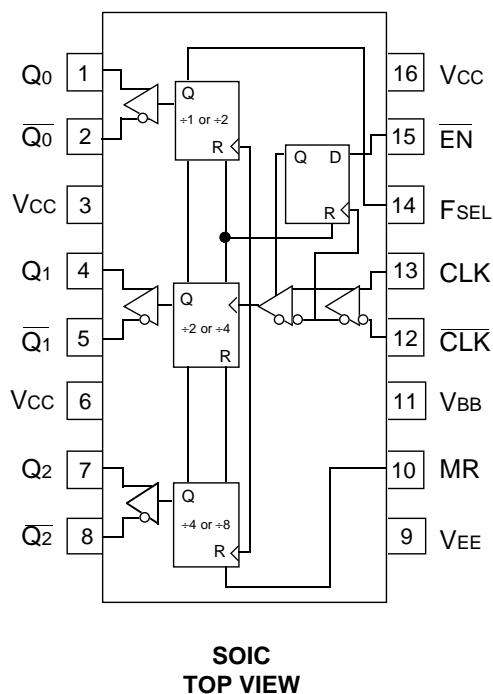


## FEATURES

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- Available in 16-pin SOIC package

## PIN CONFIGURATION/BLOCK DIAGRAM



## PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
FSEL	Function Select
EN	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q0	Differential ÷1 or ÷2 Outputs
Q1	Differential ÷2 or ÷4 Outputs
Q2	Differential ÷4 or ÷8 Outputs

## DESCRIPTION

The SY100S834/L is low skew (÷1, ÷2, ÷4) or (÷2, ÷4, ÷8) clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01μF capacitor. The VBB output is designed to act as the switching reference for the input of the SY100S834/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The Function Select (FSEL) input is used to determine what clock generation chip function is. When FSEL input is LOW, SY100S834/L functions as a divide by 2, by 4 and by 8 clock generation chip. However, if FSEL input is HIGH, it functions as a divide by 1, by 2 and by 4 clock generation chip. This latter feature will increase the clock frequency by two folds.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple SY100S834/Ls in a system.

## TRUTH TABLE

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0-2
X	X	H	Reset Q0-2

### NOTES:

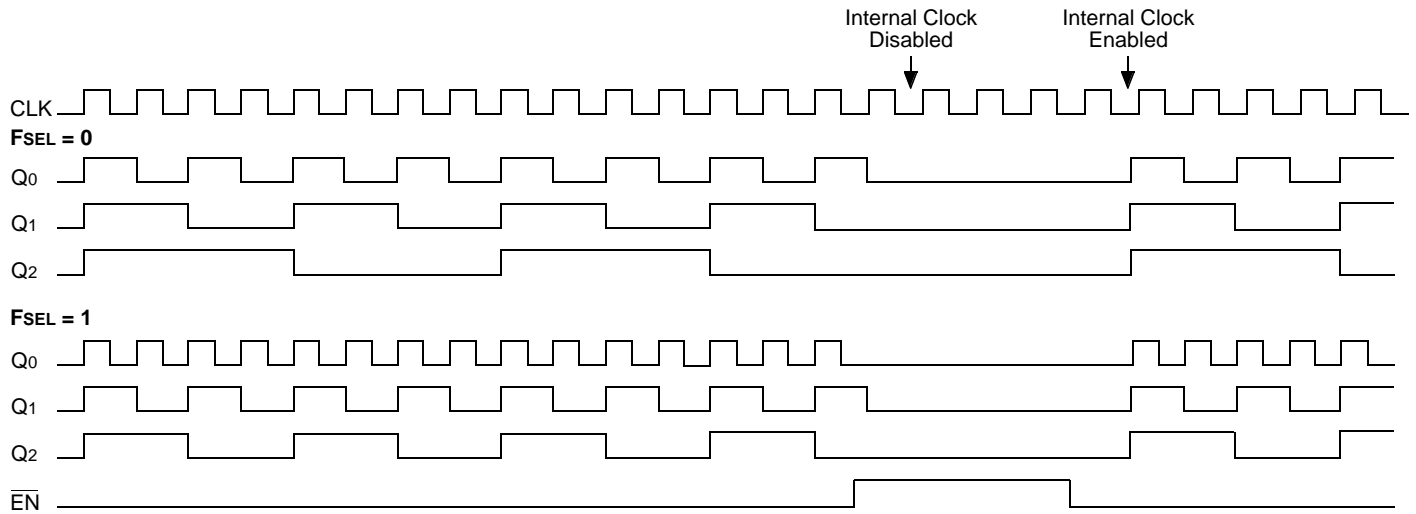
Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

FSEL	Q0 Outputs	Q1 Outputs	Q2 Outputs
L	Divide by 2	Divide by 4	Divide by 8
H	Divide by 1	Divide by 2	Divide by 4



**TIMING DIAGRAM**



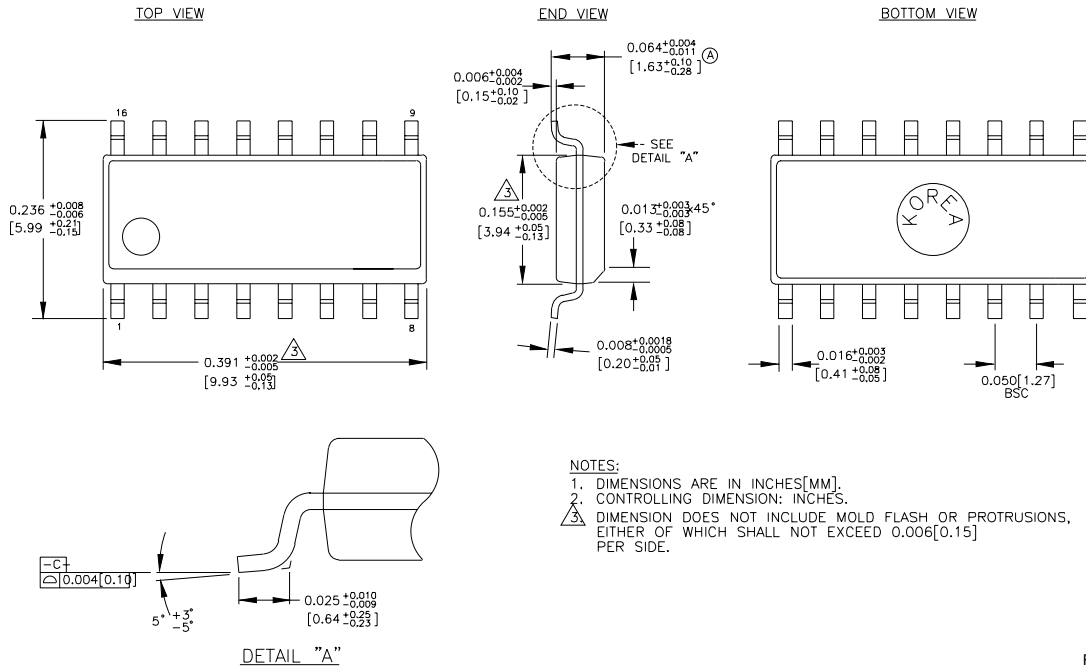
The  $\overline{EN}$  signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the  $\overline{EN}$  signal not been asserted.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range	VEE Range (V)
SY100S834ZC	Z16-2	Commercial	-4.2 to -5.5
SY100S834ZCTR	Z16-2	Commercial	-4.2 to -5.5
SY100S834LZC	Z16-2	Commercial	-3.0 to -3.8
SY100S834LZCTR	Z16-2	Commercial	-3.0 to -3.8

Ordering Code	Package Type	Operating Range	VEE Range (V)
SY100S834ZI	Z16-2	Industrial	-4.2 to -5.5
SY100S834ZITR	Z16-2	Industrial	-4.2 to -5.5
SY100S834LZI	Z16-2	Industrial	-3.0 to -3.8
SY100S834LZITR	Z16-2	Industrial	-3.0 to -3.8

**16 LEAD SOIC .150" WIDE (Z16-2)**



Rev. 02

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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