

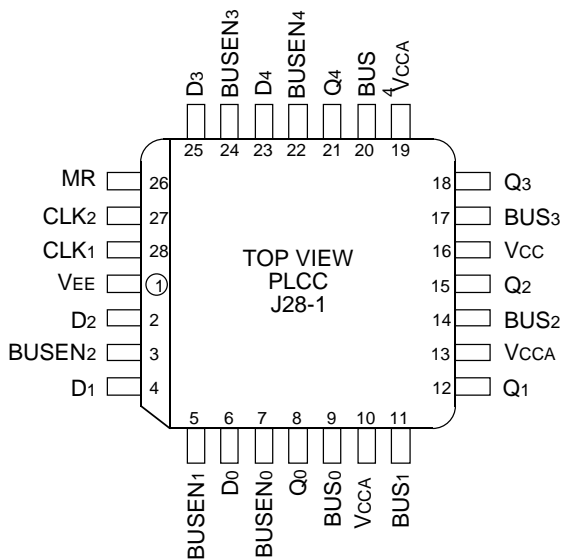
**FEATURES**

- 25Ω cut-off bus outputs
- 50Ω receiver outputs
- Transmit and receive registers with separate clocks
- 1500ps max. delay from CLK1 to Bus Outputs (BUS)
- 1500ps max. delay from CLK2 to Receiver Outputs (Q)
- Individual bus enable pins
- Internal 75KΩ input pull-down resistors
- Voltage and temperature compensation for improved noise immunity
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Available in 28-pin PLCC package

**DESCRIPTION**

The SY100S891 is a 5-bit registered transceiver containing five bus transceivers with both transmit and receive registers. The bus outputs (BUS<sub>0</sub> – BUS<sub>4</sub>) are specified for driving a 25 ohm bus and the receive outputs (Q<sub>0</sub> – Q<sub>4</sub>) are specified for driving a 50 ohm line. The bus outputs have a normal high level output voltage and a normal low level output voltage when the bus enable (BUSEN<sub>0</sub> – BUSEN<sub>4</sub>) is high. However, the output is switched to a cut-off level when a bus-enable is low. This cut-off level is sufficiently low that a relatively high impedance is presented to the bus in order to minimize reflections. There is one bus-enable for each bus driver; a clock (CLK<sub>1</sub>) which is common to all five bus driver registers; and a separate clock (CLK<sub>2</sub>) which is common to all five receive registers. Data at the D inputs is clocked to the Bus register by a positive transition of CLK<sub>1</sub> and data on the bus is clocked into the Receiver register by a positive transition of CLK<sub>2</sub>. A high on the Master Reset clears all registers.

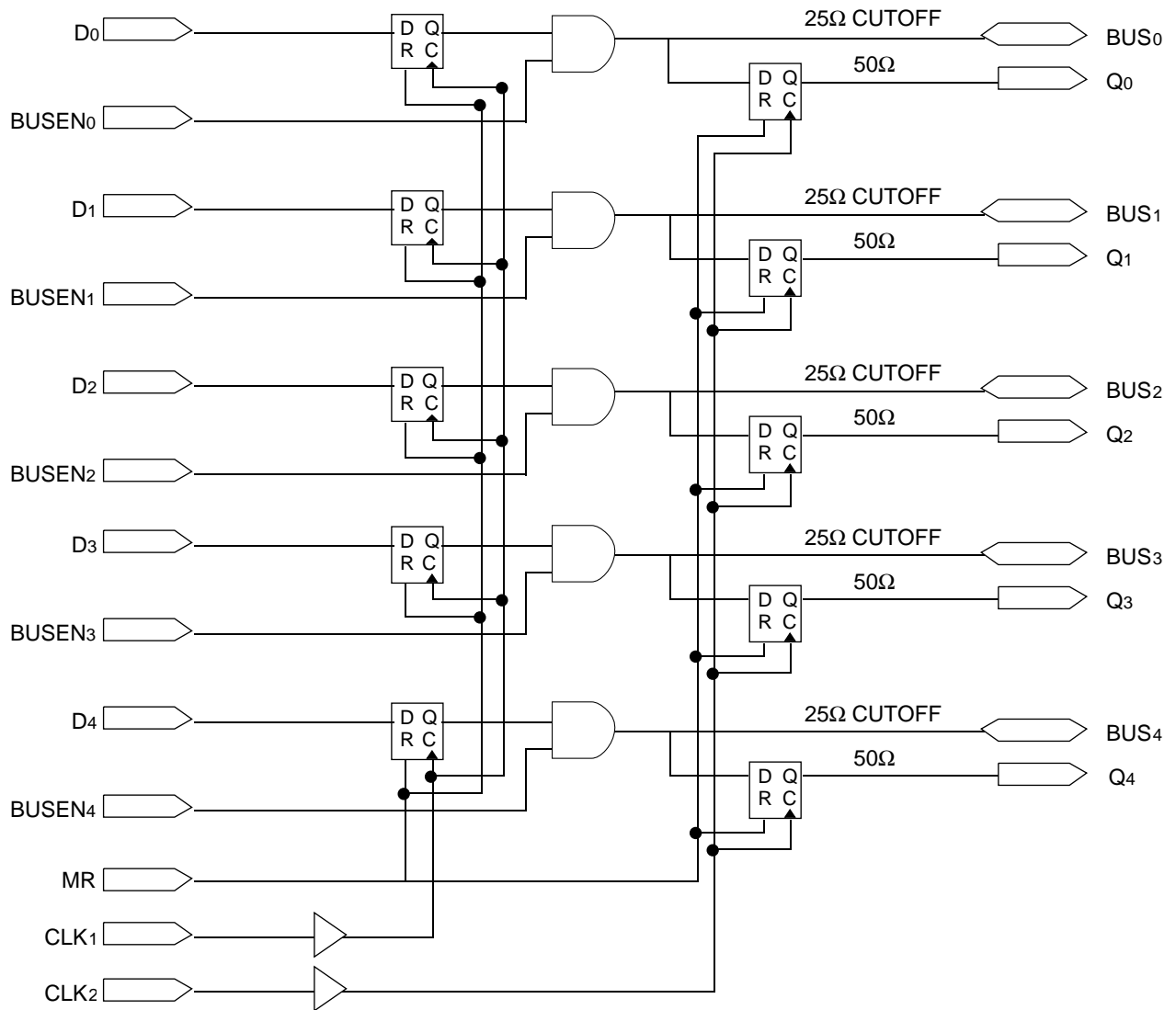
**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
BUSEN <sub>0-4</sub>	Bus Enable Inputs
D <sub>0</sub> – D <sub>4</sub>	Data Inputs
CLK <sub>1</sub>	Bus Driver Clock Input
CLK <sub>2</sub>	Receive Register Clock
MR	Master Reset
Q <sub>0</sub> – Q <sub>4</sub>	Bus Receive Outputs
BUS <sub>0-4</sub>	Bus Outputs

**BLOCK DIAGRAM**



**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V <sub>CUT</sub>	Cut-off Bus Output Voltage	-2200	-2160	-2100	mV	$V_{IN} = V_{IH} (Max.)$ or $V_{IL} (Min.)$	Loading with $25\Omega$ to $-2.20V$
V <sub>OH</sub>	Output HIGH Voltage Bus	-1025	-955	-880	mV	$V_{IN} = V_{IH} (Max.)$ or $V_{IL} (Min.)$	Loading with $25\Omega$ to $-2.0V$
V <sub>OL</sub>	Output LOW Voltage Bus	-1810	-1705	-1620	mV		
V <sub>OHA</sub>	Output HIGH Voltage Bus	-1035	—	—	mV	$V_{IN} = V_{IH} (Min.)$ or $V_{IL} (Max.)$	
V <sub>OLA</sub>	Output LOW Voltage Bus	—	—	-1610	mV		
V <sub>OH</sub>	Output HIGH Voltage Receiver	-1025	-955	-880	mV	$V_{IN} = V_{IH} (Max.)$ or $V_{IL} (Min.)$	Loading with $50\Omega$ to $-2.0V$
V <sub>OL</sub>	Output LOW Voltage Receiver	-1810	-1705	-1620	mV		
V <sub>OHA</sub>	Output HIGH Voltage Receiver	-1035	—	—	mV	$V_{IN} = V_{IH} (Min.)$ or $V_{IL} (Max.)$	
V <sub>OLA</sub>	Output LOW Voltage Receiver	—	—	-1610	mV		
V <sub>IH</sub>	Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.5	—	—	$\mu A$	$V_{IN} = V_{IL} (Min.)$	
I <sub>IH</sub>	Input High Current	—	—	150	$\mu A$	$V_{IN} = V_{IH} (Max.)$	
I <sub>EE</sub>	Power Supply Current	-216	—	—	mA	Inputs Open	
C <sub>IN</sub>	Input Pin Capacitance	—	4	—	pF		
C <sub>OUT</sub>	Output Pin Capacitance	—	5	—	pF		

## AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay <sup>(1)</sup> CLK1 to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
tPLH tPHL	Propagation Delay <sup>(2)</sup> CLK2 to Q	500	800	1200	500	800	1200	500	800	1200	ps	
tPLH tPHL	Propagation Delay <sup>(1)</sup> BUSEN to Bus	500	800	1200	500	800	1200	500	800	1200	ps	
tPLH tPHL	Propagation Delay <sup>(1)</sup> Master Reset to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
tPLH tPHL	Propagation Delay <sup>(2)</sup> Master Reset to Q	500	800	1200	500	800	1200	500	800	1200	ps	
tS	Set-up Time Bus Wrt CLK2 D Wrt CLK1	—	—	400	—	—	400	—	—	400	ps	
		—	—	400	—	—	400	—	—	400		
tREL	Master Reset Release Time	—	—	1000	—	—	1000	—	—	1000	ps	
tH	Hold Time Bus Wrt CLK2 D Wrt CLK1	—	—	400	—	—	400	—	—	400	ps	
		—	—	400	—	—	400	—	—	400		
tr	Output Rise Time Bus <sup>(3)</sup> Q <sup>(4)</sup>	500	—	1000	500	—	1000	500	—	1000	ps	
		300	—	900	300	—	900	300	—	900		
tf	Output Fall Time Bus <sup>(3)</sup> Q <sup>(4)</sup>	500	—	1000	500	—	1000	500	—	1000	ps	
		300	—	900	300	—	900	300	—	900		
tskew	Skew (Maximum difference between slowest and fastest path)	—	100	—	—	100	—	—	100	—	ps	

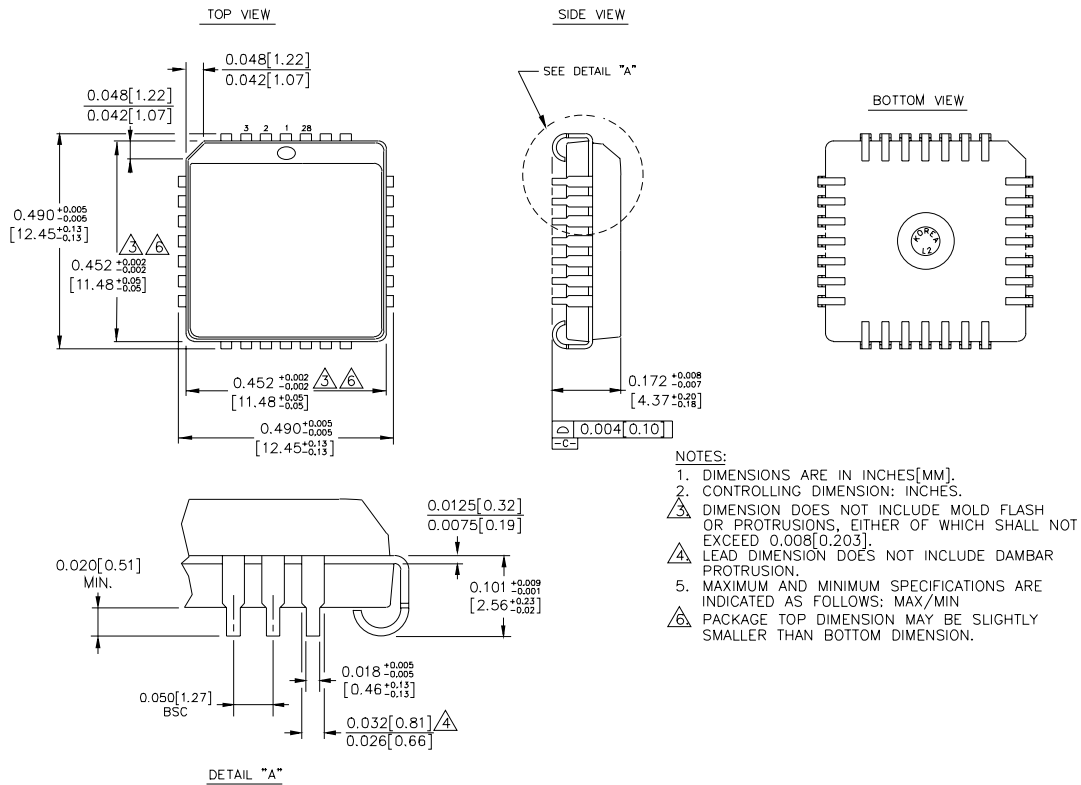
### NOTES:

1. Loaded with  $25\Omega$  to  $-2.0V$
2. Loaded with  $50\Omega$  to  $-2.0V$
3.  $25\Omega$  Load
4.  $50\Omega$  Load

## PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S891JC	J28-1	Commercial
SY100S891JCTR	J28-1	Commercial

**28 LEAD PLCC (J28-1)**



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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