5V/3.3V 32-1250Mbps AnyRate™ CLOCK AND DATA RECOVERY

SY87701V

FEATURES

- **3.3V and 5V power supply options**
- **Clock and data recovery from 32Mbps up to 1.25Gbps NRZ data stream**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications for applications such as OC-1, OC-3, OC-12, ATM, FDDI, etc.**
- **Two on-chip PLLs: one for clock generation and another for clock recovery**
- **Selectable reference frequencies**
- **Differential PECL high-speed serial I/O**
- **Line receiver input: no external buffering needed**
- **Link fault indication**
- **100K ECL compatible I/O**
- **Available in 28-pin SOIC and 32-pin EP-TQFP packages**

DESCRIPTION

The SY87701V is a complete Clock Recovery and Data Retiming integrated circuit for data rates from 32Mbps up to 1.25Gbps NRZ. The device is ideally suited for SONET/SDH/ATM and Fibre Channel applications and other high-speed data transmission systems.

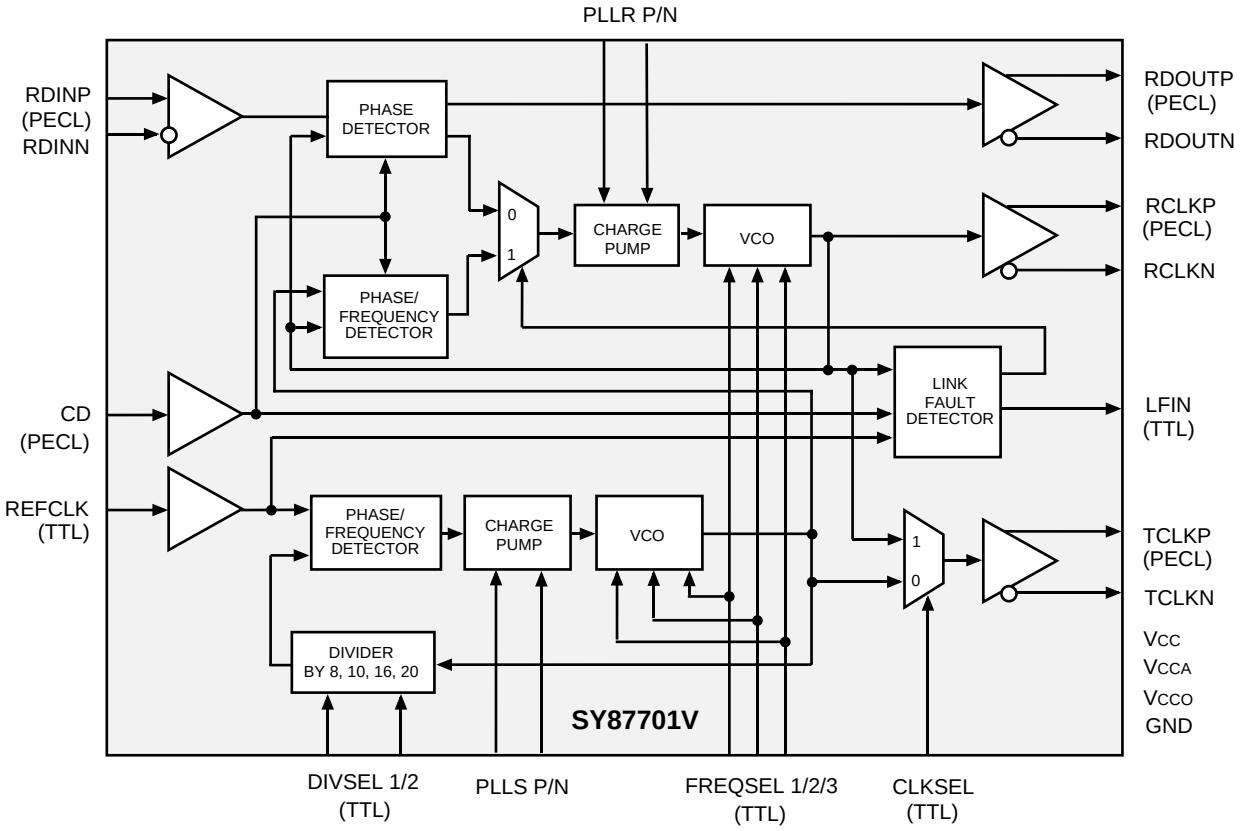
Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

The SY87701V also includes a link fault detection circuit.

APPLICATIONS

- **SONET/SDH/ATM OC-1, OC-3, OC-12, OC-24**
- **Fibre Channel, Escon**
- **Gigabit Ethernet/Fast Ethernet**
- **Proprietary architecture up to 1.25Gbps**

BLOCK DIAGRAM



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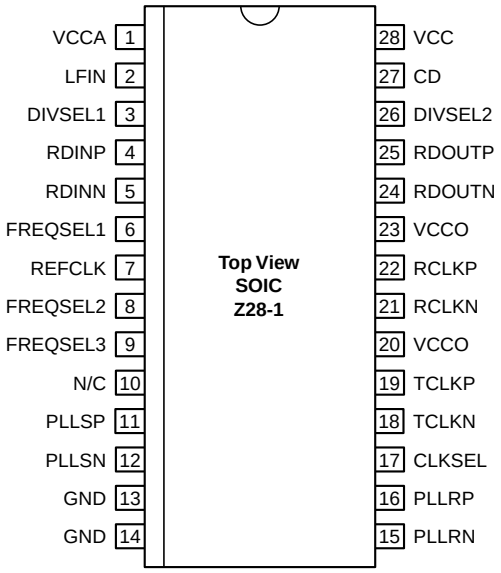
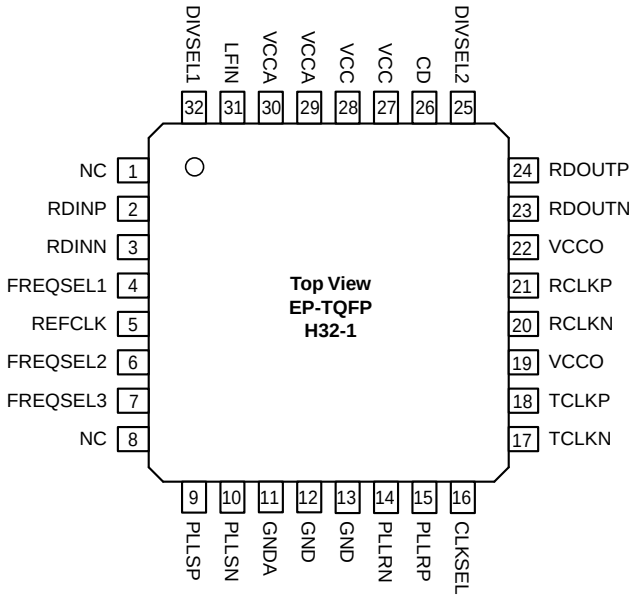
Rev.: H Amendment: /0
Issue Date: September 2000

PIN CONFIGURATION





PIN DESCRIPTIONS

INPUTS

RDINP, RDINN [Serial Data Input] Differential PECL.

These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of eight frequency ranges depending on the state of the FREQSEL pins. See “Frequency Selection” Table.

REFCLK [Reference Clock] TTL input.

This input is used as the reference for the internal frequency synthesizer and the “training” frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs.

CD [Carrier Detect] PECL Input.

This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to lock onto the clock frequency generated from REFCLK.

FREQSEL1, ..., FREQSEL3 [Frequency Select] TTL Inputs.

These inputs select the output clock frequency range as shown in the “Frequency Selection” Table.

DIVSEL1, DIVSEL2 [Divider Select] TTL Inputs.

These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” Table.

CLKSEL [Clock Select] TTL Input.

This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.

OUTPUTS

LFIN [Link Fault Indicator] TTL Output.

This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000ppm). LFIN is an asynchronous output.

RDOUTP, RDOUTN [Receive Data Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent the recovered data from the input data stream (RDIN). This recovered data is sampled on the rising edge of RCLK.

RCLKP, RCLKN [Clock Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent the recovered clock used to sample the recovered data (RDOUT).

TCLKP, TCLKN [Clock Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).

PLLSP, PLLSN [Clock Synthesis PLL Loop Filter]

External loop filter pins for the clock synthesis PLL.

PLLRP, PLLRN [Clock Recovery PLL Loop Filter]

External loop filter pins for the receiver PLL.

POWER & GROUND

VCC	Supply Voltage(1)
VCCA	Analog Supply Voltage(1)
VCCO	Output Supply Voltage(1)
GND	Ground
N/C	No Connect

NOTE:

1. V_{CC}, V_{CCA}, V_{CCO} must be the same value.

FUNCTIONAL DESCRIPTION

Clock Recovery

Clock Recovery, as shown in the block diagram generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30µs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

Lock Detect

The SY87701V contains a link fault indication circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than approximately 1000ppm, the PLL will be declared out of lock. The lock detect circuit will pull the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 1000ppm, the PLL will be declared in lock and the lock detect output will go active.

CHARACTERISTICS

Performance

The SY87701V PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

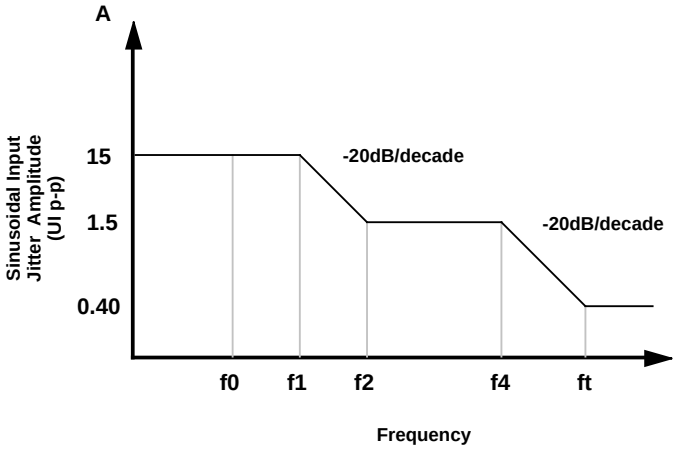
Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1dB optical/electrical power penalty. SONET input jitter tolerance requirement condition is the input jitter amplitude which causes an equivalent of 1dB power penalty.

Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 2.

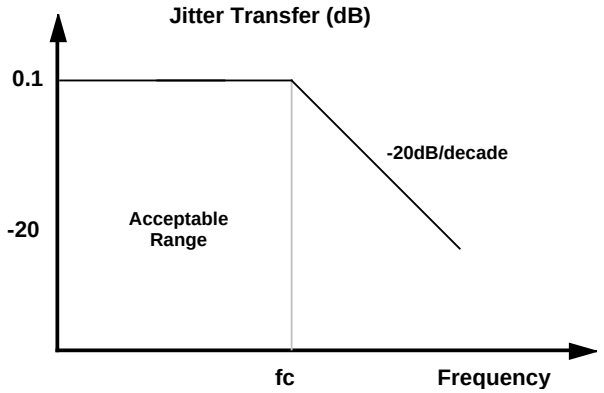
Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. rms when a serial data input with no jitter is presented to the serial data inputs.



OC/STS-N Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
3	10	30	300	6.5	65
12	10	30	300	25	250

Figure 1. Input Jitter Tolerance



OC/STS-N Level	fc (kHz)	P (dB)
3	130	0.1
12	225	0.1

Figure 2. Jitter Transfer

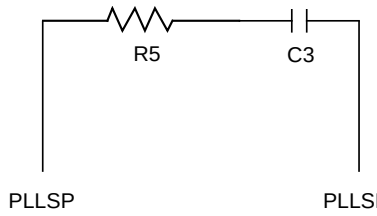
FREQUENCY SELECTION TABLE

FREQSEL1	FREQSEL2	FREQSEL3	f_{VCO}/f_{RCLK}	f_{RCLK} Data Rates (Mbps)
0	0	0	1	750 – 1250
0	0	1	2	375 – 625
0	1	0	4	188 – 313
0	1	1	6	125 – 208
1	0	0	8	94 – 157
1	0	1	12	63 – 104
1	1	0	16	47 – 78
1	1	1	24	32 – 52

REFERENCE FREQUENCY SELECTION

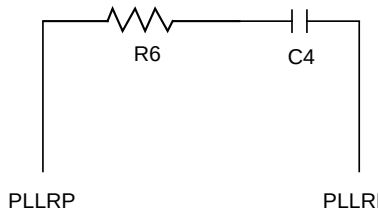
DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

LOOP FILTER COMPONENTS(1)



SONET
R5 = 80Ω
C3 = 1.5µF (X7R Dielectric)

Wide Range
R5 = 350Ω
C3 = 0.47µF (X7R Dielectric)



SONET
R6 = 50Ω
C4 = 1.0µF (X7R Dielectric)

Wide Range
R6 = 680Ω
C4 = 0.47µF (X7R Dielectric)

NOTE:
1. Suggested Values. Values may vary for different applications.

ABSOLUTE MAXIMUM RATINGS(1, 2)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC}	V
I_{OUT}	Output Current –Continuous –Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +85	°C
θ_{JA}	Thermal Resistance @still air	80 single layer board, 46 multi-layer	°C/W

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Airflow of 500LFPM recommended.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.15 4.75	3.3 5.0	3.45 5.25	V V	
I_{CC}	Power Supply Current	—	170	230	mA	

PECL 100K DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{CC} - 1.165	—	V_{CC} - 0.880	V	
V_{IL}	Input LOW Voltage	V_{CC} - 1.810	—	V_{CC} - 1.475	V	
I_{IL}	Input LOW Current	0.5	—	—	µA	$V_{IN} = V_{IL}$(Min.)
V_{OH}	Output HIGH Voltage	V_{CC} - 1.075	—	V_{CC} - 0.830	V	50Ω to V_{CC} –2V
V_{OL}	Output LOW Voltage	V_{CC} - 1.860	—	V_{CC} - 1.570	V	50Ω to V_{CC} –2V

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to +85°C

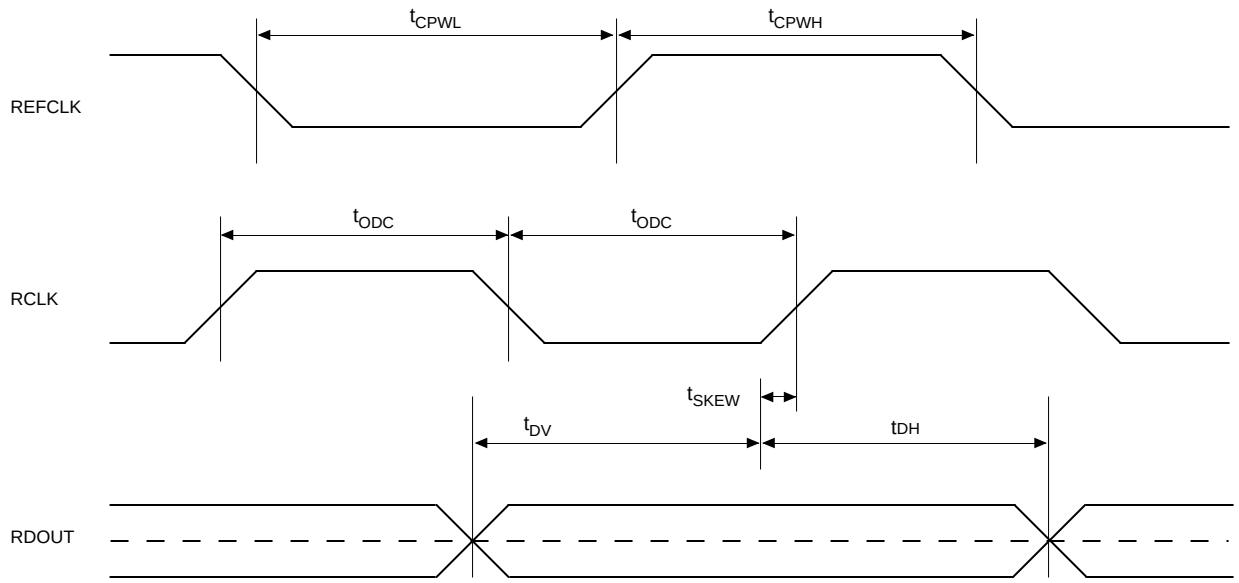
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	–175 —	— —	— +100	µA µA	V_{IN} = 2.7V, V_{CC} = Max. $V_{IN} = V_{CC}$, V_{CC} = Max.
I_{IL}	Input LOW Current	–300	—	—	µA	V_{IN} = 0.5V, V_{CC} = Max.
V_{OH}	Output HIGH Voltage	2.0	—	—	V	I_{OH} = –0.4mA
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 4mA
I_{OS}	Output Short Circuit Current	15	—	100	mA	V_{OUT} = 0V (maximum 1sec)

AC ELECTRICAL CHARACTERISTICS

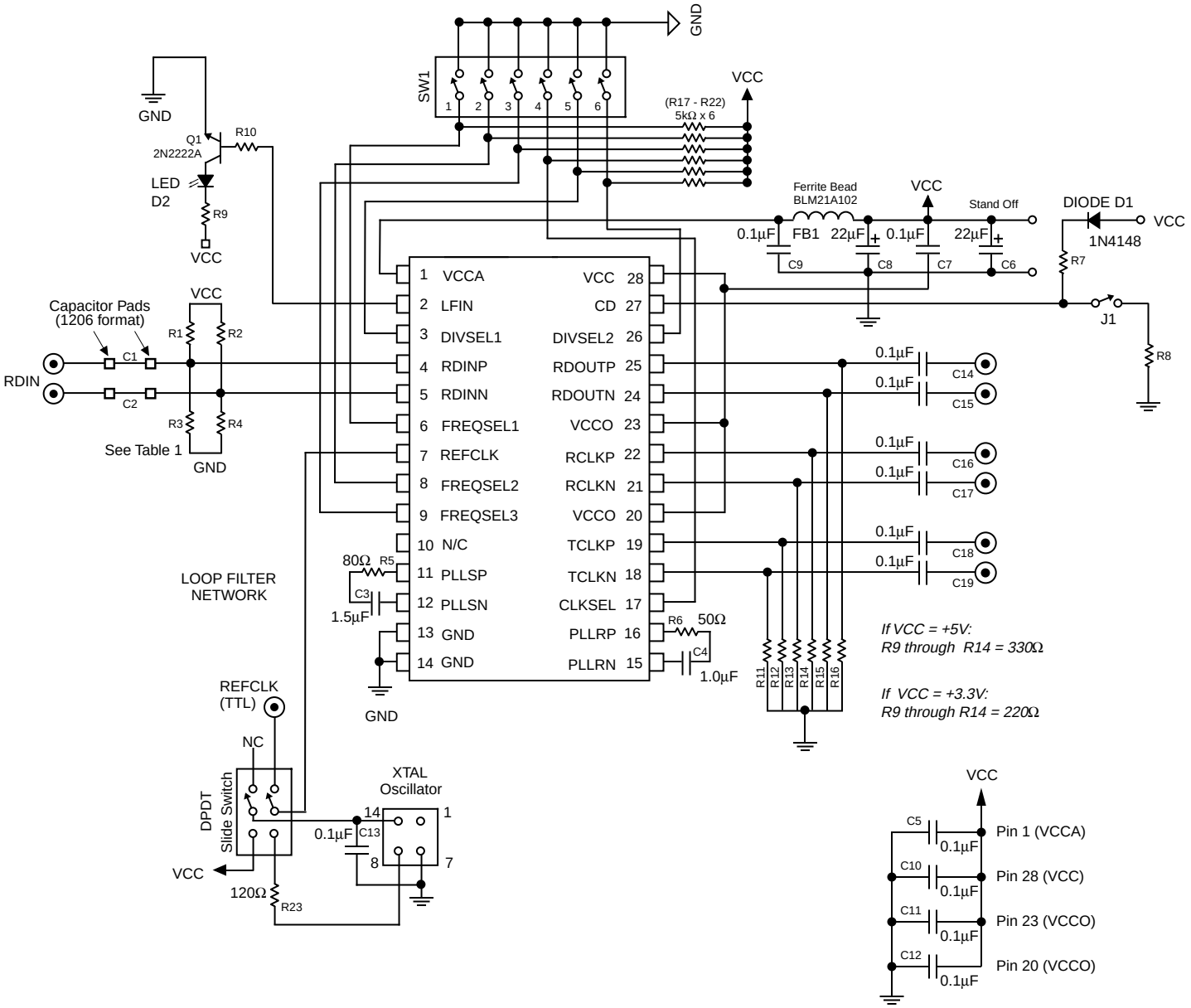
$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{VCO}	VCO Center Frequency	750	—	1250	MHz	f_{REFCLK} * Byte Rate
Δf_{VCO}	VCO Center Frequency Tolerance	—	5	—	%	Nominal
t_{ACQ}	Acquisition Lock Time	—	—	15	µs	
t_{CPWH}	REFCLK Pulse Width HIGH	4	—	—	ns	
t_{CPWL}	REFCLK Pulse Width LOW	4	—	—	ns	
t_{ir}	REFCLK Input Rise Time	—	0.5	2	ns	
t_{ODC}	Output Duty Cycle (RCLK/TCLK)	45	—	55	% of UI	
t_r, t_f	ECL Output Rise/Fall Time	100	—	500	ps	50Ω to V_{CC} –2 (20% to 80%)
t_{skew}	Recovered Clock Skew	–200	—	+200	ps	
t_{DV}	Data Valid	$1/(2*f_{RCLK}) - 200$	—	—	ps	
t_{DH}	Data Hold	$1/(2*f_{RCLK}) - 200$	—	—	ps	

TIMING WAVEFORMS



APPLICATION EXAMPLE



NOTE:

1. C5 and C10–C12 are decoupling capacitors and should be kept as close to the power pins as possible.

For AC coupling only		For DC mode only	
when VCC = +5V	*when VCC = +3.3V*	*when VCC = +5V*	*when VCC = +3.3V*
C1 = C2 = 0.1µF	C1 = C2 = 0.1µF	C1 = C2 = Shorted	C1 = C2 = Shorted
R1 = R2 = 1.2kΩ	R1 = R2 = 680Ω	R1 = R2 = 82Ω	R1 = R2 = 130Ω
R3 = R4 = 3.4kΩ	R3 = R4 = 1kΩ	R3 = R4 = 130Ω	R3 = R4 = 82Ω

Table 1.

Material List

For Bypass and AC coupling capacitor, high quality factor (High Q) capacitors are recommended. This will optimize the performance of the device in high frequency domain. The suggested dielectric characteristics for these capacitors are NPO and/or COG. AVX is a suggested provider of electronic components. www.avxcorp.com

Description	Component Part No.(1, 2)
SY87700L/SY87700V/SY87701L/SY87701V	U1
80Ω	PLLS+, *R5*
1.5µF	PLLS–, *C3*
50Ω	PLLR+, *R6*
1.0µF	PLLR–, *C4*
5kΩ or 4.7kΩ	Pull Up Resistor x 6, *R17 – R22*
330Ω or 220Ω (see schematic)	Output Pull Down Resistor, *R11 – R16*
4.7KΩ	Pull Up Resistor, *R7*
130Ω	Pull Up Resistor, *R9*
12kΩ	Pull Down Resistor, *R8*
12kΩ	*R10*
120Ω	*R23*
0.1µF	AC Coupling Capacitors x 6, *C1, C2, C14 – C19*
Tantalum, 22µF, 16V	Decoupling Capacitor, *C6, C8*
0.1µF	Decoupling Capacitors x 7, *C5, C7, C9 – C13*
Murata BLM21A102F	Ferrite Bead, *FB1*
1N4148	Diode, *D1*
Johnson SMAs, ID#142-0701-201	SMAs x 9
6-pin Dip switch	SW1
	DPDT Slide Switch
	LED

NOTES:

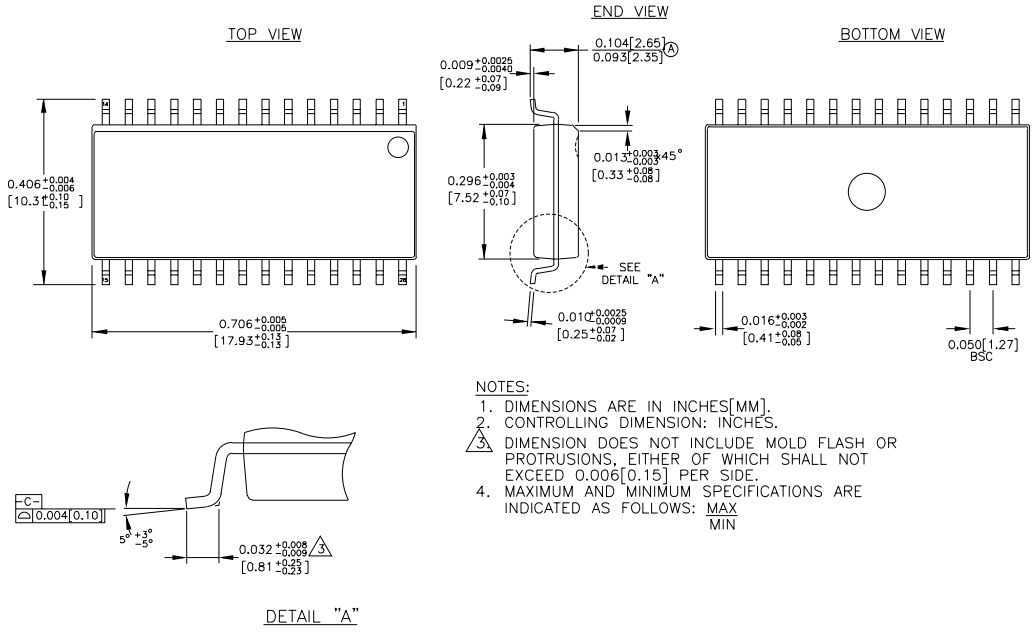
1. For V_{CC} = 3.3V
   R8 = 12kΩ; R = 130Ω
2. For V_{CC} = 5.0V
   R8 = 24kΩ; R9 = 200Ω

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY87701VZC	Z28-1	Commercial
SY87701VHC	H32-1*	Commercial

*Contact factory for availability.

28 LEAD SOIC .300" WIDE (Z28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

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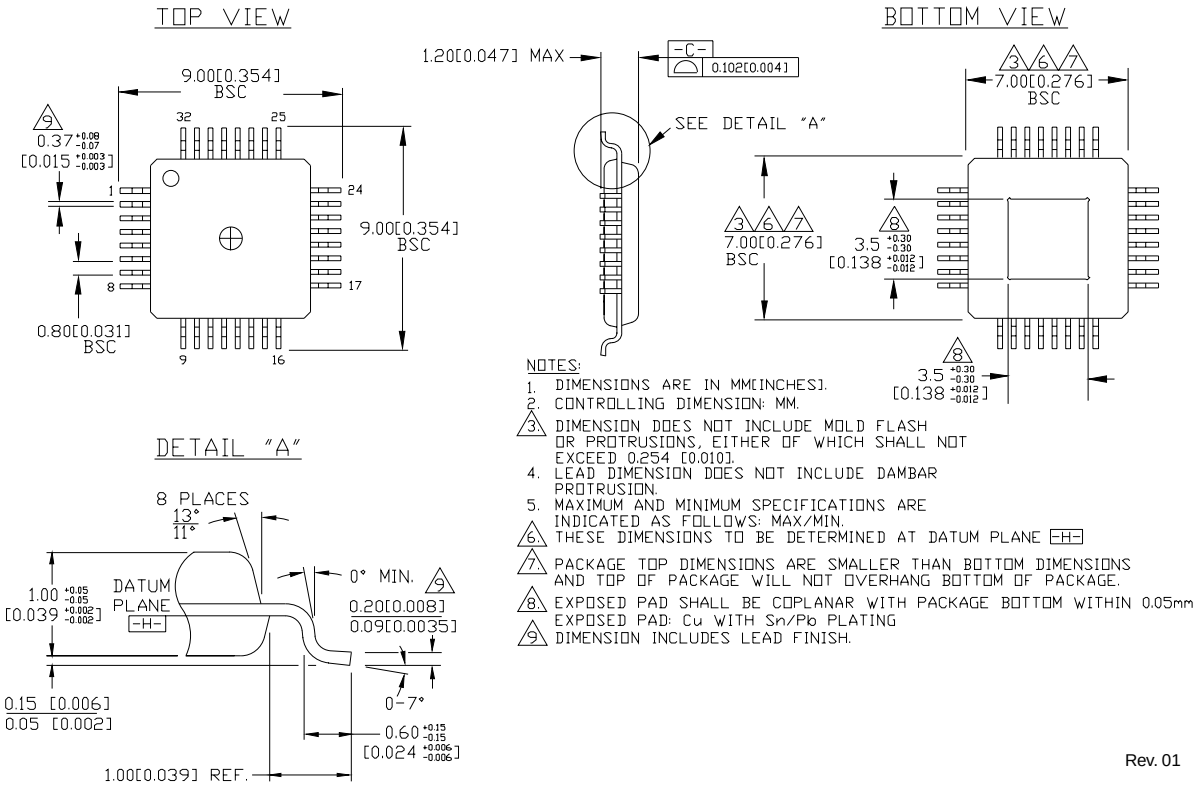
32 LEAD EPAD TQFP (DIE UP) (H32-1)



NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
9. EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINISH.

Rev. 01

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