



REDUCED LATENCY DRAM (RLDRAM)

MT49H8M32 – 1 Meg x 32 x 8 banks
 MT49H16M16 – 2 Meg x 16 x 8 banks

For the latest data sheet, please refer to the Micron
 Web site: www.micron.com/dramds

FEATURES

- 2.5V V_{EXT}, 1.8V V_{DD}, 1.8V V_{DDQ} I/O
- Cyclic bank addressing for maximum data out bandwidth
- Non-multiplexed addresses
- Non-interruptible sequential burst of two (2-bit prefetch) and four (4-bit prefetch) DDR
- Target 600 Mb/s/p data rate
- Programmable Read Latency (RL) of 5-8
- Data valid signal (DVLD) activated as read data is available
- Data Mask signals (DM0/DM1) to mask first and second part of write data burst
- IEEE 1149.1 compliant JTAG boundary scan
- Pseudo-HSTL 1.8V I/O Supply
- Internal Auto Precharge
- Refresh requirements: 32ms at 100°C junction temperature (8K refresh for each bank, 64K refresh command must be issued in total each 32ms)

OPTIONS

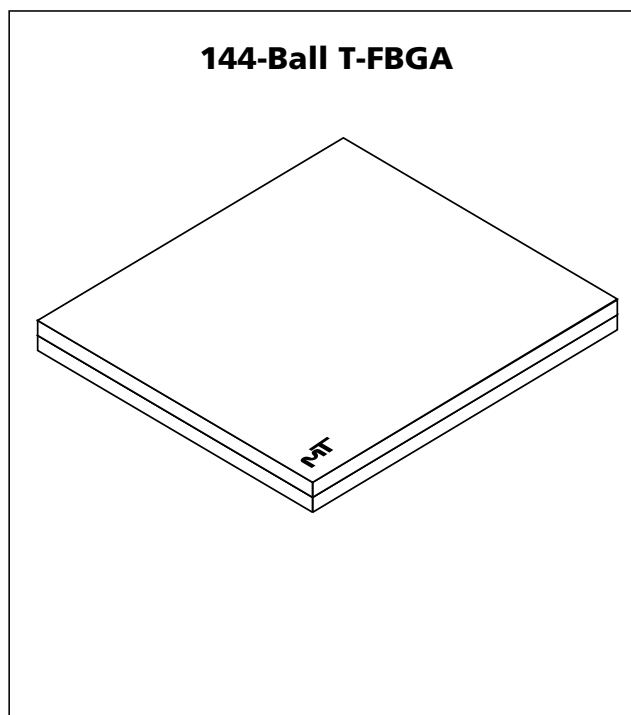
- Clock Cycle Timing

| | |
|-----------------|------|
| 3.3ns (300 MHz) | -3.3 |
| 4ns (250 MHz) | -4 |
| 5ns (200 MHz) | -5 |
- Configuration

| | |
|---------------------------------------|--------------|
| 8 Meg x 32 (1 Meg x 32 x 8 banks) | MT49H8M32FM |
| 16 Meg x 16 (2 Meg x 16 x 8 banks) | MT49H16M16FM |
- Package

| | |
|--------------------------------|----|
| 144-ball, 11mm x 18.5mm T-FBGA | FM |
|--------------------------------|----|

MARKING



row/column address multiplexing and is optimized for fast random access and high-speed bandwidth.

RLDRAM is designed for communication data storages like transmit or receive buffers in telecommunication systems as well as data or instruction cache applications requiring large amounts of memory.

POWER-UP INITIALIZATION

Since the RLDRAM does not have a designated reset function, the following procedure must be executed in order to initialize the internal state machine, regulators, and force the DRAM to be in ready state.

- Apply power, then start clock
- After power on, an initial pause of 200µs is required
- MRS command for 2 clocks and set standard mode register for 1 clock (2 dummies plus 1 valid MRS set)
- 8 refresh cycles (minimum), one on each bank and separated by 2,048 cycles (^tMRS must be satisfied between MRS and first REF command)
- Ready for normal operation (^tRC cycles after the last refresh command)

VALID PART NUMBERS

| PART NUMBER | DESCRIPTION |
|-----------------|-------------|
| MT49H8M32FM-xx | 8 Meg x 32 |
| MT49H16M16FM-xx | 16 Meg x 16 |

GENERAL DESCRIPTION

The Micron[®] 256Mb Reduced Latency DRAM (RLDRAM) contains 8 banks x32Mb of memory accessible with 32-bit or 16-bit I/Os in a double data rate (DDR) format where the data is provided and synchronized with a differential echo clock signal. RLDRAM does not require

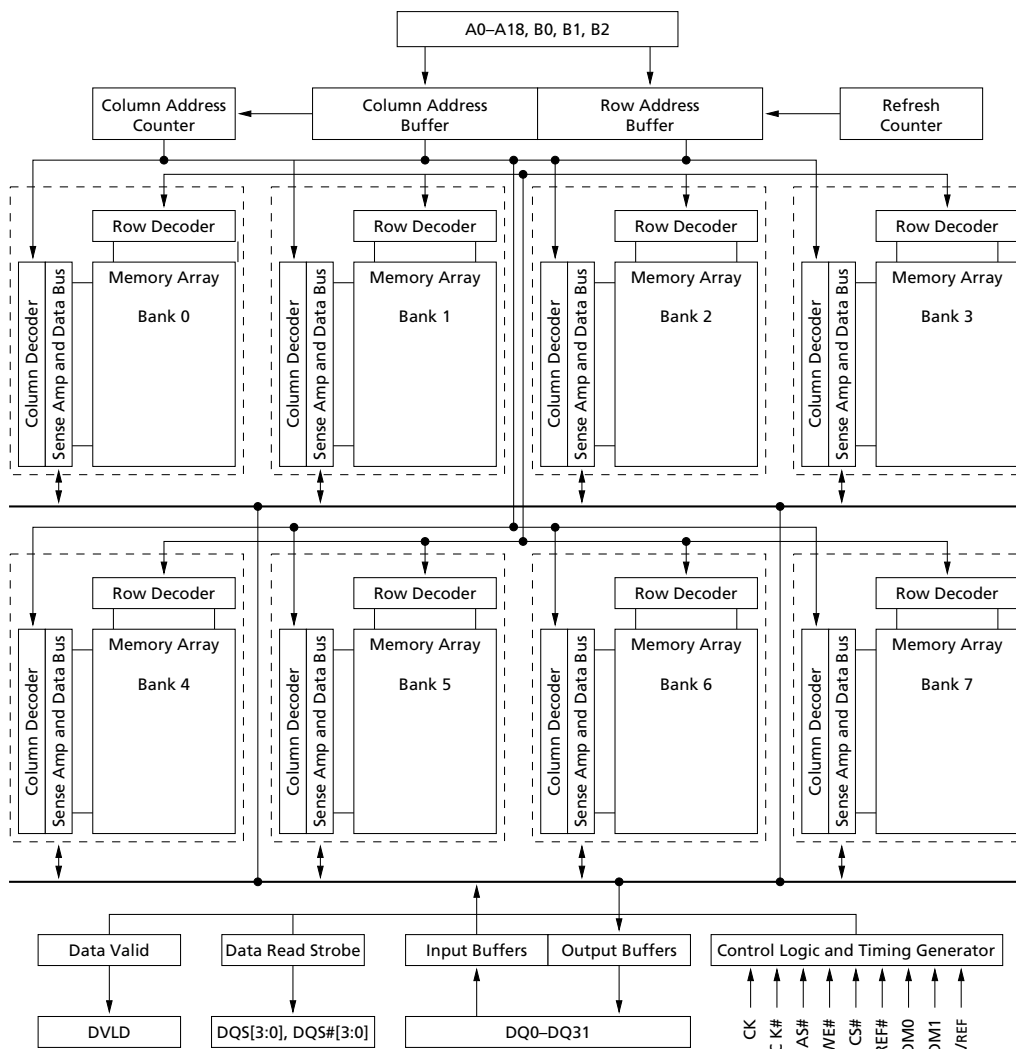


POWER-DOWN

Because the RLDRAM uses multiple power supply voltage, the following sequence is required for power-down.

- Take all input signals to be V_{ss} or High-Z
It is recommended to place Schottky diodes on the board between the 2.5V and 1.8V power supplies.

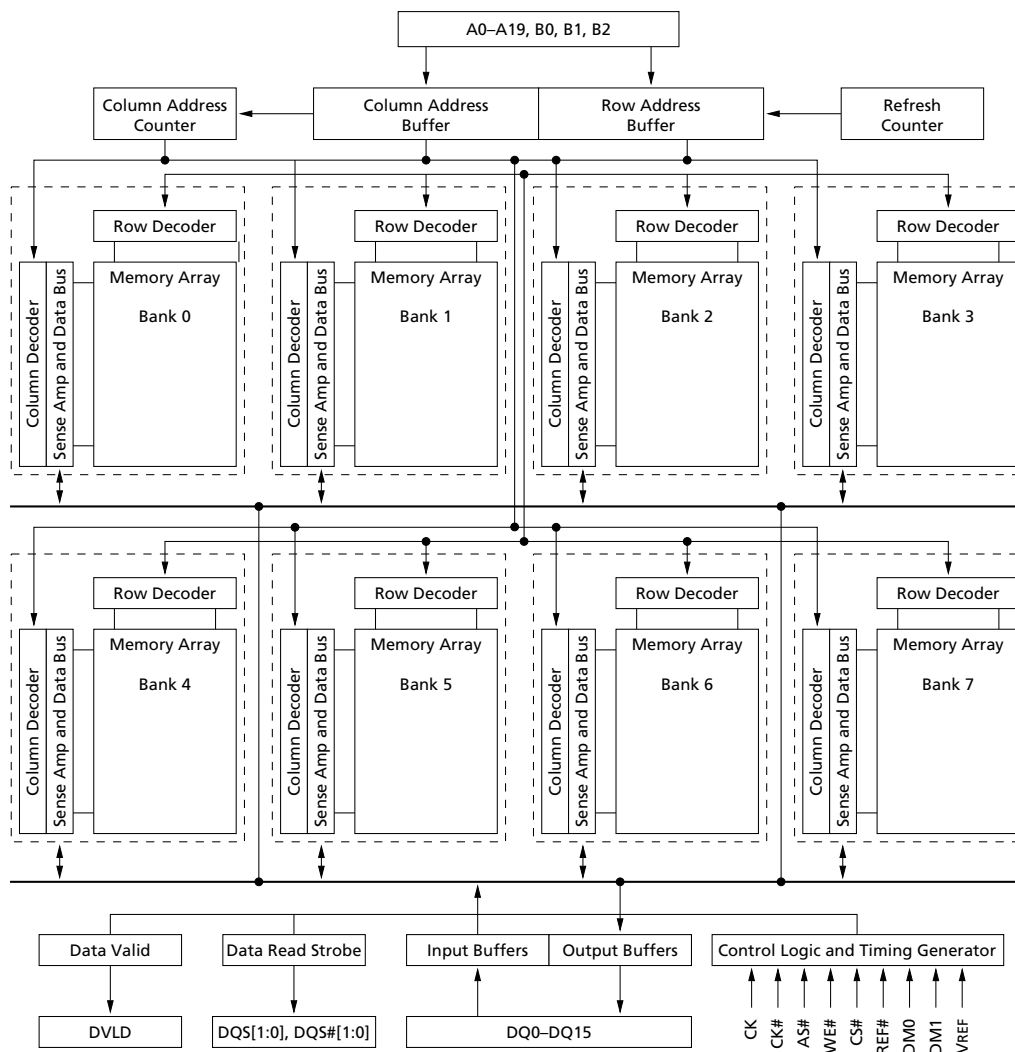
**FUNCTIONAL BLOCK DIAGRAM
8 Meg x 32**



NOTE: 1. When the BL4 setting is used, A18 is a "Don't Care."



FUNCTIONAL BLOCK DIAGRAM
16 Meg x 16



- NOTE:** 1. When the BL4 setting is used, A19 is a "Don't Care."
2. In the 16 Meg x 16 configuration, only DQS[1:0] and DQS#[1:0] are used.



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8 MEG x 32 BALL ASSIGNMENT (Top View)
144-Ball T-FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----------|-----------------|------------------|------------------|------------------|---|---|---|---|------------------|------------------|------|-----------------|
| A | V _{SS} | V _{EXT} | V _{REF} | V _{SS} | | | | | V _{SS} | V _{EXT} | TMS | TCK |
| B | V _{SS} | DQ8 | DQ9 | V _{SSQ} | | | | | V _{SSQ} | DQ1 | DQ0 | V _{SS} |
| C | V _{SS} | DQ10 | DQ11 | V _{DDQ} | | | | | V _{DDQ} | DQ3 | DQ2 | V _{SS} |
| D | V _{SS} | DQS1 | DQS1# | V _{SSQ} | | | | | V _{SSQ} | DQS0# | DQS0 | V _{SS} |
| E | V _{SS} | DQ12 | DQ13 | V _{DDQ} | | | | | V _{DDQ} | DQ5 | DQ4 | V _{SS} |
| F | DM0 | DQ14 | DQ15 | V _{SSQ} | | | | | V _{SSQ} | DQ7 | DQ6 | DVLD |
| G | A5 | A6 | A7 | V _{DD} | | | | | V _{DD} | A2 | A1 | A0 |
| H | A8 | A9 | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A4 | A3 |
| J | AS# | B2 | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B0 | CK |
| K | WE# | REF# | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B1 | CK# |
| L | A18 | CS# | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A14 | A13 |
| M | A15 | A16 | A17 | V _{DD} | | | | | V _{DD} | A12 | A11 | A10 |
| N | DM1 | DQ22 | DQ23 | V _{SSQ} | | | | | V _{SSQ} | DQ31 | DQ30 | NC |
| P | V _{SS} | DQ20 | DQ21 | V _{DDQ} | | | | | V _{DDQ} | DQ29 | DQ28 | V _{SS} |
| R | V _{SS} | DQS2 | DQS2# | V _{SSQ} | | | | | V _{SSQ} | DQS3# | DQS3 | V _{SS} |
| T | V _{SS} | DQ18 | DQ19 | V _{DDQ} | | | | | V _{DDQ} | DQ27 | DQ26 | V _{SS} |
| U | V _{SS} | DQ16 | DQ17 | V _{SSQ} | | | | | V _{SSQ} | DQ25 | DQ24 | V _{SS} |
| V | V _{SS} | V _{EXT} | V _{REF} | V _{SS} | | | | | V _{SS} | V _{EXT} | TDO | TDI |

16 MEG x 16 BALL ASSIGNMENT (Top View)
144-Ball T-FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----------|-----------------|------------------|------------------|------------------|---|---|---|---|------------------|------------------|------|-----------------|
| A | V _{SS} | V _{EXT} | V _{REF} | V _{SS} | | | | | V _{SS} | V _{EXT} | TMS | TCK |
| B | V _{SS} | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQ1 | DQ0 | V _{SS} |
| C | V _{SS} | NC | NC | V _{DDQ} | | | | | V _{DDQ} | DQ3 | DQ2 | V _{SS} |
| D | V _{SS} | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQS0# | DQS0 | V _{SS} |
| E | V _{SS} | NC | NC | V _{DDQ} | | | | | V _{DDQ} | DQ5 | DQ4 | V _{SS} |
| F | DM0 | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQ7 | DQ6 | DVLD |
| G | A5 | A6 | A7 | V _{DD} | | | | | V _{DD} | A2 | A1 | A0 |
| H | A8 | A9 | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A4 | A3 |
| J | AS# | B2 | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B0 | CK |
| K | WE# | REF# | V _{DD} | V _{DD} | | | | | V _{DD} | V _{DD} | B1 | CK# |
| L | A19 | CS# | V _{SS} | V _{SS} | | | | | V _{SS} | V _{SS} | A14 | A13 |
| M | A15 | A16 | A17 | V _{DD} | | | | | V _{DD} | A12 | A11 | A10 |
| N | DM1 | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQ15 | DQ14 | A18 |
| P | V _{SS} | NC | NC | V _{DDQ} | | | | | V _{DDQ} | DQ13 | DQ12 | V _{SS} |
| R | V _{SS} | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQS1# | DQS1 | V _{SS} |
| T | V _{SS} | NC | NC | V _{DDQ} | | | | | V _{DDQ} | DQ11 | DQ10 | V _{SS} |
| U | V _{SS} | NC | NC | V _{SSQ} | | | | | V _{SSQ} | DQ9 | DQ8 | V _{SS} |
| V | V _{SS} | V _{EXT} | V _{REF} | V _{SS} | | | | | V _{SS} | V _{EXT} | TDO | TDI |


BALL DESCRIPTIONS

| T-FBGA (x32) | T-FBGA (x16) | SYMBOL | TYPE | DESCRIPTION |
|---|---|--|------------------|--|
| 12J, 12K | 12J, 12K | CK, CK# | Input | Differential input clock pair |
| 2L | 2L | CS# | Input | Chip select |
| 1J | 1J | AS# | Input | Address strobe |
| 1K | 1K | WE# | Input | Write enable |
| 2K | 2K | REF# | Input | Auto refresh |
| 11J, 11K, 2J | 11J, 11K, 2J | B[0:2] | Input | Bank select |
| 12G, 11G, 10G, 12H, 11H, 1G, 2G, 3G, 1H, 2H, 12M, 11M, 10M, 12L, 11L, 1M, 2M, 3M, 1L | 12G, 11G, 10G, 12H, 11H, 1G, 2G, 3G, 1H, 2H, 12M, 11M, 10M, 12L, 11L, 1M, 2M, 3M, 12N, 1L | A[0:18] A[0:19] | Input | Address input |
| 1F, 1N | 1F, 1N | DM0, DM1 | Input | Data Mask |
| 11A 12V | 11A 12V | TMS TDI | Input | IEEE 1149.1 Test Inputs: JEDEC-standard 1.8V I/O levels. These pins may be left Not Connected if the JTAG function is not used in the circuit. |
| 12A | 12A | TCK | Input | IEEE 1149.1 Clock Input: JEDEC-standard 1.8V I/O levels. This pin must be tied to V _{ss} if the JTAG function is not used in the circuit. |
| 3A, 3V | 3A, 3V | V _{REF} | Input | Input Reference Voltage: Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers. |
| 11B, 10B, 11C, 10C, 11E, 10E, 11F, 10F, 2B, 3B, 2C, 3C, 2E, 3E, 2F, 3F, 2U, 3U, 2T, 3T, 2P, 3P, 2N, 3N, 11U, 10U, 11T, 10T, 11P, 10P, 11N, 10N | 11B, 10B, 11C, 10C, 11E, 10E, 11F, 10F, 11U, 10U, 11T, 10T, 11P, 10P, 11N, 10N | DQ0–DQ31 | Input/ Output | Synchronous Data I/Os: Input data must meet setup and hold times around the rising edges of CK and CK#. Output data is synchronized to DQS and DQS#. |
| 11D, 2D, 2R, 11R, 10D, 3D, 3R, 10R | 11D, 11R, 10D, 10R | DQS0–3 (x32) DQS#0–3 (x32) DQS0–1 (x16) DQS#0–1 (x16) | Output | Differential data read strobe |
| 12F | 12F | DVLD | Output | Data Valid |
| 11V | 11V | TDO | Output | IEEE 1149.1 Test Output: JEDEC-standard 1.8V I/O level. |
| 2A, 2V, 10A, 10V | 2A, 2V, 10A, 10V | V _{EXT} | Supply | Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range. |
| 3J, 3K, 4G, 4J, 4K, 4M, 9G, 9J, 9K, 9M, 10J, 10K | 3J, 3K, 4G, 4J, 4K, 4M, 9G, 9J, 9K, 9M, 10J, 10K | V _{DD} | Supply | Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range. |

(continued on next page)


BALL DESCRIPTIONS (continued)

| T-FBGA (x32) | T-FBGA (x16) | SYMBOL | TYPE | DESCRIPTION |
|---|---|------------------|--------|--|
| 4C, 4E, 4P, 4T, 9C, 9E, 9P, 9T | 4C, 4E, 4P, 4T, 9C, 9E, 9P, 9T | V _{DDQ} | Supply | Power Supply: Isolated Output Buffer Supply. Nominally 1.8V. See DC Electrical Characteristics and Operating Conditions for range. |
| 1A–E, 1P–V, 3H, 3L, 4A, 4H, 4L, 4V, 9A, 9H, 9L, 9V, 10H, 10L, 12B–E, 12P–U | 1A–E, 1P–V, 3H, 3L, 4A, 4H, 4L, 4V, 9A, 9H, 9L, 9V, 10H, 10L, 12B–E, 12P–U | V _{SS} | Supply | Power Supply: GND. |
| 4B, 4D, 4F, 4N, 4R, 4U, 9B, 9D, 9F, 9N, 9R, 9U | 4B, 4D, 4F, 4N, 4R, 4U, 9B, 9D, 9F, 9N, 9R, 9U | V _{SSQ} | Supply | Power Supply: Isolated Output Buffer Supply. GND. |
| 12N | 2B–2F, 2N–2U, 3B–3F, 3N–3U | NC | – | No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. |


TRUTH TABLE¹

| OPERATION | CS# | AS# | WE# | REF# | A[19:0] ² | B[2:0] | DM[1:0] |
|-------------------------------------|-----|-----|-----|------|----------------------|--------|---------|
| READ Cycle | L | L | H | H | VALID | VALID | X |
| WRITE Cycle | L | L | L | H | VALID | VALID | VALID |
| NOP: No operation | L | H | H | H | X | X | X |
| Deselect | H | X | X | X | X | X | X |
| Auto Refresh | L | H | H | L | X | VALID | X |
| MRS: Mode Register Set ³ | L | L | L | L | VALID | X | X |

- NOTE:**
- X = "Don't Care."
H = logic HIGH.
L = logic LOW.
 - In the x32 configuration A19 is not used.
 - Only A17–A0 are used for the Mode Register Set Command.



PROGRAMMING DESCRIPTION

The following table shows, for three operating frequencies, the different RLD RAM configurations that can be programmed into the Mode Register. The Read Latency (RL) values and the Write Latencies (WL) used by the

RLDRAM for the two Burst Lengths (BL) are also indicated. Finally, the minimum allowed ^tRC in clock cycles and in ns are shown as well. The shaded areas correspond to configurations that are not allowed.

RLDRAM Programming Table

| | | FREQUENCY | | | | | |
|-----------------------|------|----------------|------|------|------|------|------|
| | | -3.3 (300 MHz) | | | | | |
| | Unit | 1 | 2 | 3 | 4 | 5 | 6 |
| Config. Nb. | | 1 | 2 | 3 | 4 | 5 | 6 |
| RL | TCK | 5 | 5 | 5 | 6 | 7 | 8 |
| WL (BL2) | TCK | 2 | 2 | 2 | 3 | 4 | 5 |
| WL (BL4) | TCK | 1 | 1 | 1 | 2 | 3 | 4 |
| ^t RC (MIN) | TCK | 5 | 6 | 7 | 8 | 9 | 10 |
| ^t RC (MIN) | ns | 16.7 | 20.0 | 23.3 | 26.7 | 30.0 | 33.3 |
| | | -4 (250 MHz) | | | | | |
| | Unit | 1 | 2 | 3 | 4 | 5 | 6 |
| Config. Nb. | | 1 | 2 | 3 | 4 | 5 | 6 |
| RL | TCK | 5 | 5 | 5 | 6 | 7 | 8 |
| WL (BL2) | TCK | 2 | 2 | 2 | 3 | 4 | 5 |
| WL (BL4) | TCK | 1 | 1 | 1 | 2 | 3 | 4 |
| ^t RC (MIN) | TCK | 5 | 6 | 7 | 8 | 9 | 10 |
| ^t RC (MIN) | ns | 20 | 24 | 28 | 32 | 36 | 40 |
| | | -5 (200 MHz) | | | | | |
| | Unit | 1 | 2 | 3 | 4 | 5 | 6 |
| Config. Nb. | | 1 | 2 | 3 | 4 | 5 | 6 |
| RL | TCK | 5 | 5 | 5 | 6 | 7 | 8 |
| WL (BL2) | TCK | 2 | 2 | 2 | 3 | 4 | 5 |
| WL (BL4) | TCK | 1 | 1 | 1 | 2 | 3 | 4 |
| ^t RC (MIN) | TCK | 5 | 6 | 7 | 8 | 9 | 10 |
| ^t RC (MIN) | ns | 25 | 30 | 35 | 40 | 45 | 50 |

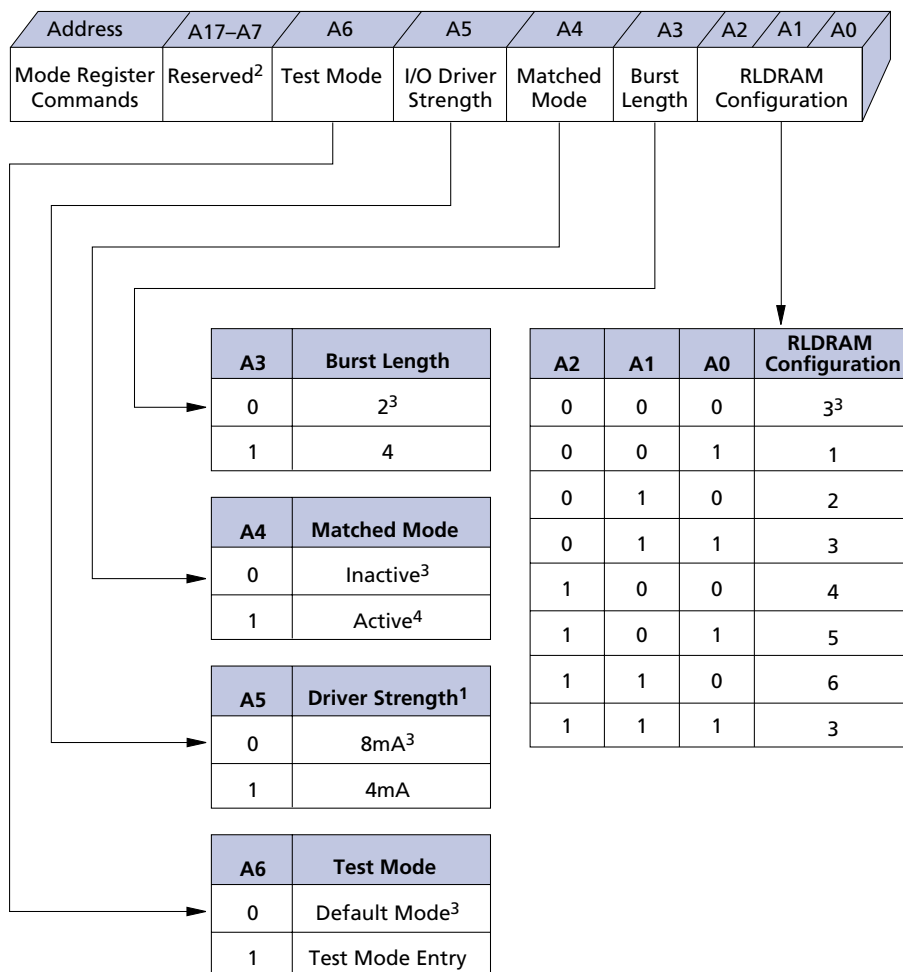
- NOTE:**
1. The speed sort -3.3 provides part functional up to 300 MHz in the configurations 4, 5, and 6 only.
The functionality of the configurations 1, 2, and 3 is not guaranteed for speed sort -3.3.
 2. The speed sort -4 provides part functional up to 250 MHz in the configurations 3, 4, 5, and 6 only.
The functionality of the configurations 1 and 2 is not guaranteed for speed sort -4.
 3. The speed sort -5 provides part functional up to 200 MHz in all configurations.



MODE REGISTER DESCRIPTION

The address signals A[17:0] are used to set the mode register.

Mode Register Command Table



- NOTE:**
1. HSTL-compliant current specification
 2. Bits A17-A6 MUST be set LOW (Logic 0)
 3. Default configuration
 4. When Matched Mode is asserted, the automatic I/O impedance calibration is activated
 5. Test Mode entry for vendor test mode only
 6. The Mode Register Set default configuration corresponds to all address bits equal to zero



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The RLDRAM incorporates a serial boundary scan Test Access Port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the RLDRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 1.8V I/O logic levels.

The RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

It is possible to operate the RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

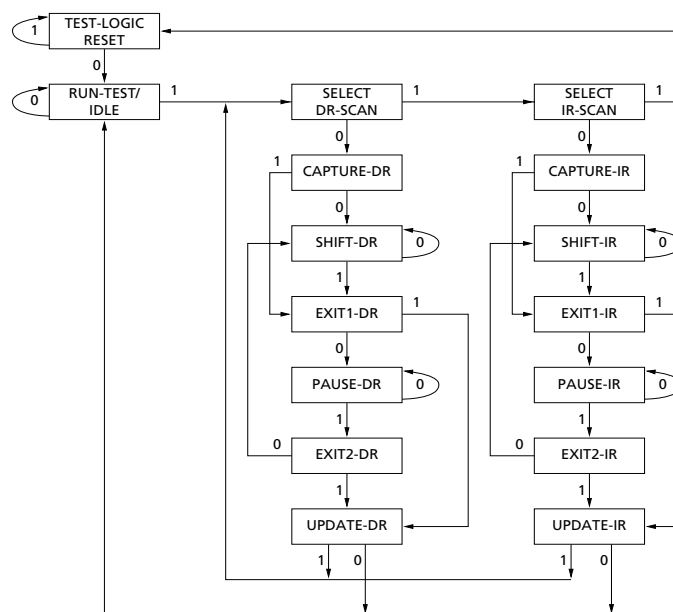
TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 1. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 2.)

Figure 1
TAP Controller State Diagram



NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.



TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 1.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 2.)

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the RLD RAM and may be performed while the RLD RAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the RLD RAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 2. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the RLD RAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

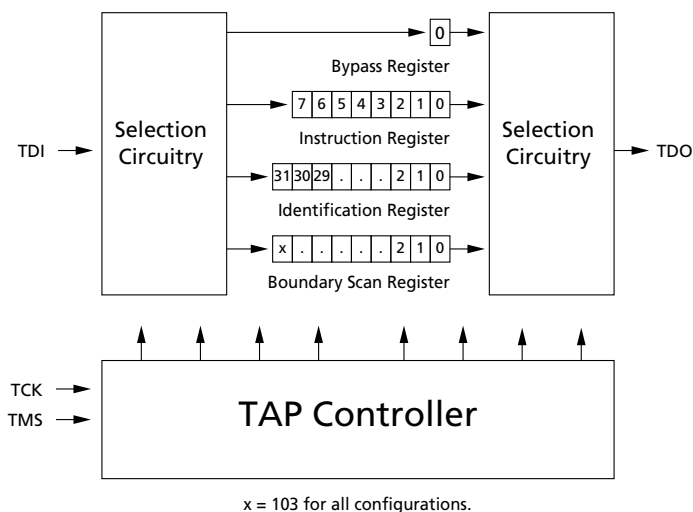
BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the RLD RAM. Several no connect (NC) pins are also included in the scan register to reserve pins. The RLD RAM has a 104-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the RLD RAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

**Figure 2
TAP Controller Block Diagram**





IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the RLDRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table (see page 16). Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this RLDRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the RLDRAM and cannot preload the I/O buffers. The RLDRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the RLDRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the RLDRAM outputs in a High-Z state, CQ, CQ#.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction regis-

ter upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bi-directional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the RLDRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (meta-stable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}). The RLDRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

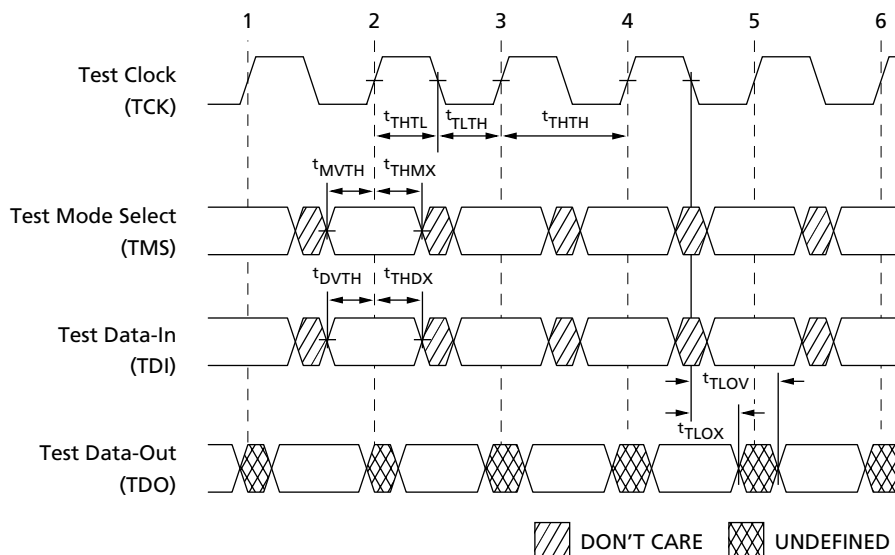
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.



TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (+20°C ≤ T_j ≤ +100°C, +1.7V ≤ V_{DD} ≤ +1.9V)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|-------------------------|-------------------|-----|-----|-------|
| Clock | | | | |
| Clock cycle time | t ^{THTH} | 20 | | ns |
| Clock frequency | f ^{TF} | | 50 | MHz |
| Clock HIGH time | t ^{THTL} | 10 | | ns |
| Clock LOW time | t ^{TLTH} | 10 | | ns |
| Output Times | | | | |
| TCK LOW to TDO unknown | t ^{TLOX} | 0 | 10 | ns |
| TCK LOW to TDO valid | t ^{TLOV} | | 10 | ns |
| TDI valid to TCK HIGH | t ^{DVTH} | 5 | | ns |
| TCK HIGH to TDI invalid | t ^{THDX} | 5 | | ns |
| Setup Times | | | | |
| TMS setup | t ^{MVTH} | 5 | | ns |
| Capture setup | t ^{CS} | 5 | | ns |
| Hold Times | | | | |
| TMS hold | t ^{THMX} | 5 | | ns |
| Capture hold | t ^{CH} | 5 | | ns |

NOTE: 1. t^{CS} and t^{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 4.



TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ 110°C, +2.4V ≤ V_{DD} ≤ +2.6V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|--|------------------|-------------------------|-------------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | V _{REF} + 0.15 | V _{DD} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | V _{IL} | V _{SSQ} - 0.3 | V _{REF} - 0.15 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | I _{LI} | -5.0 | 5.0 | μA | |
| Output Leakage Current | Output(s) disabled, 0V ≤ V _{IN} ≤ V _{DDQ} | I _{LO} | -5.0 | 5.0 | μA | |
| Output Low Voltage | I _{OLC} = 100μA | V _{OL1} | | V _{REF} - TBD | V | 1 |
| Output Low Voltage | I _{OLT} = 2mA | V _{OL2} | | V _{REF} - TBD | V | 1 |
| Output High Voltage | I _{OHC} = 100μA | V _{OH1} | V _{REF} + TBD | | V | 1 |
| Output High Voltage | I _{OHT} = 2mA | V _{OH2} | V _{REF} + TBD | | V | 1 |

- NOTE:**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH(AC)} ≤ V_{DD} + 1.5V for t ≤ 'KHKH/2
 Undershoot: V_{IL(AC)} ≥ -0.5V for t ≤ 'KHKH/2
 Power-up: V_{IH} ≤ +1.9 and V_{DD} ≤ 1.7V and V_{DDQ} ≤ 1.4V for t ≤ 200ms
 During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals (such as LD#, R/W#, etc.) may not have pulse widths less than 'KHKL (MIN) or operate at frequencies exceeding 'KF (MAX).



IDENTIFICATION REGISTER DEFINITIONS

| INSTRUCTION FIELD | ALL DEVICES | DESCRIPTION |
|---------------------------------------|------------------|--|
| REVISION NUMBER (31:28) | 00ab | ab = 10 for x32, 01 for x16. |
| DEVICE ID (27:12) | 0000000010100111 | This represents the part number |
| MICRON JEDEC ID CODE (11:1) | 00000101100 | Allows unique identification of RLDRAM vendor. |
| ID Register Presence Indicator (0) | 1 | Indicates the presence of an ID register. |

SCAN REGISTER SIZES

| REGISTER NAME | BIT SIZE |
|---------------|----------|
| Instruction | 8 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 104 |

INSTRUCTION CODES

| INSTRUCTION | CODE | DESCRIPTION |
|----------------|-----------|---|
| EXTEST | 0000 0000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction is not 1149.1-compliant. This operation does not affect RLDRAM operations. |
| IDCODE | 0010 0001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLDRAM operations. |
| SAMPLE/PRELOAD | 0000 0101 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant. |
| BYPASS | 1111 1111 | Places the bypass register between TDI and TDO. This operation does not affect RLDRAM operations. |



Boundary Scan (Exit) Order

| BIT# | FBGA BALL |
|------|-----------|
| 1 | J1 |
| 2 | J2 |
| 3 | H2 |
| 4 | H1 |
| 5 | G1 |
| 6 | G3 |
| 7 | G2 |
| 8 | F1 |
| 9 | F3 |
| 10 | F3 |
| 11 | F2 |
| 12 | F2 |
| 13 | E3 |
| 14 | E3 |
| 15 | E2 |
| 16 | E2 |
| 17 | D2 |
| 18 | D3 |
| 19 | C2 |
| 20 | C2 |
| 21 | C3 |
| 22 | C3 |
| 23 | B2 |
| 24 | B2 |
| 25 | B3 |
| 26 | B3 |
| 27 | B10 |
| 28 | B10 |
| 29 | B11 |
| 30 | B11 |
| 31 | C10 |
| 32 | C10 |
| 33 | C11 |
| 34 | C11 |
| 35 | D10 |

| BIT# | FBGA BALL |
|------|-----------|
| 36 | D11 |
| 37 | E11 |
| 38 | E11 |
| 39 | E10 |
| 40 | E10 |
| 41 | F11 |
| 42 | F11 |
| 43 | F10 |
| 44 | F10 |
| 45 | F12 |
| 46 | G11 |
| 47 | G10 |
| 48 | G12 |
| 49 | H12 |
| 50 | H11 |
| 51 | J11 |
| 52 | J12 |
| 53 | K12 |
| 54 | K11 |
| 55 | L11 |
| 56 | L12 |
| 57 | M12 |
| 58 | M10 |
| 59 | M11 |
| 60 | M12 |
| 61 | N10 |
| 62 | N10 |
| 63 | N11 |
| 64 | N11 |
| 65 | P10 |
| 66 | P10 |
| 67 | P11 |
| 68 | P11 |
| 69 | R11 |
| 70 | R10 |

| BIT# | FBGA BALL |
|------|-----------|
| 71 | T11 |
| 72 | T11 |
| 73 | T10 |
| 74 | T10 |
| 75 | U11 |
| 76 | U11 |
| 77 | U10 |
| 78 | U10 |
| 79 | U3 |
| 80 | U3 |
| 81 | U2 |
| 82 | U2 |
| 83 | T3 |
| 84 | T3 |
| 85 | T2 |
| 86 | T2 |
| 87 | R3 |
| 88 | R2 |
| 89 | P2 |
| 90 | P2 |
| 91 | P3 |
| 92 | P3 |
| 93 | N2 |
| 94 | N2 |
| 95 | N3 |
| 96 | N3 |
| 97 | N1 |
| 98 | M2 |
| 99 | M3 |
| 100 | M1 |
| 101 | L1 |
| 102 | L2 |
| 103 | K2 |
| 104 | K1 |

NOTE: 1. Any unused pins that are in the order will read as a logic "0."



ABSOLUTE MAXIMUM RATINGS*

| | |
|---|------------------------------------|
| Storage Temperature | -55°C to +150°C |
| I/O Voltage | -0.3V to + V _{DDQ} + 0.3V |
| Voltage on V _{EXT} Supply Relative to V _{SS} ... | -0.3V to +2.8V |
| Voltage on V _{DD} Supply Relative to V _{SS} | -0.3V to +2.1V |
| Voltage on V _{DDQ} Supply Relative to V _{SS} .. | -0.3V to +2.1V |
| Junction Temperature** | 100°C |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

RECOMMENDED DC OPERATION RANGES

All values are recommended operating conditions unless otherwise noted. External on board (PCB) capacitance values are required as follows:

- V_{DDQ} :2 x 0.1µF/device
- V_{DD} :2 x 0.1µF/device
- V_{REF} :0.1µF/device
- V_{EXT} :0.1µF/device

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +1.75V ≤ V_{DD} ≤ +1.85V unless otherwise noted)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|------------------|----------------------------|----------------------------|-------|---------|
| Supply Voltage | V _{EXT} | 2.38 | 2.63 | V | 1 |
| Supply Voltage | V _{DD} | 1.75 | 1.85 | V | 1, |
| Isolated Output Buffer Supply | V _{DDQ} | 1.7 | 1.9 | V | 1, 4 |
| Reference Voltage | V _{REF} | 0.95 x V _{DDQ} /2 | 1.05 x V _{DDQ} /2 | V | 1, 2, 3 |

- NOTE:**
1. All voltages referenced to V_{SS} (GND).
 2. Typically the value of V_{REF} is expect to be 0.5x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
 3. Peak to peak AC noise on V_{REF} must not exceed 2% V_{REF(DC)}.
 4. During normal operation, V_{DDQ} must not exceed V_{DD}.



DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +1.75V ≤ V_{DD} ≤ +1.85V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYM | MIN | MAX | UNITS | NOTES |
|------------------------------|---|------------------|-------------------------|-------------------------|-------|---------|
| Input High (Logic 1) Voltage | Matched Impedance Mode | V _{IH} | V _{REF} + 0.15 | V _{DDQ} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | Matched Impedance Mode | V _{IL} | V _{SSQ} - 0.3 | V _{REF} - 0.15 | V | 1, 2 |
| Output High Voltage | Matched Impedance Mode | V _{OH} | V _{DDQ} | | V | 1, 3, 4 |
| Output Low Voltage | Matched Impedance Mode | V _{OL} | | 0 | V | 1, 3, 4 |
| Input High (Logic 1) Voltage | HSTL Strong | V _{IH} | V _{REF} + 0.1 | V _{DDQ} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | HSTL Strong | V _{IL} | V _{SSQ} - 0.3 | V _{REF} - 0.1 | V | 1, 2 |
| Output High Voltage | HSTL Strong | V _{OH} | V _{DDQ} - 0.4 | | V | 1, 3, 4 |
| Output Low Voltage | HSTL Strong | V _{OL} | | 0.4 | V | 1, 3, 4 |
| Input High (Logic 1) Voltage | HSTL Weak | V _{IH} | | | V | 1, 2 |
| Input Low (Logic 0) Voltage | HSTL Weak | V _{IL} | | | V | 1, 2 |
| Output High Voltage | HSTL Weak | V _{OH} | | | V | 1, 3, 4 |
| Output Low Voltage | HSTL Weak | V _{OL} | | | V | 1, 3, 4 |
| Clock Input Leakage Current | | I _{LC} | -5 | 5 | μA | |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DDQ} | I _{LI} | -5 | 5 | μA | |
| Output Leakage Current | | I _{LO} | -5 | 5 | μA | |
| Reference Voltage Current | | I _{REF} | -5 | 5 | μA | |

- NOTE:**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7V for t ≤ t^{KHKH}/2
 Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ t^{KHKH}/2
 Power-up: V_{IH} ≤ V_{DDQ} + 0.3V and V_{DD} ≤ 1.7V and V_{DDQ} ≤ 1.4V for t ≤ 200ms
 During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than t^{KHKL} (MIN) or operate at cycle rates less than t^{KHKH} (MIN).
 - AC load current is higher than the shown DC values. AC I/O curves are available upon request.
 - HSTL outputs meet JEDEC HSTL Class I and Class II standards.


I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (+20°C ≤ T_J ≤ +110°C; V_{DD} = MAX unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | TYPICAL | | | UNITS | NOTES |
|--------------------------|---|---------------------------------------|---------|-----|-----|-------|-------|
| | | | -3.3 | -4 | -5 | | |
| Operating Supply Current | BL = 2, t ^{CK} = MIN, t ^{RC} = MIN, 1 bank active, Address change up to 8 times during minimum t ^{RC} | I _{DD1} (V _{DD}) | 248 | 208 | 168 | mA | 1 |
| | | I _{DD1} (V _{EXT}) | 17 | 16 | 15 | mA | 1 |
| Operating Supply Current | BL = 4, t ^{CK} = MIN, t ^{RC} = MIN, 4 banks interleave, Address change up to 8 times during minimum t ^{RC} Continuous data | I _{DD4R} (V _{DD}) | 403 | 337 | 271 | mA | 1 |
| | | I _{DD4R} (V _{EXT}) | 27 | 25 | 22 | mA | 1 |
| Operating Supply Current | BL = 2, t ^{CK} = MIN, t ^{RC} = MIN, 8 banks interleave, Address change up to 8 times during minimum t ^{RC} Continuous data | I _{DD8} (V _{DD}) | 610 | 509 | 409 | mA | 1 |
| | | I _{DD8} (V _{EXT}) | 41 | 36 | 32 | mA | 1 |
| Standby Current | t ^{CK} = MIN, CS# = 1 all banks idle, Command toggling | I _{DDs} (V _{DD}) | TBD | TBD | TBD | mA | |
| | | I _{DDs} (V _{EXT}) | TBD | TBD | TBD | mA | |

NOTE: 1. Values determined with outputs in high impedance state.



CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|-----------------------------------|---|-----------------|-----|-----|-------|
| Address/Control Input Capacitance | $T_A = 25^\circ\text{C}; f = 1 \text{ MHz}$ | C _i | 2 | 4 | pF |
| Input/Output Capacitance (DQ) | | C _o | 2 | 4 | pF |
| Clock Capacitance | | C _{CK} | 2 | 4 | pF |

AC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

($+20^\circ\text{C} \leq T_J \leq +110^\circ\text{C}$; $+1.75\text{V} \leq V_{DD} \leq +1.85\text{V}$ unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|-------------------------------|------------------------|-----------------|-------------------------|-------------------------|-------|
| Input High (Logic 1) Voltage | Matched Impedance Mode | V _{IH} | V _{REF} + 0.3 | V _{DDQ} + 0.3 | V |
| Input Low (Logic 0) Voltage | Matched Impedance Mode | V _{IL} | V _{SSQ} - 0.3 | V _{REF} - 0.3 | V |
| CK Differential Input Voltage | Matched Impedance Mode | V _{ID} | 0.6 | V _{DDQ} + 0.6 | V |
| CK Input Crossing Point | Matched Impedance Mode | V _{IX} | V _{REF} - 0.15 | V _{REF} + 0.15 | V |
| Input High (Logic 1) Voltage | HSTL Strong | V _{IH} | V _{REF} + 0.2 | V _{DDQ} + 0.3 | V |
| Input Low (Logic 0) Voltage | HSTL Strong | V _{IL} | V _{SSQ} - 0.3 | V _{REF} - 0.2 | V |
| CK Differential Input Voltage | HSTL Strong | V _{ID} | 0.6 | V _{DDQ} + 0.6 | V |
| CK Input Crossing Point | HSTL Strong | V _{IX} | V _{REF} - 0.15 | V _{REF} + 0.15 | V |
| Input High (Logic 1) Voltage | HSTL Weak | V _{IH} | | | V |
| Input Low (Logic 0) Voltage | HSTL Weak | V _{IL} | | | V |
| CK Differential Input Voltage | HSTL Weak | V _{ID} | | | V |
| CK Input Crossing Point | HSTL Weak | V _{IX} | | | V |



AC ELECTRICAL CHARACTERISTICS

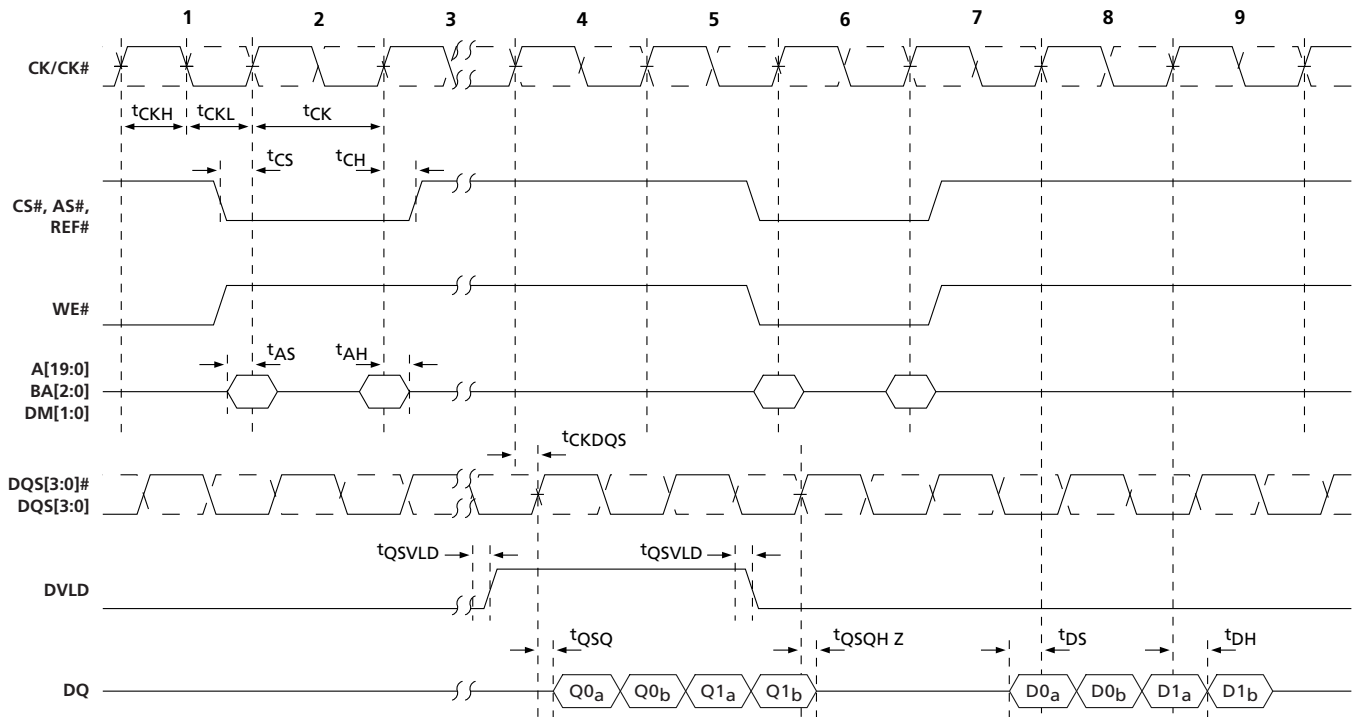
(Notes 4, 5) (+20°C ≤ T_j ≤ +110°C; +1.75V ≤ V_{DD} ≤ +1.85V)

| DESCRIPTION | SYMBOL | -3.3 | | -4 | | -5 | | UNITS | NOTES |
|----------------------|----------------------------------|------|------|------|------|------|------|-----------------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Clock | | | | | | | | | |
| Clock cycle time | t _{CK} | 3.3 | | 4.0 | | 5.0 | | ns | |
| Clock HIGH time | t _{CKH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | |
| Clock LOW time | t _{CKL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | |
| Clock to DQS,DQS# | t _{CKDQS} | 2.3 | 3.7 | 2.3 | 3.7 | 2.3 | 3.7 | ns | 1 |
| DQS,DQS# HIGH time | t _{DQSH} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |
| DQS,DQS# LOW time | t _{DQSL} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |
| Output Times | | | | | | | | | |
| DQS to output valid | t _{QSQ} | -0.3 | 0.3 | -0.3 | 0.3 | -0.3 | 0.3 | ns | 2 |
| DQS to output High-Z | t _{QSQHZ} | 0.4 | | 0.4 | | 0.4 | | ns | |
| DQS# to DVLD | t _{QSVLD} | -0.4 | 0.4 | -0.4 | 0.4 | -0.4 | 0.4 | ns | 3 |
| MRS to any command | t _{MRSC} | 4 | | 4 | | 4 | | t _{CK} | 4 |
| Setup Times | | | | | | | | | |
| Address/Command | t _{AS} /t _{CS} | 1.0 | | 1.0 | | 1.0 | | ns | |
| Data-in | t _{DS} | 0.5 | | 0.5 | | 0.5 | | ns | |
| Hold Times | | | | | | | | | |
| Address/Command | t _{AH} /t _{CH} | 1.0 | | 1.0 | | 1.0 | | ns | |
| Data-in | t _{DH} | 0.5 | | 0.5 | | 0.5 | | ns | |

- NOTE:**
1. All timing parameters are referenced to V_{REF} or to the signal crossing points for different signals.
 2. Parameter only valid within one DQS/DQ group, e.g., DQS0, DQS0# and DQ0–DQ7; DQS1, DQS1# and DQ8–DQ15.
 3. The rising and falling edges of DVLD are referenced to falling edges of DQS.
 4. In Matched Impedance Mode, TBD cycles are required.



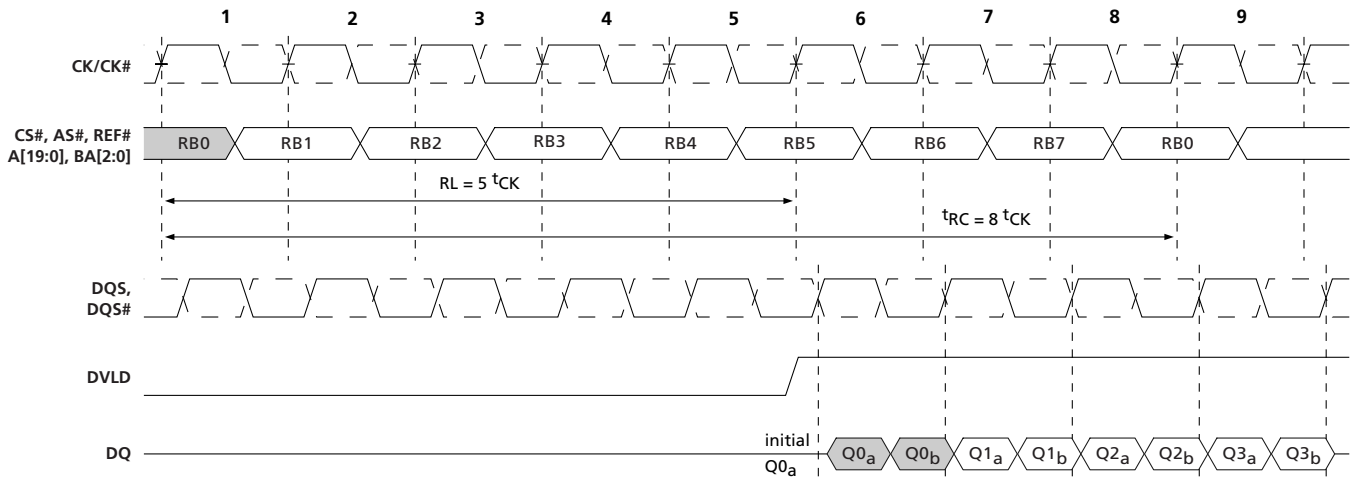
GENERAL OVERVIEW AND TIMING DEFINITION
(BL2/WL2)



- NOTE:**
1. Address A[19:0] and commands CS#, AS#, WE#, REF# are referenced to the rising edge of the clock CK.
 2. Input Data DQ is referenced to the rising or falling edge of the clock.
 3. DVLD is referenced to the falling edge of DQS.



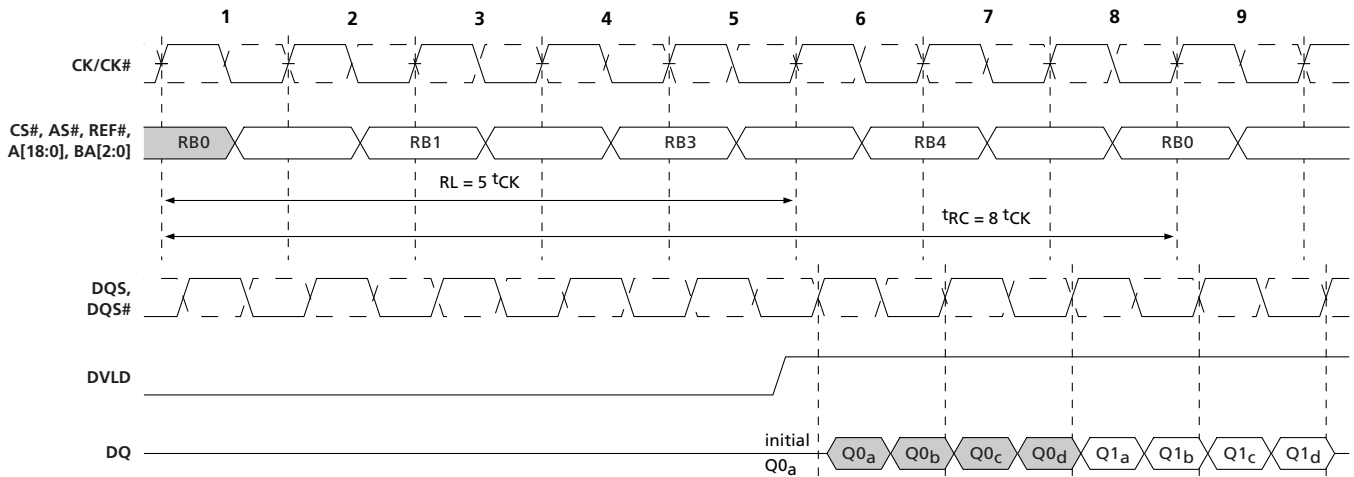
READ TIMING
(BL = 2)



- NOTE:**
1. Starting with all banks closed, 8 banks cyclic access.
 2. 2-bit prefetch, BL = 2.
 3. Read latency (RL) programmable.
 4. CS# = 1 deactivates command inputs. DQS and DQS# not affected.



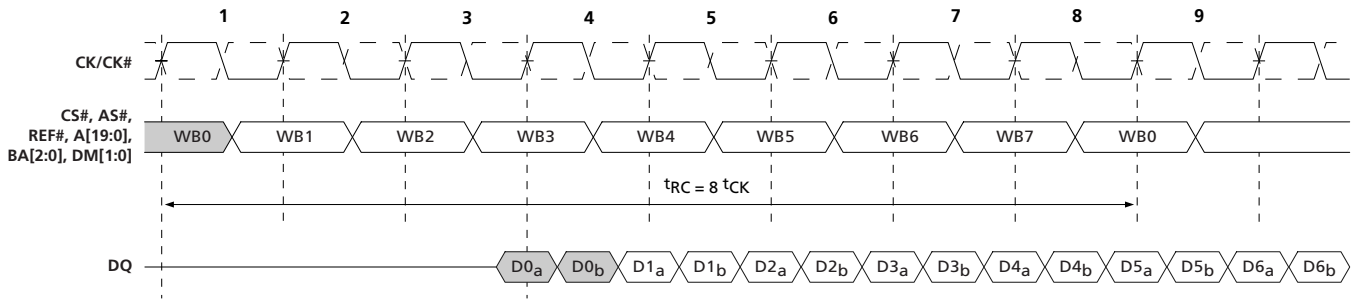
READ TIMING
(BL = 4)



- NOTE:**
1. Starting with all banks closed, 4 bank cyclic access.
 2. 4 bit prefetch, BL = 4.
 3. Read latency (RL) programmable.
 4. CS# = 1 deactivates command inputs. DQS not affected.



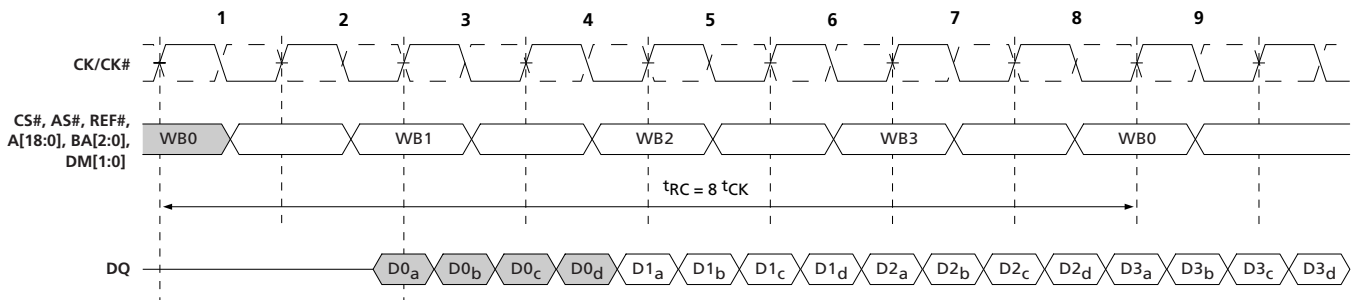
WRITE TIMING
(BL = 2, RL = 6)



- NOTE:**
1. DQS and DQS# are not relevant during WRITE cycles.
 2. Starting with all banks closed, 8 banks cyclic access.
 3. Write latency $WL = RL - BL/2 - 2 = 3$.



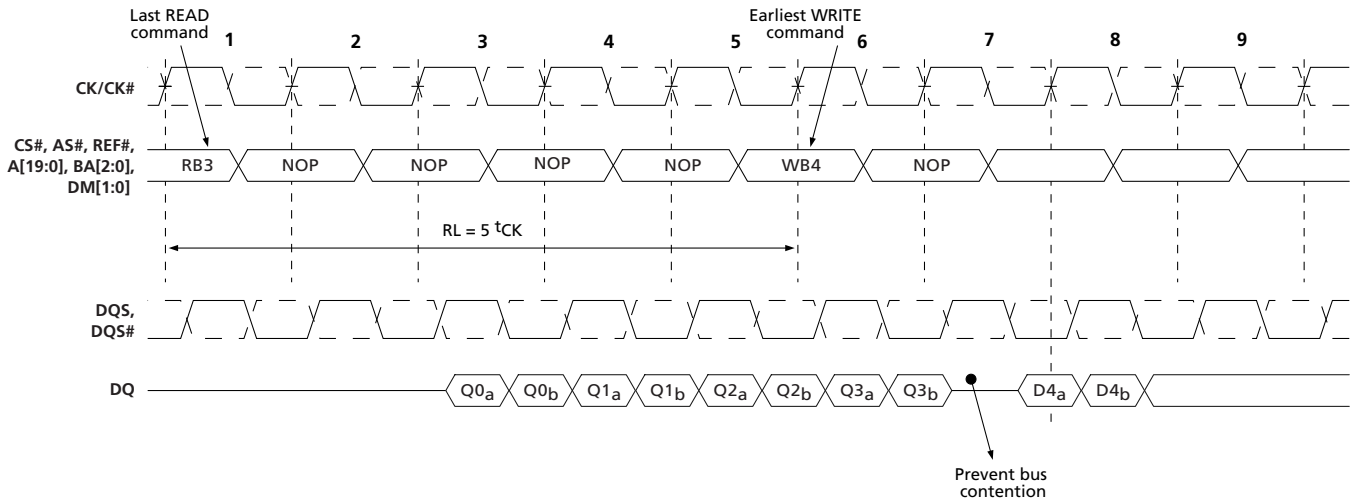
WRITE TIMING
(BL = 4, RL = 6)



- NOTE:**
1. DQS and DQS# are not relevant during WRITE cycles.
 2. Starting with all banks closed, 4 banks cyclic access.
 3. Write latency $WL = RL - BL/2 - 2 = 2$.



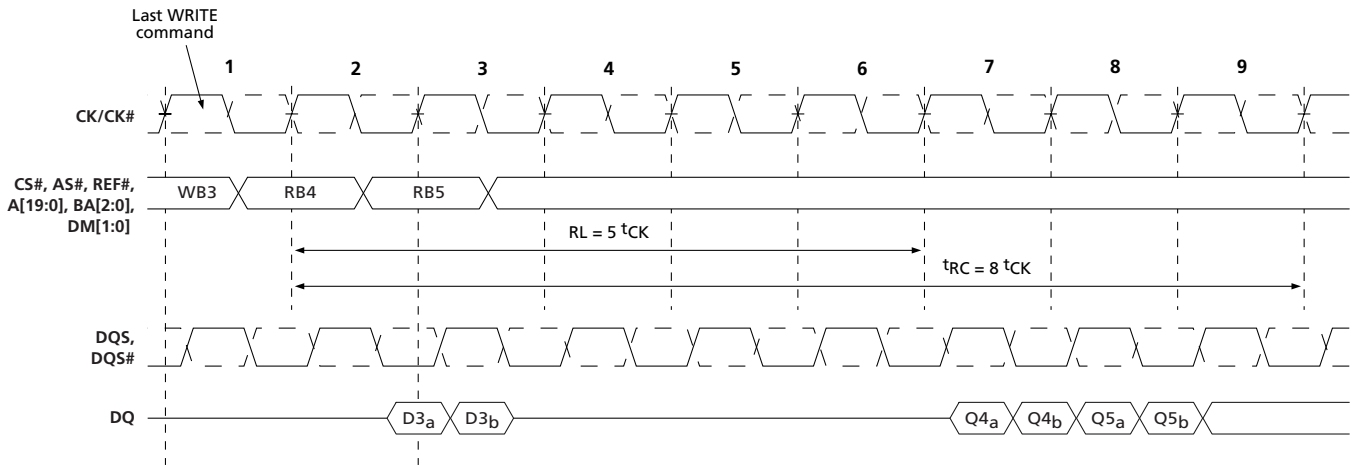
READ TO WRITE TIMING
(BL = 2, WL = 2)



NOTE: 1. In order to avoid bus contention from a READ to a WRITE the proper number of clock cycles has to be inserted.

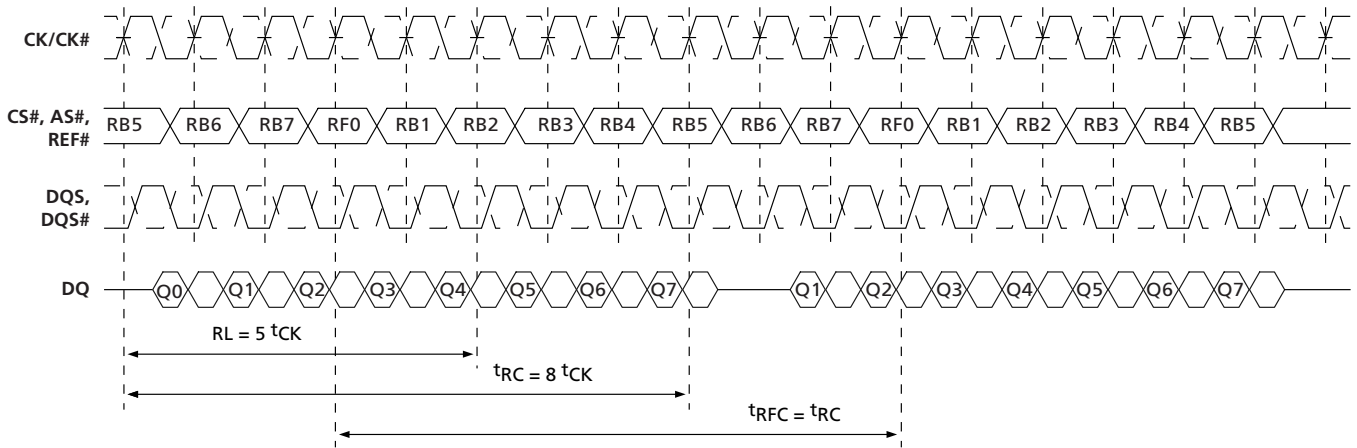


WRITE TO READ TIMING
(BL = 2, WL = 2)





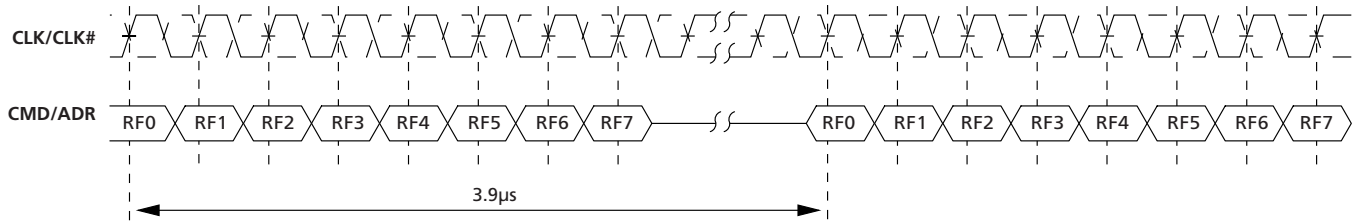
REFRESH TIMING



- NOTE:**
1. Bank scheduled refresh.
 2. Refresh cycle to be issued on closed bank.
 3. Bank address from controller, row address generated internally.



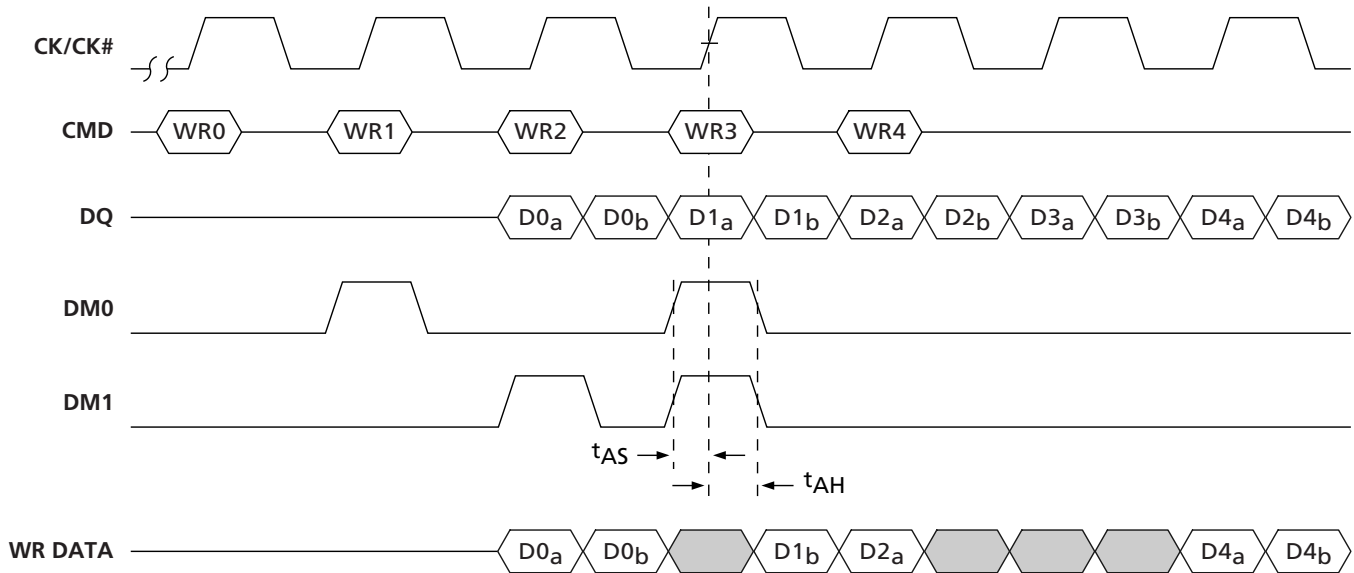
EXAMPLE OF REFRESH IMPLEMENTATION
(Cyclic Bank Burst Refresh)



- NOTE:**
1. Cyclic Burst refresh on all Banks.
 2. Each Refresh command on the next Bank is asserted on the next clock rising edge.
 3. Cycle for a burst refresh: $32\text{ms}/8192 = 3.9\mu\text{s}$.



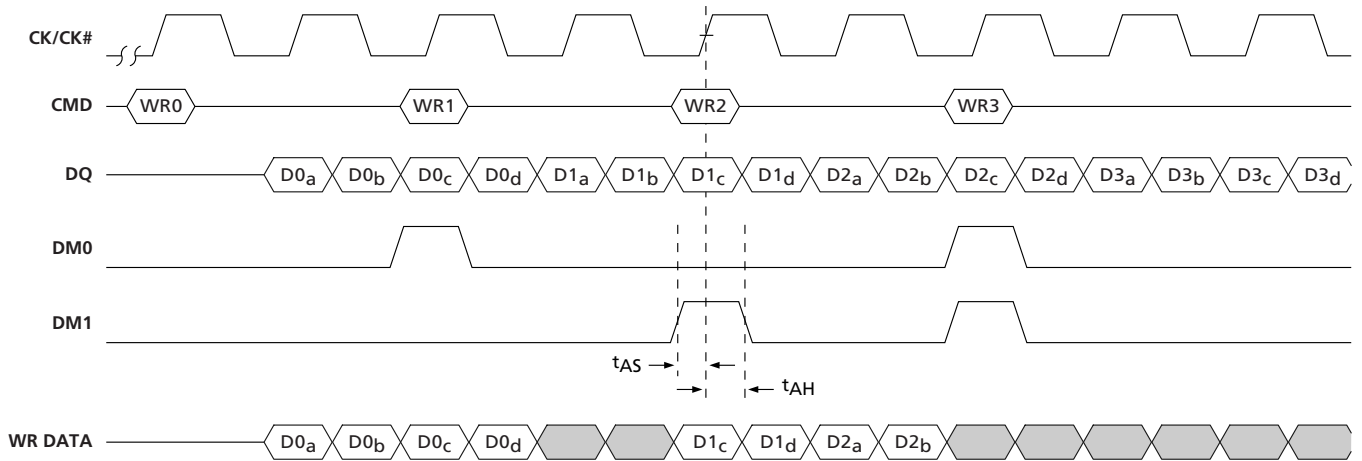
WRITE DATA MASK TIMING
(BL = 2, WL = 2)



NOTE: 1. Shaded WR Data is not written into the memory.



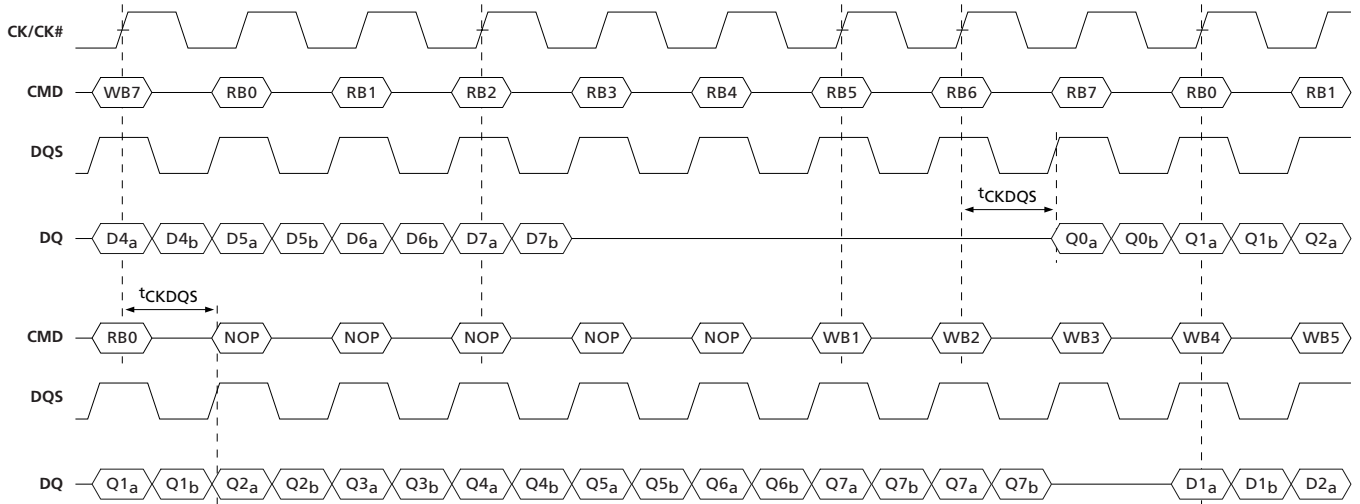
WRITE DATA MASK TIMING
(BL = 4, WL = 1)



NOTE: 1. Shaded WR Data is not written into the memory.

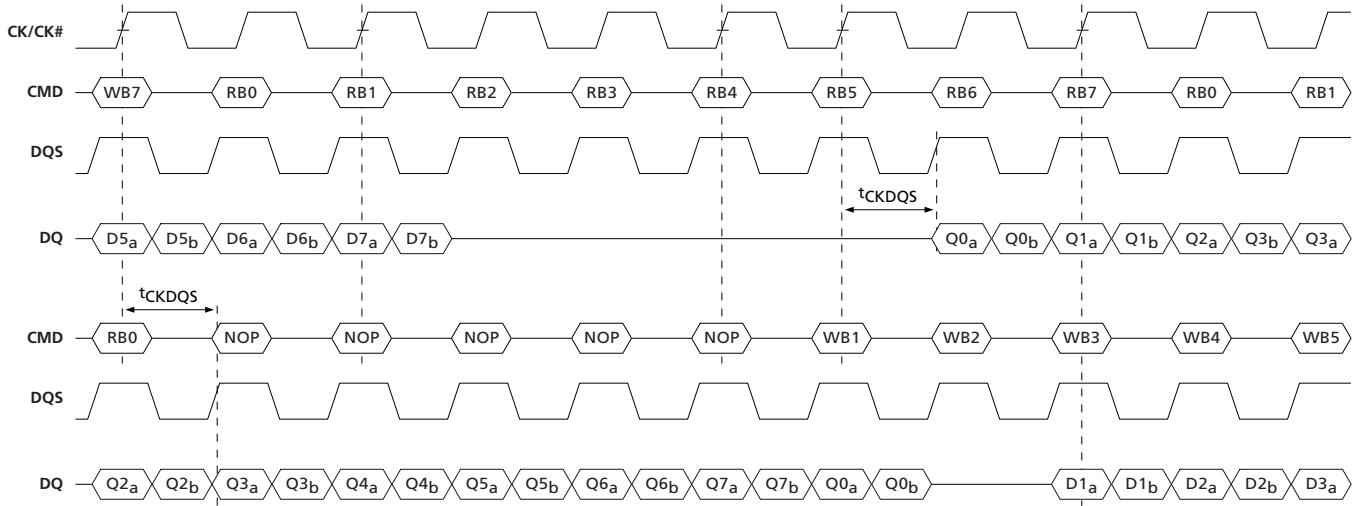


WRITE/READ AND READ/WRITE TIMING, CYCLIC BANK ACCESS
(RL = 6, BL = 2, WL = 3)



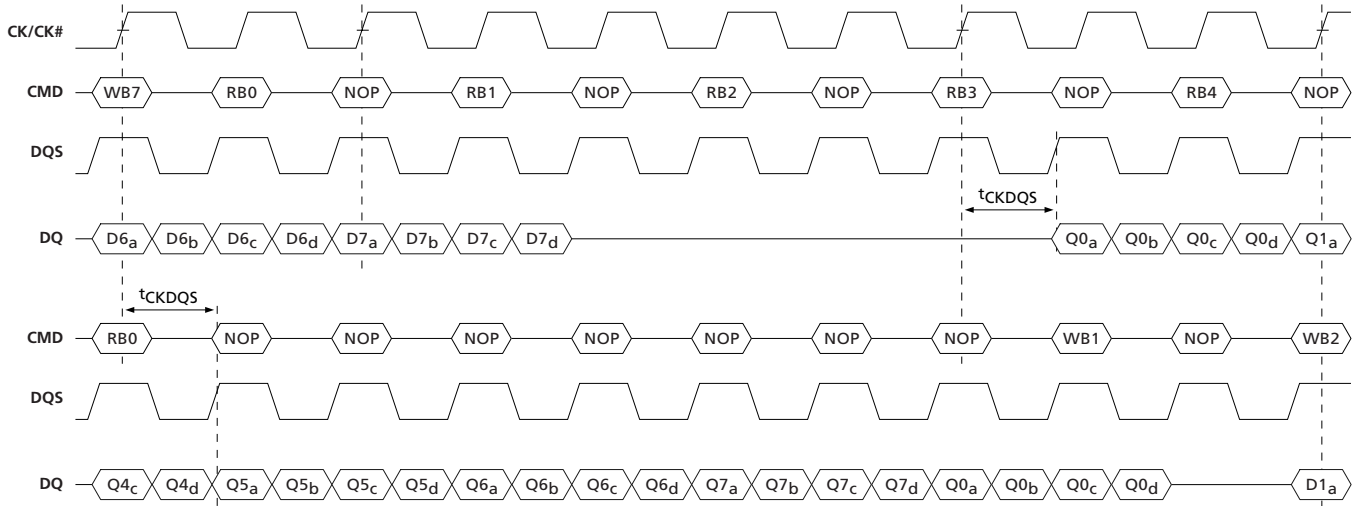


WRITE/READ AND READ/WRITE TIMING, CYCLIC BANK ACCESS
(RL = 5, BL = 2, WL = 2)



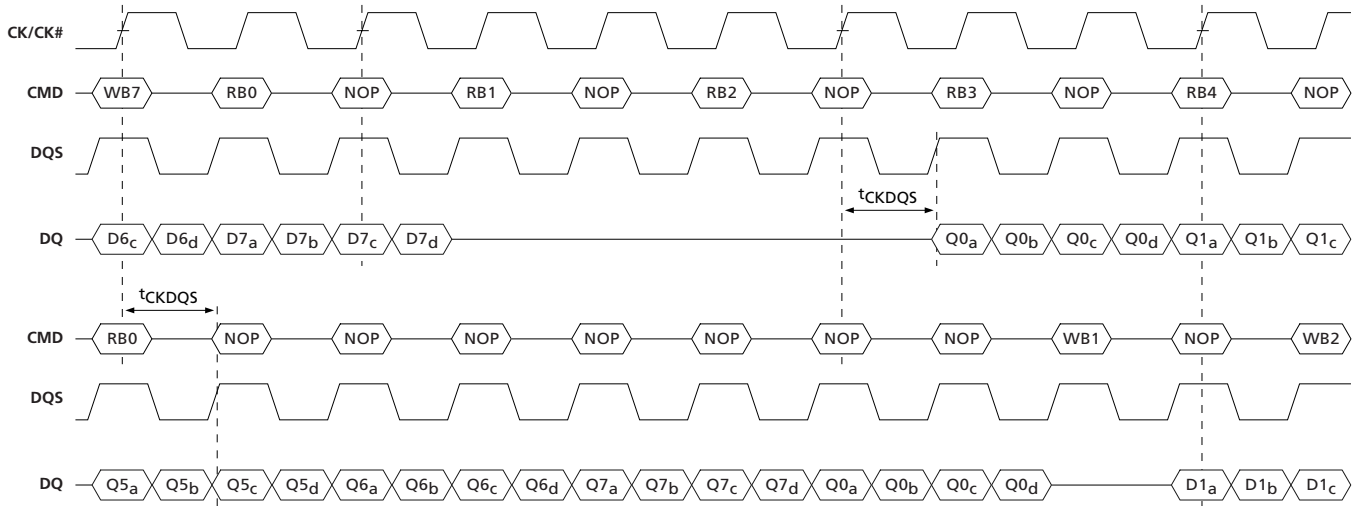


WRITE/READ AND READ/WRITE TIMING, CYCLIC BANK ACCESS
(RL = 6, BL = 4, WL = 2)



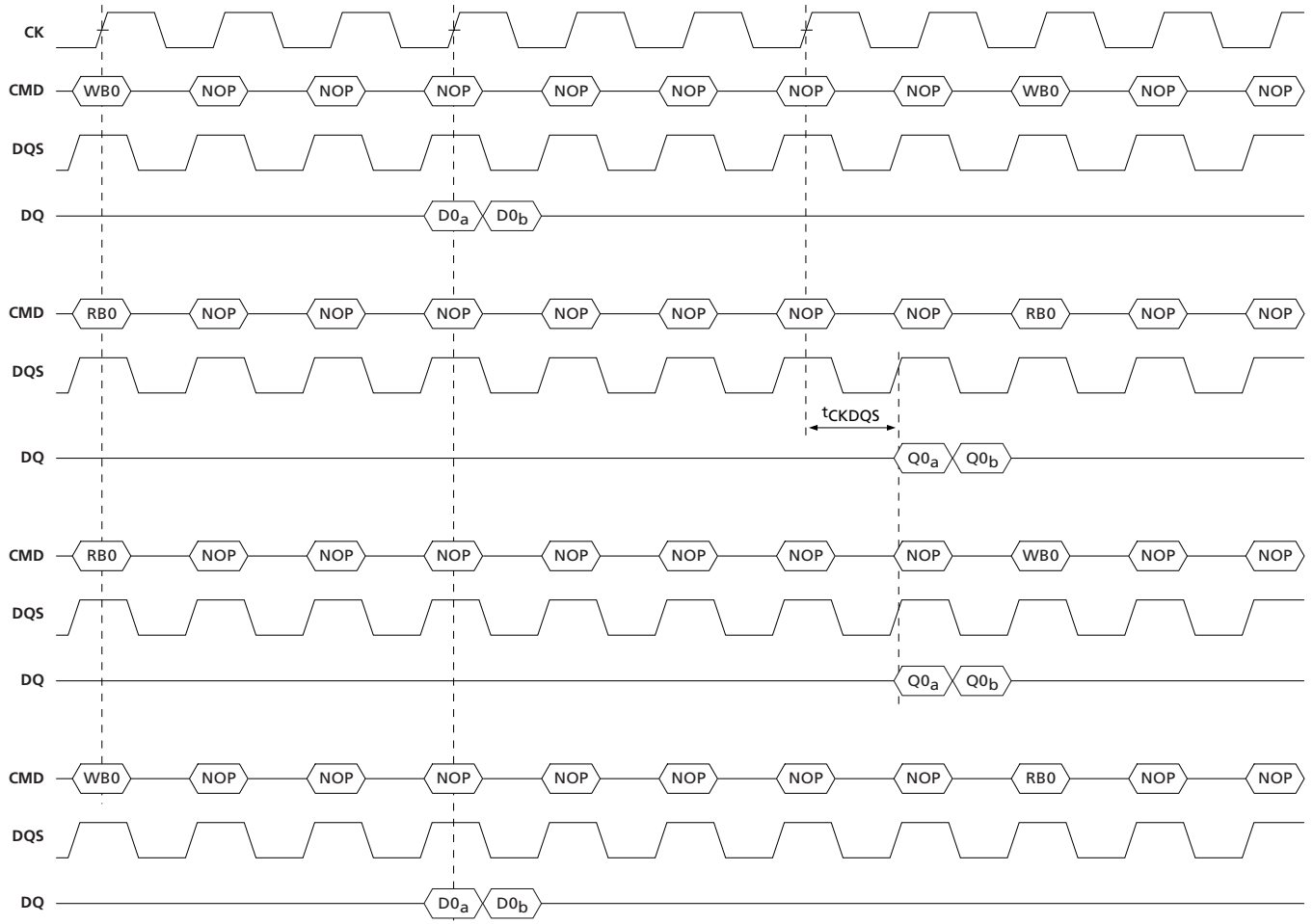


WRITE/READ AND READ/WRITE TIMING, CYCLIC BANK ACCESS
(RL = 5, BL = 4, WL = 1)



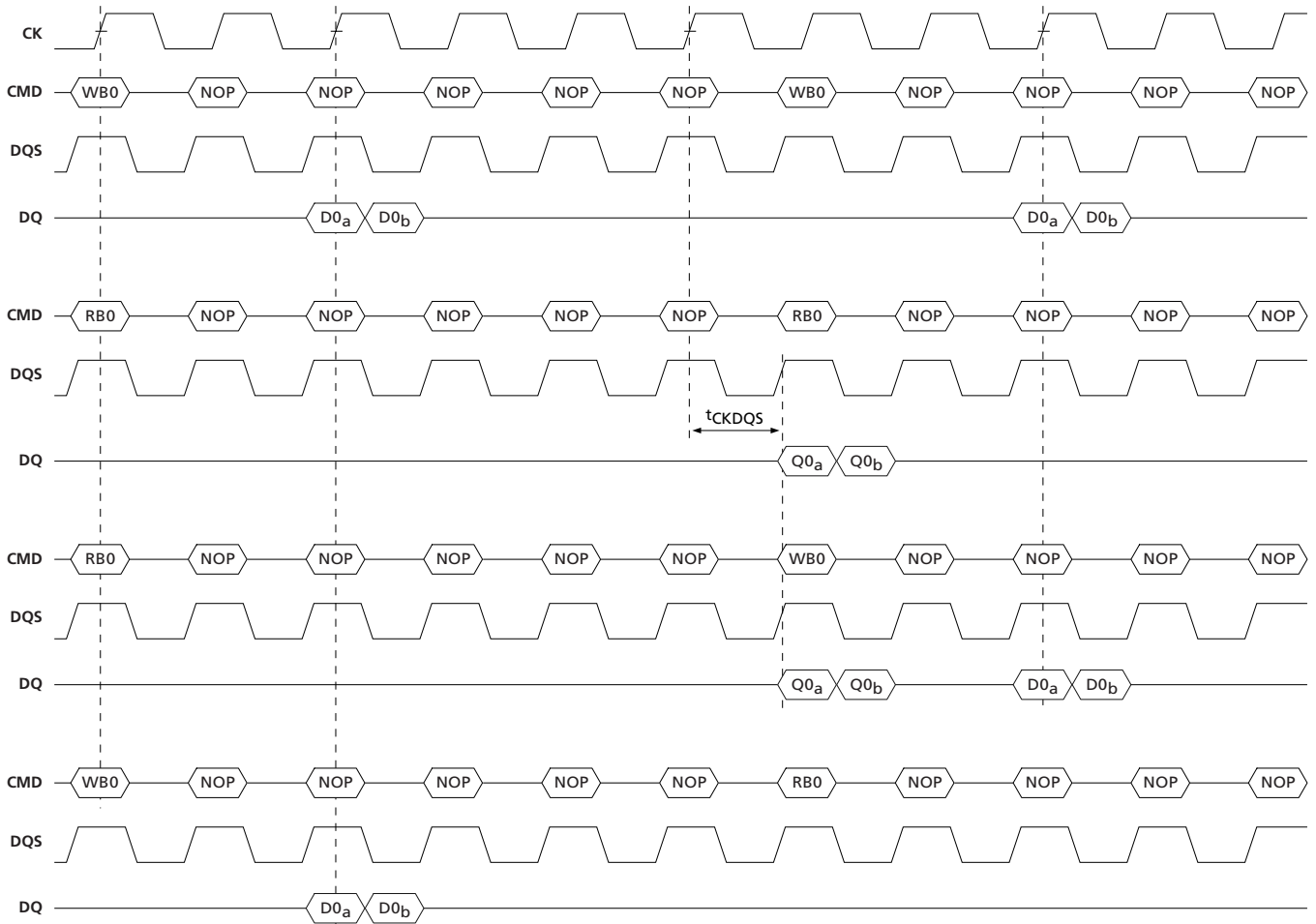


RANDOM ACCESS, SINGLE BANK
(RL = 6, BL = 2, WL = 3)



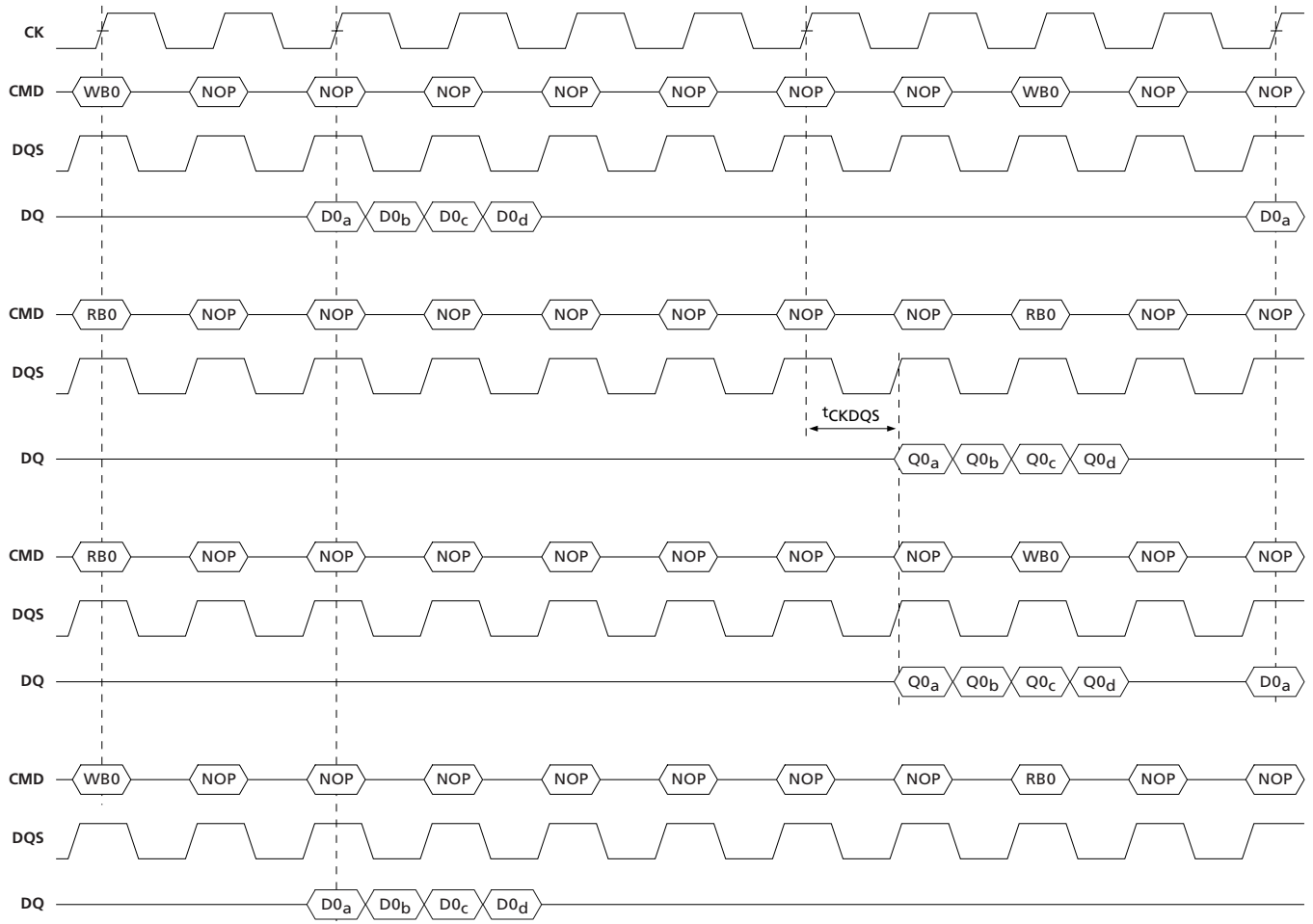


RANDOM ACCESS, SINGLE BANK
(RL = 5, BL = 2, WL = 2, t_{RC} = 6)



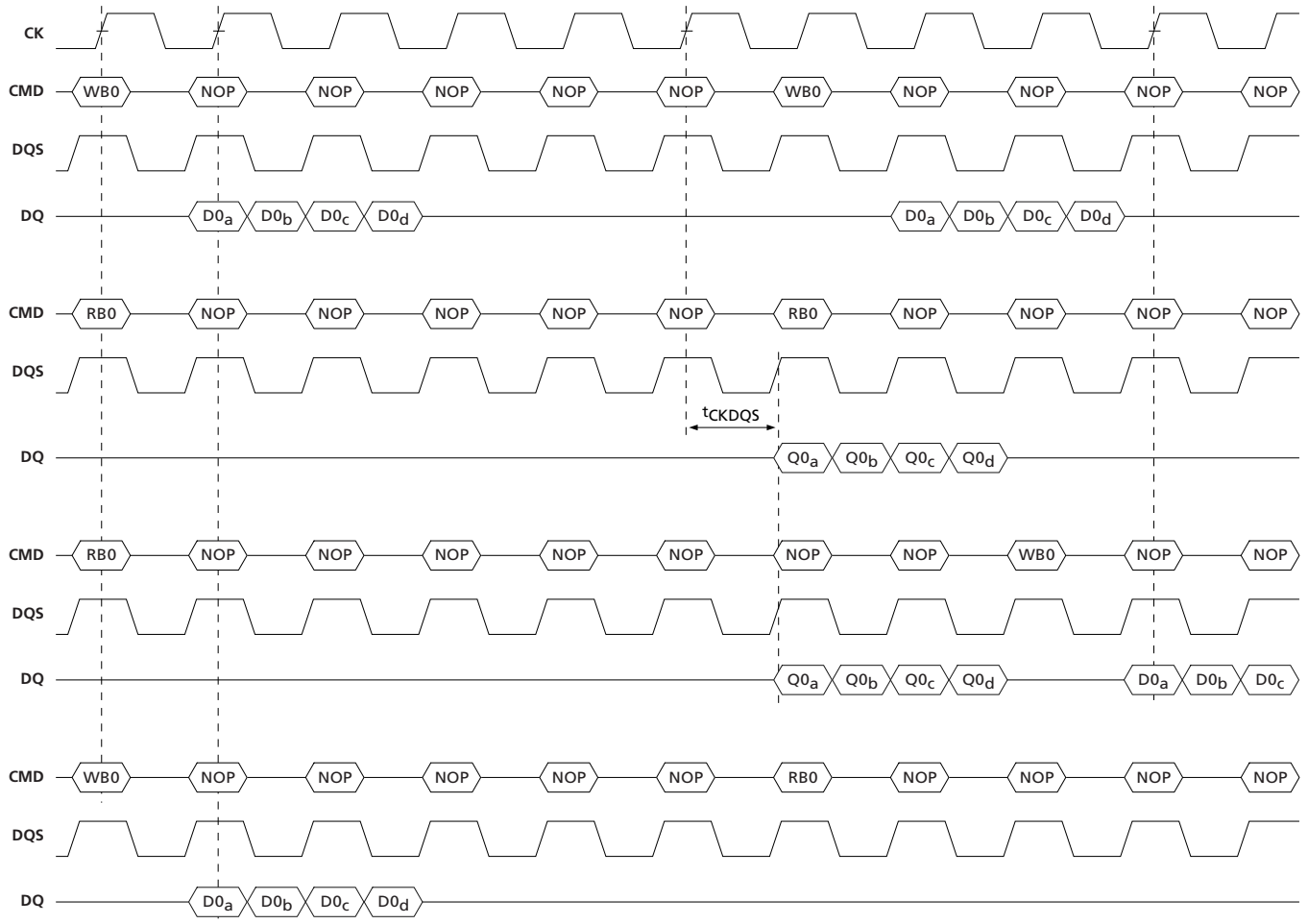


RANDOM ACCESS, SINGLE BANK
(RL = 6, BL = 4, WL = 2)



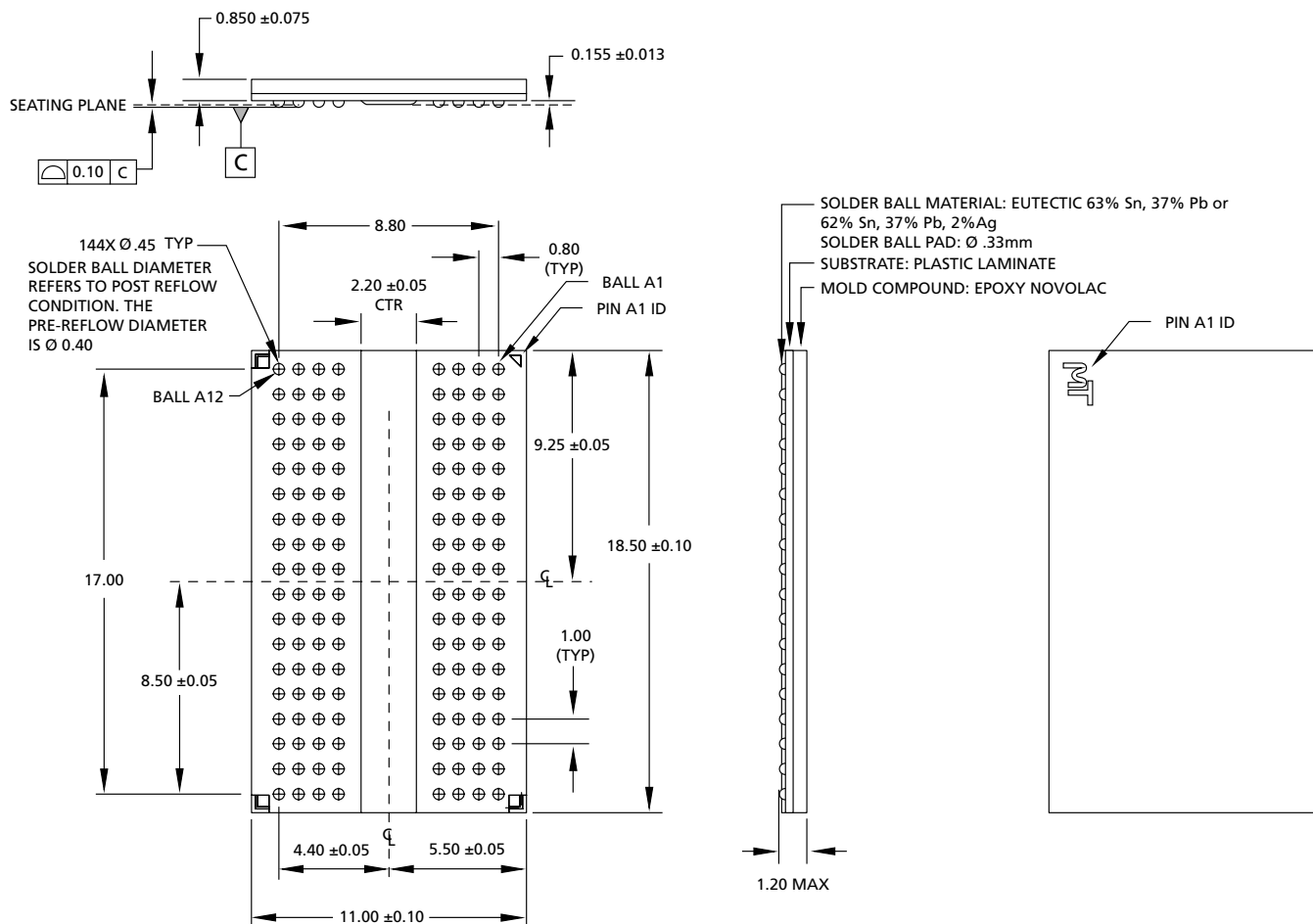


RANDOM ACCESS, SINGLE BANK
(RL = 5, BL = 4, WL = 1, t_{RC} = 6)





144-BALL T-FBGA



NOTE: 1. All dimensions in millimeters.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

E-mail: prodmktg@micron.com, Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992

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Rev. 3, Advance 6/02
• Removed confidential mark

Rev. 2, Advance 2/02
• ?
• ?

Original document, Advance 12/01