# DRAM

# 1 MEG x 4 DRAM

## STANDARD OR SELF REFRESH



## FEATURES

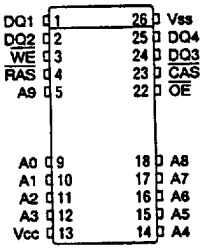
- 1,024-cycle refresh distributed across 16ms (MT4C4001J) or 128ms (MT4C4001J S)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes (MT4C4001J S only)
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C4001J S)

## OPTIONS / MARKING

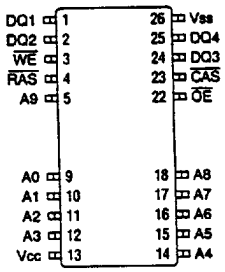
- Timing
  - 60ns access: -6
  - 70ns access: -7
  - 80ns access: -8
- Packages
  - Plastic SOJ (300 mil): DJ
  - Plastic TSOP (300 mil): TG
- Version
  - 1,024-cycle refresh in 16ms: None
  - 1,024-cycle refresh in 128ms: S
- Part Number Example: MT4C4001JDJ-6 S

## PIN ASSIGNMENT (Top View)

### 20/26-Pin SOJ
(DC-1)




### 20/26-Pin TSOP
(DD-1)




## GENERAL DESCRIPTION

The MT4C4001J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, the outputs (Qs) are activated and retain the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the

$\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms for the MT4C4001J and every 128ms for the MT4C4001J S, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

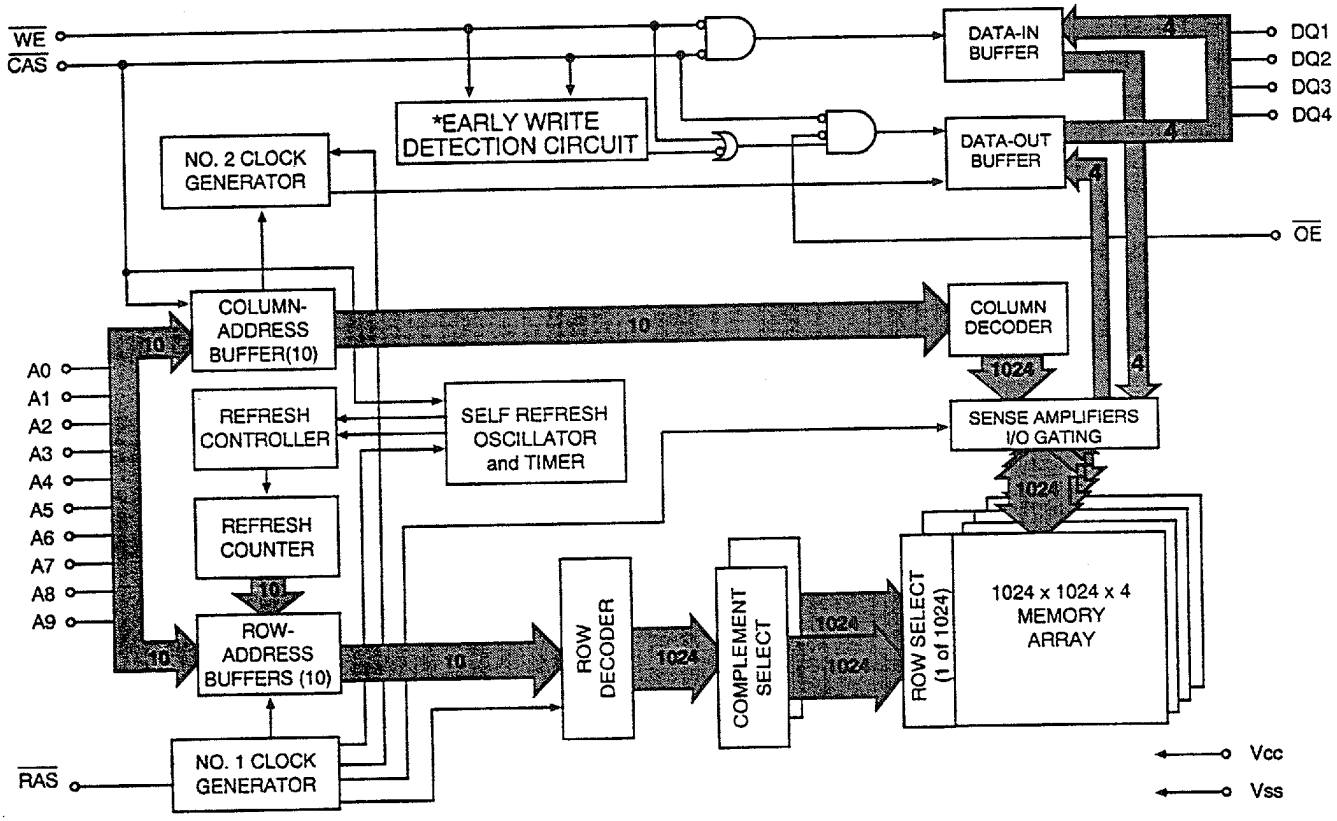
## REFRESH

An optional SELF REFRESH mode is also available. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified $^{t}$RASS. Additionally, the "S" option allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of $^{t}$RPS (=$^{t}$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or BURST REFRESH sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

## FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE




***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

## TRUTH TABLE

| FUNCTION | | RAS | CAS | WE | OE | ADDRESSES | | DATA-IN/OUT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | $^tR$ | $^tC$ | DQ1-DQ4 |
| Standby | | H | H→X | X | X | X | X | High-Z |
| READ | | L | L | H | L | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | X | ROW | COL | Data-In |
| READ WRITE | | L | L | H→L | L→H | ROW | COL | Data-Out, Data-In |
| FAST-PAGE-MODE READ | 1st Cycle | L | H→L | H | L | ROW | COL | Data-Out |
| | 2nd Cycle | L | H→L | H | L | n/a | COL | Data-Out |
| FAST-PAGE-MODE EARLY-WRITE | 1st Cycle | L | H→L | L | X | ROW | COL | Data-In |
| | 2nd Cycle | L | H→L | L | X | n/a | COL | Data-In |
| FAST-PAGE-MODE READ-WRITE | 1st Cycle | L | H→L | H→L | L→H | ROW | COL | Data-Out, Data-In |
| | 2nd Cycle | L | H→L | H→L | L→H | n/a | COL | Data-Out, Data-In |
| RAS ONLY REFRESH | | L | H | X | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | L | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | X | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | X | High-Z |
| SELF REFRESH (MT4C4001J S only) | | H→L | L | H | X | X | X | High-Z |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 4.5 | 5.5 | V | |
| Input High (Logic 1) Voltage, all inputs | VIH | 2.4 | Vcc+1 | V | |
| Input Low (Logic 0) Voltage, all inputs | VIL | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ VIN ≤ 6.5V<br>(All other pins not under test = 0V) | II | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) | IOZ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage (IOUT = -5mA) | VOH | 2.4 | | V | |
| Output Low Voltage (IOUT = 4.2mA) | VOL | | 0.4 | V | |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) ($V_{CC}$ = +5V ±10%)

| PARAMETER/CONDITION | VERSION | SYMBOL | MAX -6 | MAX -7 | MAX -8 | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | | $I_{CC1}$ | 2 | 2 | 2 | mA | |
| STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ -0.2V) | MT4C4001J | $I_{CC2}$ | 1 | 1 | 1 | mA | |
| | MT4C4001J S | $I_{CC2}$ | 200 | 200 | 200 | µA | |
| OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: $^tRC$ = $^tRC$ [MIN]) | | $I_{CC3}$ | 110 | 100 | 90 | mA | 3, 4, 30 |
| OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling: $^tPC$ = $^tPC$ [MIN]) | | $I_{CC4}$ | 80 | 70 | 60 | mA | 3, 4, 30 |
| REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | | $I_{CC5}$ | 110 | 100 | 90 | mA | 3, 30 |
| REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | | $I_{CC6}$ | 110 | 100 | 90 | mA | 3, 5 |
| REFRESH CURRENT: Extended Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = $^tRAS$ (MIN); $\overline{WE}$, A0-A9 and $D_{IN}$ = Vcc -0.2V or 0.2V; ($D_{IN}$ may be left open); $^tRC$ = 125µs (1,024 rows at 125µs = 128ms) | MT4C4001J S | $I_{CC7}$ | 300 | 300 | 300 | µA | 3, 5, 28 |
| SELF REFRESH CURRENT: Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq ^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -.2; A0-A9 and $D_{IN}$ = Vcc -.2V or .2V ($D_{IN}$ may be left open) | MT4C4001J S | $I_{CC8}$ | 300 | 300 | 300 | µA | 5, 31 |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A9 | $C_{I1}$ | | 5 | pF | 2 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | $C_{I2}$ | | 7 | pF | 2 |
| Input/Output Capacitance: DQ | $C_{IO}$ | | 7 | pF | 2 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

| AC CHARACTERISTICS | | -6 | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Random READ or WRITE cycle time | tRC | 110 | | 130 | | 150 | | ns | |
| READ WRITE cycle time | tRWC | 150 | | 180 | | 200 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | tPC | 35 | | 40 | | 45 | | ns | |
| FAST-PAGE-MODE READ-WRITE cycle time | tPRWC | 85 | | 100 | | 105 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 60 | | 70 | | 80 | ns | 14 |
| Access time from $\overline{CAS}$ | tCAC | | 15 | | 20 | | 20 | ns | 15 |
| Output Enable | tOE | | 15 | | 20 | | 20 | ns | 23 |
| Access time from column-address | tAA | | 30 | | 35 | | 40 | ns | |
| Access time from $\overline{CAS}$ precharge | tCPA | | 35 | | 40 | | 45 | ns | |
| $\overline{RAS}$ pulse width | tRAS | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ pulse width (FAST PAGE MODE) | tRASP | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ hold time | tRSH | 15 | | 20 | | 20 | | ns | |
| $\overline{RAS}$ precharge time | tRP | 40 | | 50 | | 60 | | ns | |
| $\overline{CAS}$ pulse width | tCAS | 15 | 100,000 | 20 | 100,000 | 20 | 100,000 | ns | |
| $\overline{CAS}$ hold time | tCSH | 60 | | 70 | | 80 | | ns | |
| $\overline{CAS}$ precharge time (CBR REFRESH) | tCPN | 10 | | 10 | | 10 | | ns | 16 |
| $\overline{CAS}$ precharge time (FAST PAGE MODE) | tCP | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 20 | 45 | 20 | 50 | 20 | 60 | ns | 17 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | tCRP | 10 | | 10 | | 10 | | ns | |
| Row-address setup time | tASR | 0 | | 0 | | 0 | | ns | |
| Row-address hold time | tRAH | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ to column-address delay time | tRAD | 15 | 30 | 15 | 35 | 15 | 40 | ns | 18 |
| Column-address setup time | tASC | 0 | | 0 | | 0 | | ns | |
| Column-address hold time | tCAH | 10 | | 15 | | 15 | | ns | |
| Column-address hold time (referenced to $\overline{RAS}$) | tAR | 45 | | 50 | | 55 | | ns | |
| Column-address to $\overline{RAS}$ lead time | tRAL | 30 | | 35 | | 40 | | ns | |
| Read command setup time | tRCS | 0 | | 0 | | 0 | | ns | |
| Read command hold time (referenced to $\overline{CAS}$) | tRCH | 0 | | 0 | | 0 | | ns | 19 |
| Read command hold time (referenced to $\overline{RAS}$) | tRRH | 0 | | 0 | | 0 | | ns | 19 |
| $\overline{CAS}$ to output in Low-Z | tCLZ | 0 | | 0 | | 0 | | ns | |
| Output buffer turn-off delay | tOFF | 3 | 15 | 3 | 20 | 3 | 20 | ns | 20, 29 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

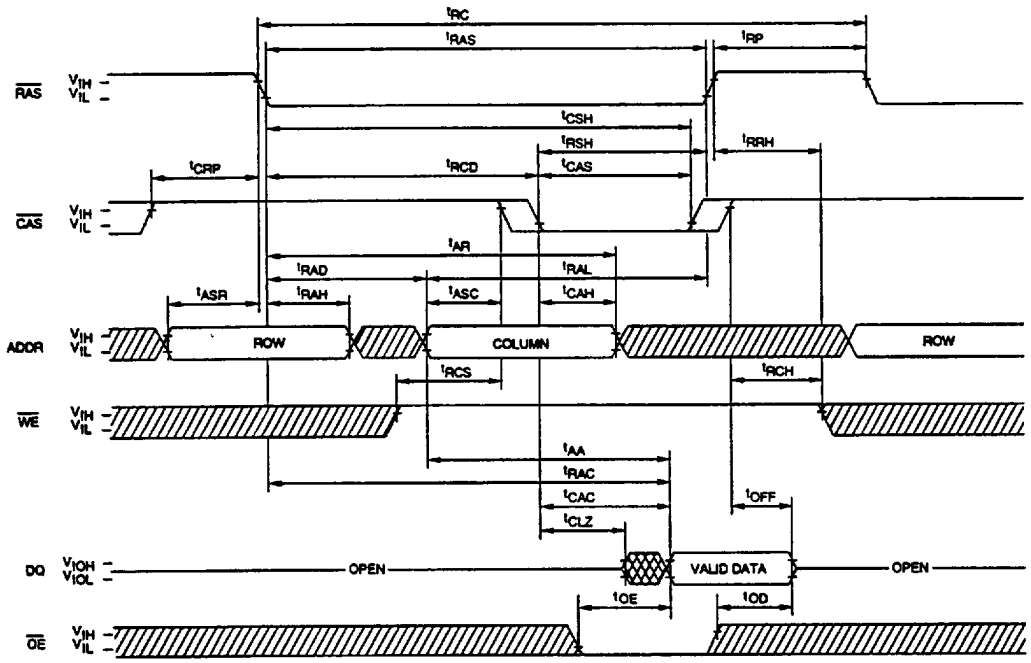
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

| AC CHARACTERISTICS | | -6 | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| $\overline{WE}$ command setup time | $t_{WCS}$ | 0 | | 0 | | 0 | | ns | 21, 27 |
| Write command hold time | $t_{WCH}$ | 10 | | 15 | | 15 | | ns | |
| Write command hold time (referenced to $\overline{RAS}$) | $t_{WCR}$ | 45 | | 55 | | 60 | | ns | |
| Write command pulse width | $t_{WP}$ | 10 | | 15 | | 15 | | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 15 | | 20 | | 20 | | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 15 | | 20 | | 20 | | ns | |
| Data-in setup time | $t_{DS}$ | 0 | | 0 | | 0 | | ns | 22 |
| Data-in hold time | $t_{DH}$ | 10 | | 15 | | 15 | | ns | 22 |
| Data-in hold time (referenced to $\overline{RAS}$) | $t_{DHR}$ | 45 | | 55 | | 60 | | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 90 | | 100 | | 110 | | ns | 21 |
| Column-address to $\overline{WE}$ delay time | $t_{AWD}$ | 55 | | 65 | | 70 | | ns | 21 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 40 | | 50 | | 50 | | ns | 21 |
| Transition time (rise or fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 9, 10 |
| Refresh period (1,024 cycles) MT4C4001J / MT4C4001J S | $t_{REF}$ | | 16 / 128 | | 16 / 128 | | 16 / 128 | ms | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns | |
| $\overline{CAS}$ setup time (CBR REFRESH) | $t_{CSR}$ | 10 | | 10 | | 10 | | ns | 5 |
| $\overline{CAS}$ hold time (CBR REFRESH) | $t_{CHR}$ | 10 | | 10 | | 10 | | ns | 5 |
| $\overline{WE}$ hold time (CBR REFRESH) | $t_{WRH}$ | 10 | | 10 | | 10 | | ns | 25 |
| $\overline{WE}$ setup time (CBR REFRESH) | $t_{WRP}$ | 10 | | 10 | | 10 | | ns | 25 |
| $\overline{WE}$ hold time (WCBR test cycle) | $t_{WTH}$ | 10 | | 10 | | 10 | | ns | 25 |
| $\overline{WE}$ setup time (WCBR test cycle) | $t_{WTS}$ | 10 | | 10 | | 10 | | ns | 25 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | $t_{ORD}$ | 0 | | 0 | | 0 | | ns | |
| Output disable | $t_{OD}$ | | 15 | | 20 | | 20 | ns | 27 |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | $t_{OEH}$ | 15 | | 20 | | 20 | | ns | 26 |
| $\overline{RAS}$ pulse width during SELF REFRESH cycle | $t_{RASS}$ | 100 | | 100 | | 100 | | µs | 31 |
| $\overline{RAS}$ precharge time during SELF REFRESH cycle | $t_{RPS}$ | 110 | | 130 | | 150 | | ns | 31 |
| $\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle | $t_{CHD}$ | 10 | | 10 | | 10 | | ns | 31 |

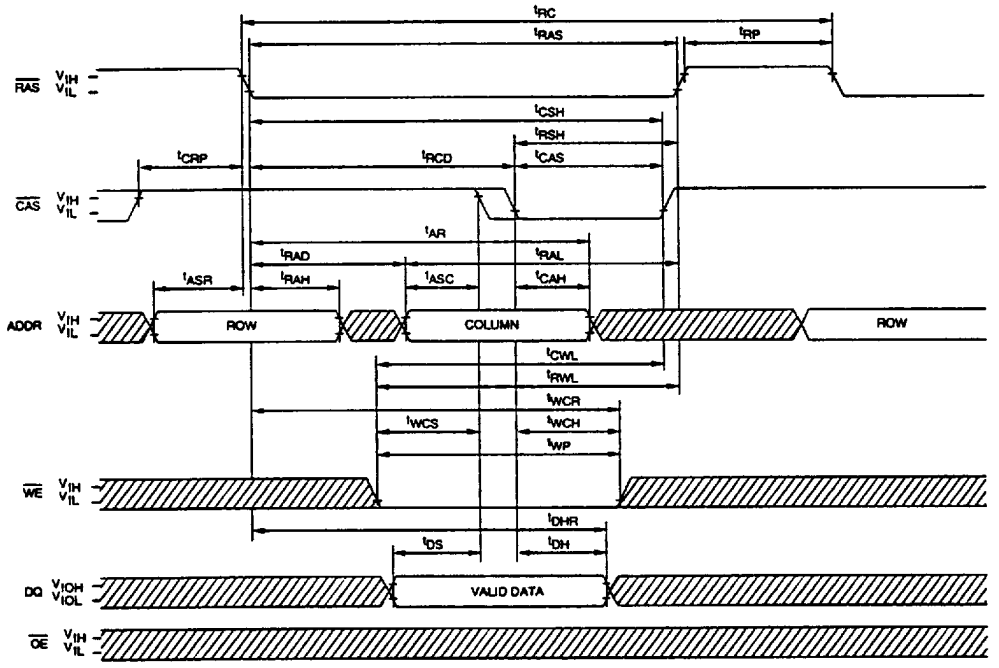
## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = 5V ±10%; f = 1 MHz.
3. $I_{CC}$ is dependent on cycle rates.
4. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $^{t}REF$ refresh requirement is exceeded.
8. AC characteristics assume $^{t}T$ = 5ns.
9. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
10. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
11. If $\overline{CAS}$ = $V_{IH}$, data output is High-Z.
12. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If $^{t}RCD$ is greater than the maximum recommended value shown in this table, $^{t}RAC$ will increase by the amount that $^{t}RCD$ exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for $^{t}CPN$.
17. Operation within the $^{t}RCD$ (MAX) limit ensures that $^{t}RAC$ (MAX) can be met. $^{t}RCD$ (MAX) is specified as a reference point only; if $^{t}RCD$ is greater than the specified $^{t}RCD$ (MAX) limit, then access time is controlled exclusively by $^{t}CAC$.
18. Operation within the $^{t}RAD$ (MAX) limit ensures that $^{t}RAC$ (MIN) and $^{t}CAC$ (MIN) can be met. $^{t}RAD$ (MAX) is specified as a reference point only; if $^{t}RAD$ is greater than the specified $^{t}RAD$ (MAX) limit, then access time is controlled exclusively by $^{t}AA$.
19. Either $^{t}RCH$ or $^{t}RRH$ must be satisfied for a READ cycle.
20. $^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to $V_{OH}$ or $V_{OL}$.
21. $^{t}WCS$, $^{t}RWD$, $^{t}AWD$ and $^{t}CWD$ are not restrictive operating parameters. $^{t}WCS$ applies to EARLY WRITE cycles. $^{t}RWD$, $^{t}AWD$ and $^{t}CWD$ apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. $^{t}WCS$, $^{t}RWD$, $^{t}CWD$ and $^{t}AWD$ are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. $^{t}WTS$ and $^{t}WTH$ are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of $^{t}WRP$ and $^{t}WRH$ in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^{t}OD$ and $^{t}OEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once $^{t}OD$ or $^{t}OFF$ occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. Extended refresh current is reduced as $^{t}RAS$ is reduced from its maximum specification during the extended refresh cycle.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.
31. If the DRAM controller uses a BURST REFRESH, a BURST REFRESH of all rows must be executed upon exiting SELF REFRESH.

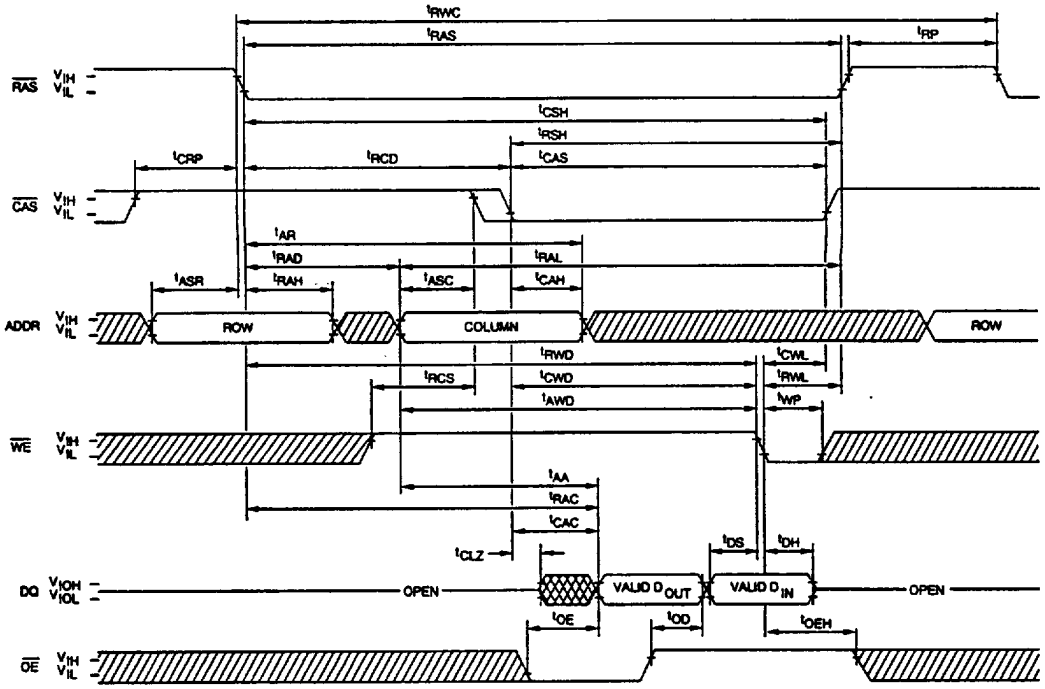
## READ CYCLE



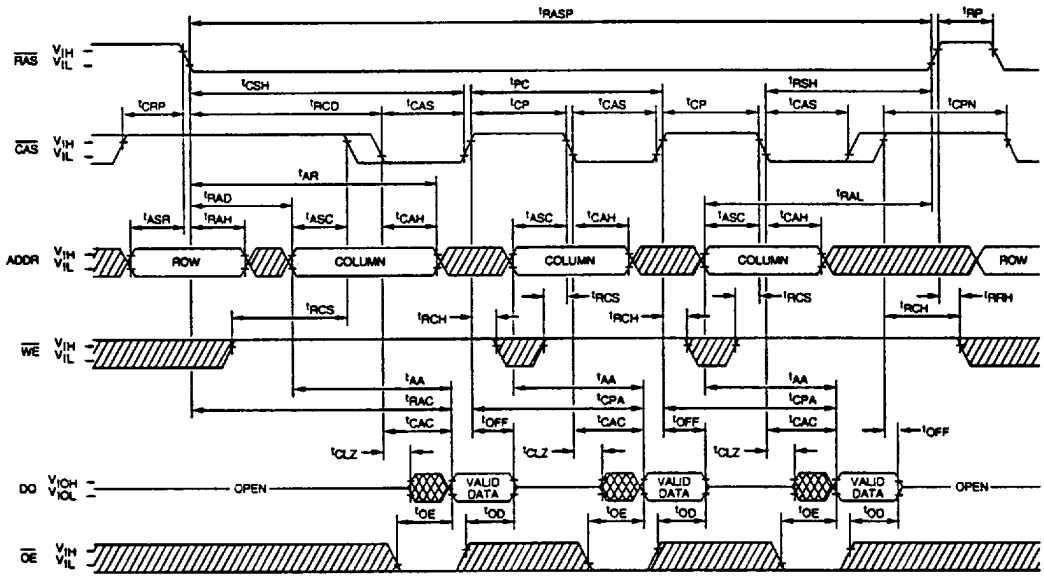

## EARLY WRITE CYCLE



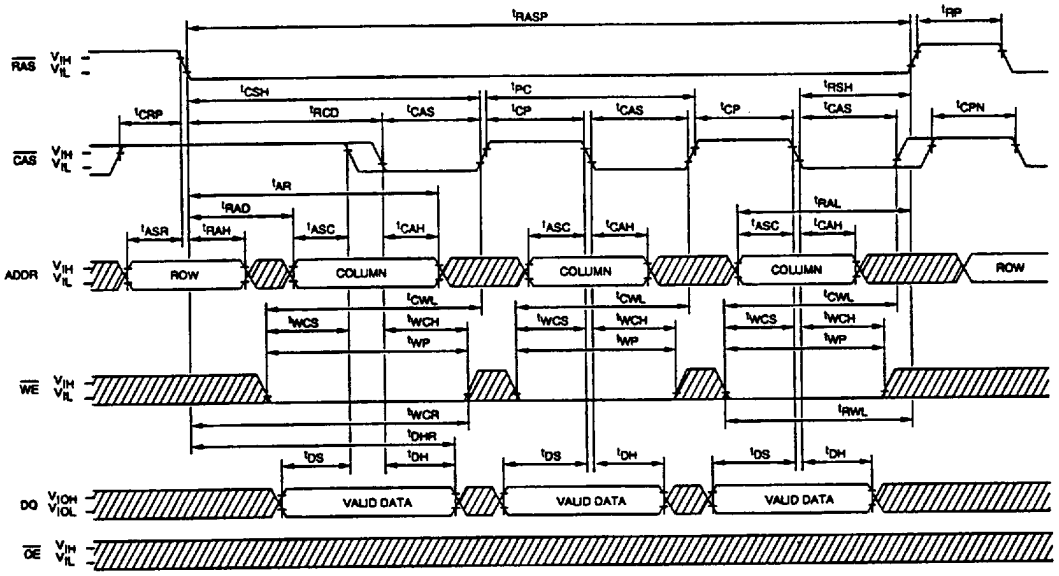
## READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



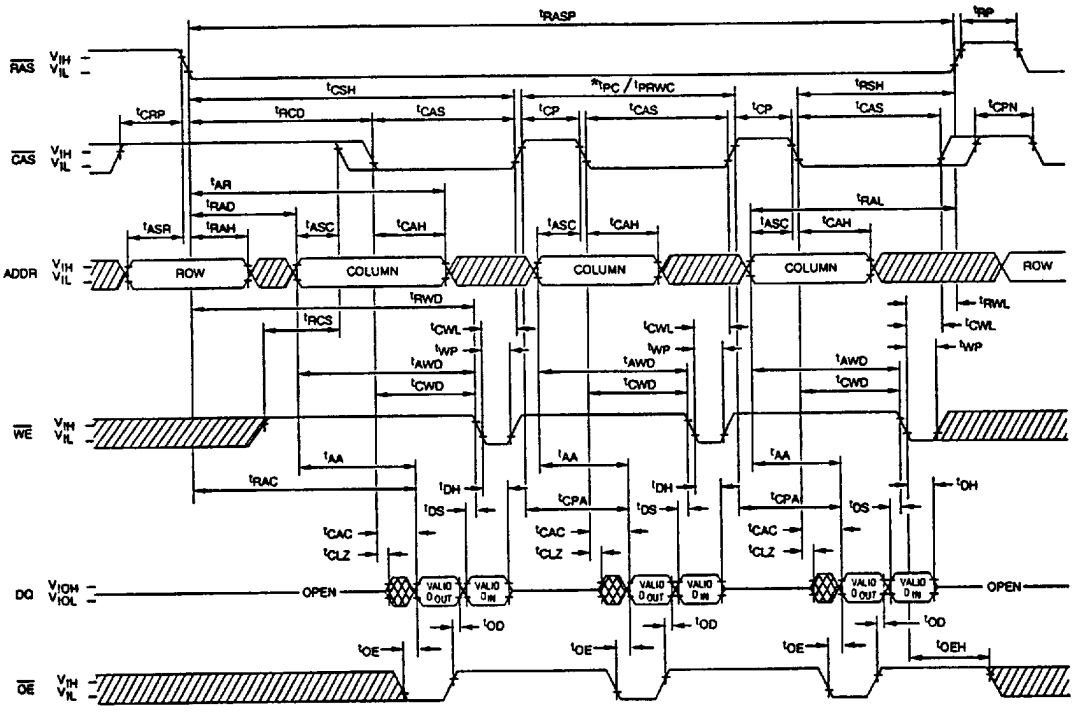

## FAST-PAGE-MODE READ CYCLE



## FAST-PAGE-MODE EARLY-WRITE CYCLE




## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

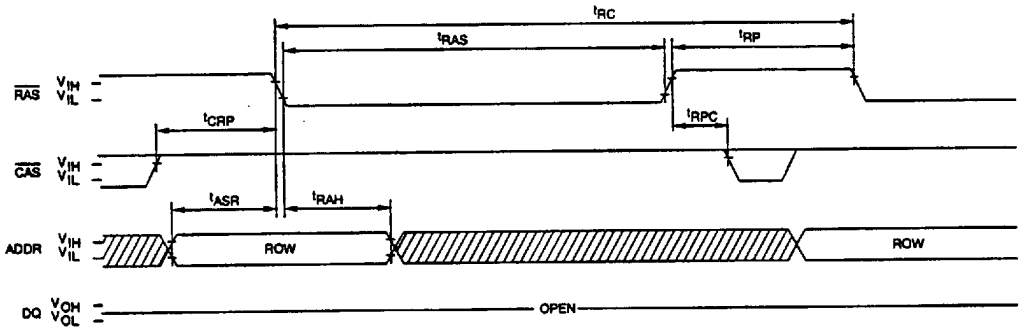



DON'T CARE

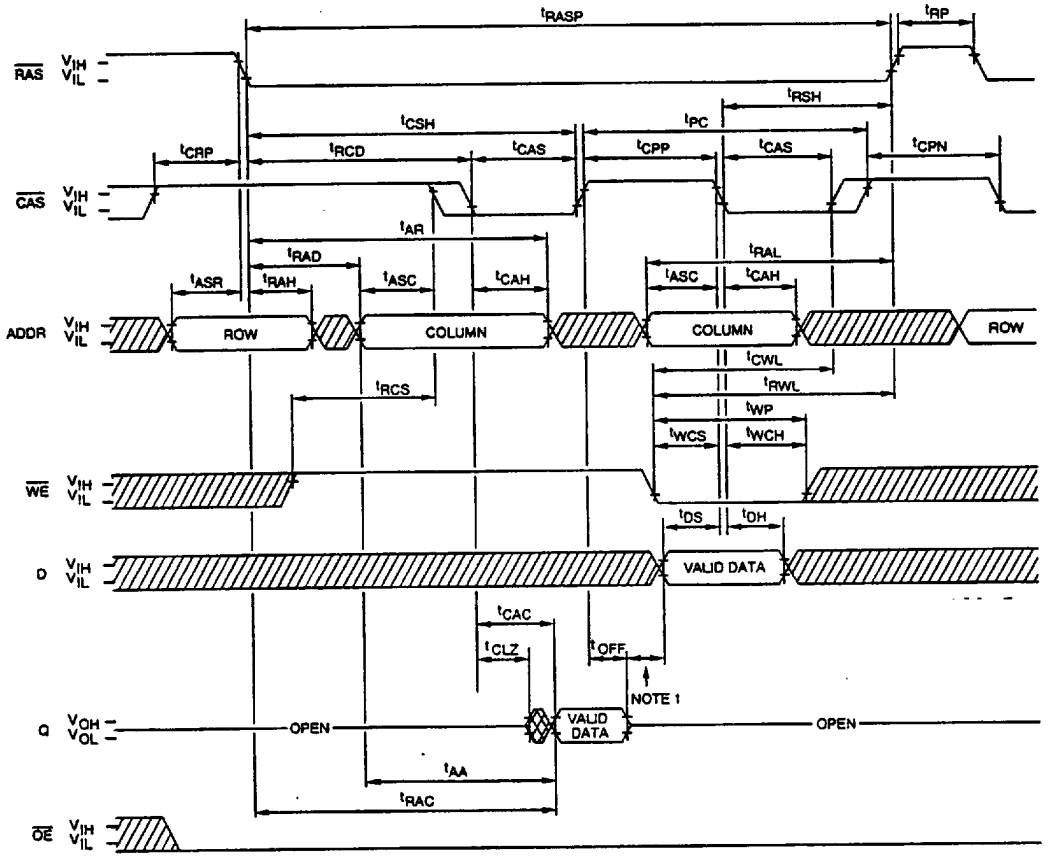
UNDEFINED

*tPC is for LATE WRITE only.

## $\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)

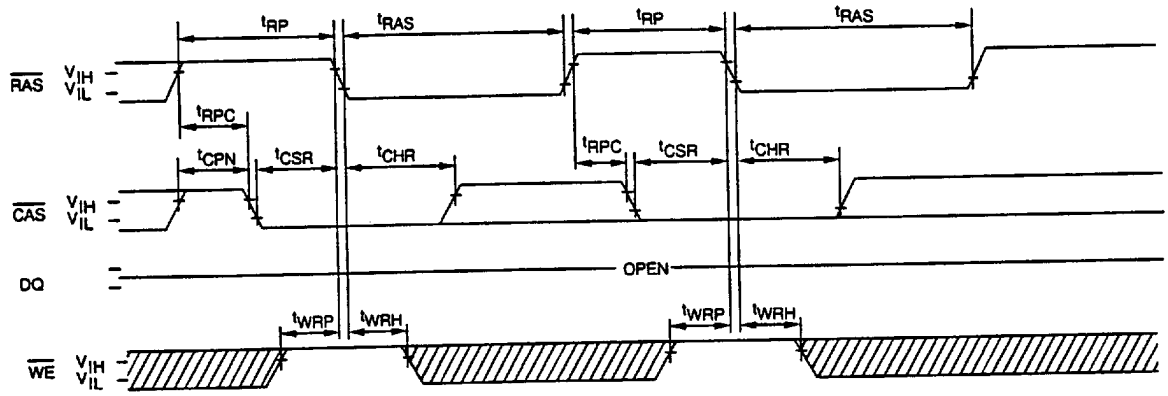



## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

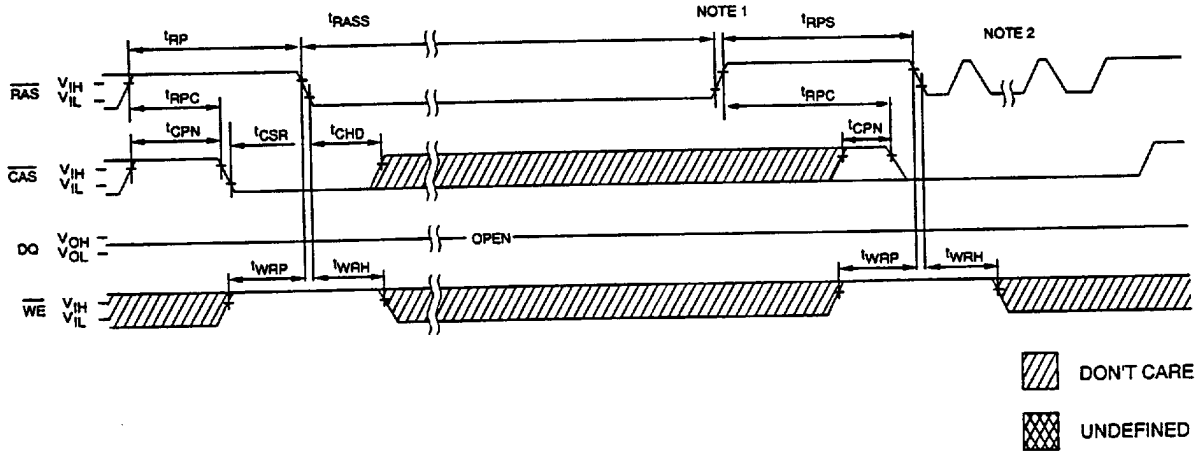



**NOTE:** 1. Do not drive data prior to tristate: $^tCPP$(MIN) or $^tCP$(whichever is greater) + $^tDS$(MIN) + any guardband between data-out and driving the bus with the new data-in.

## CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)

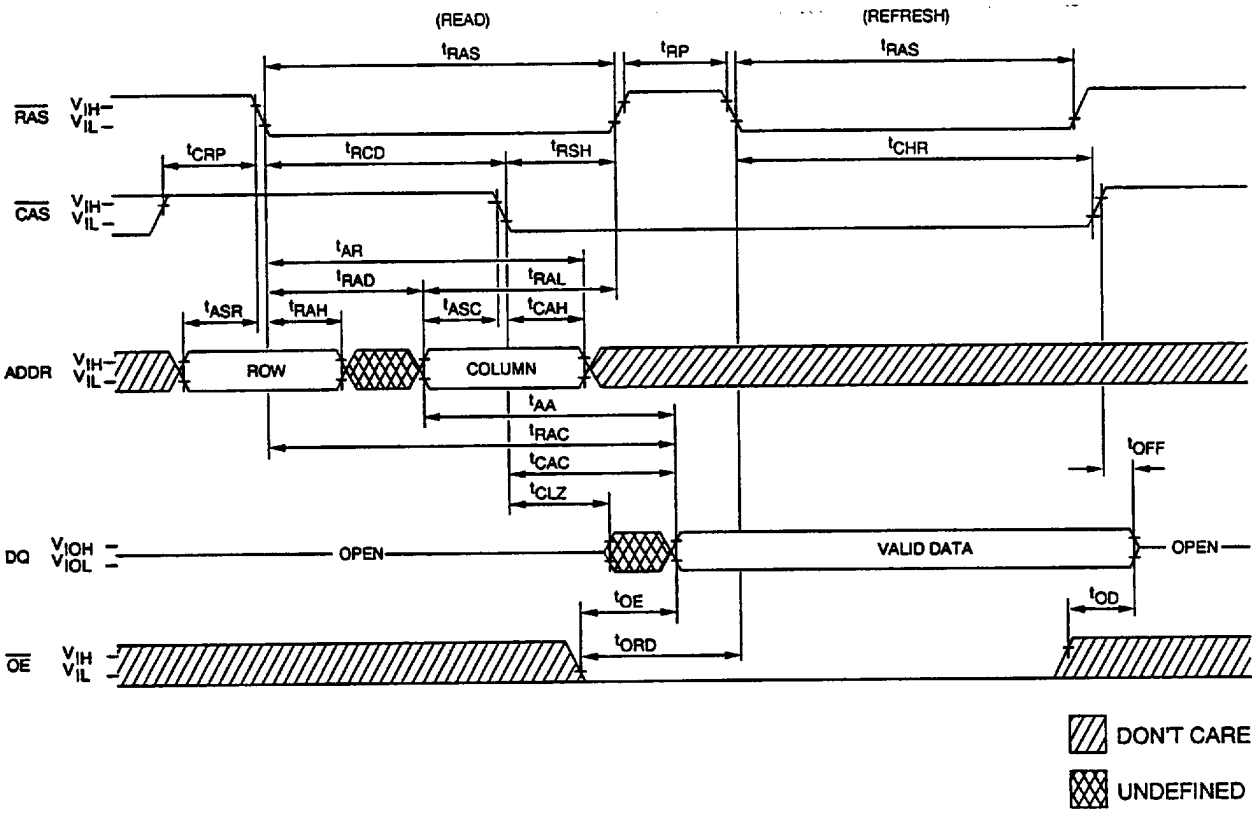



## SELF REFRESH CYCLE (MT4C4001J S only)
(A0-A9 and $\overline{OE}$ = DON'T CARE)




**NOTE:** 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

## HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



## 4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

## REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

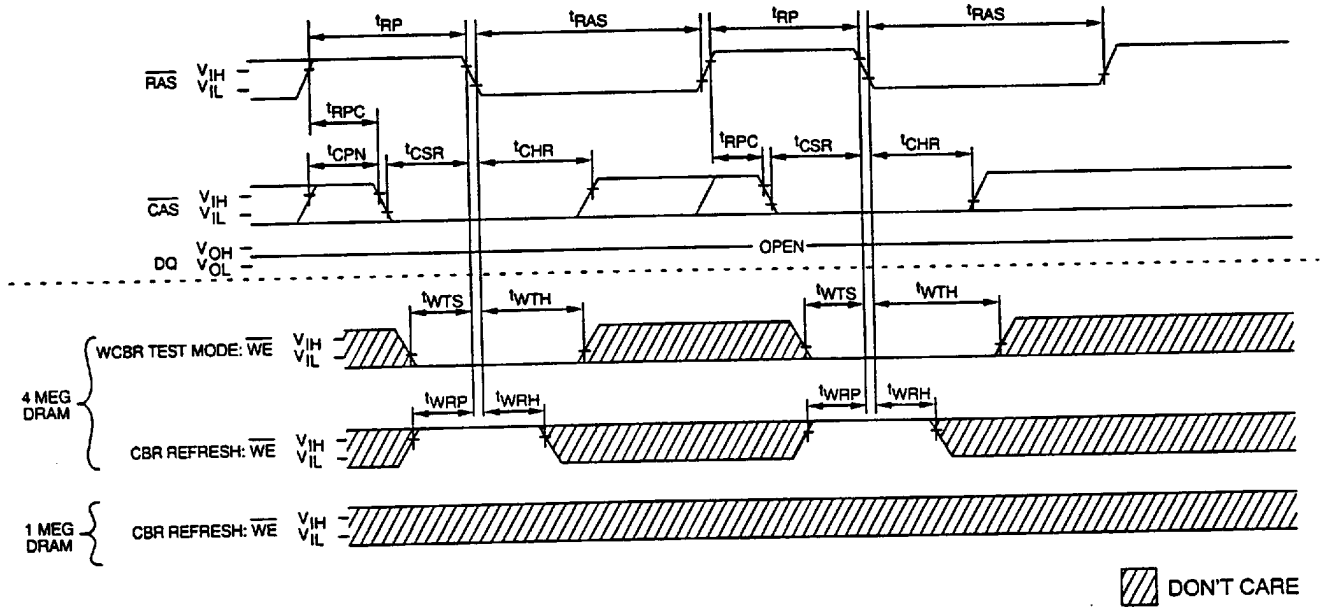
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

## POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$ ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$ ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

## SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$ ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).




**COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR**