MH88620IN

C.O. SLIC

Preliminary Information

ISSUE 3 April 1995

Features

- 600 ohm input impedance
- Externally selectable network balances
- Transformerless 2-4 wire conversion
- Programmable constant resistance feed
- Off-hook and dial pulse detection
- High immunity to externally induced longitudinal currents
- Auto ring trip
- On-hook transmission (ANI) capability
- Minimum protection circuitry required
- Compatible with requirements of CDOT DOC/ FCC, CSA/UL,CCITT
- Excellent power dissipation (SIL vertical mounting)

Applications

- On/Off-Premise PBX Line Cards
- Central Office Line Cards

Ordering Information

MH88620IN 40 Pin SIL Package

0°C to 70°C

Description

The Mitel MH88620IN SLIC provides all of the functions required to interface 2-wire off premise subscriber loops to a serial TDM, PCM, switching network of a modern PBX. The MH88620IN is manufactured using thick film hybrid technology which offers high voltage capability, reliability and high density resulting in significant printed circuit board area savings. A complete line card can be implemented with very few external components.

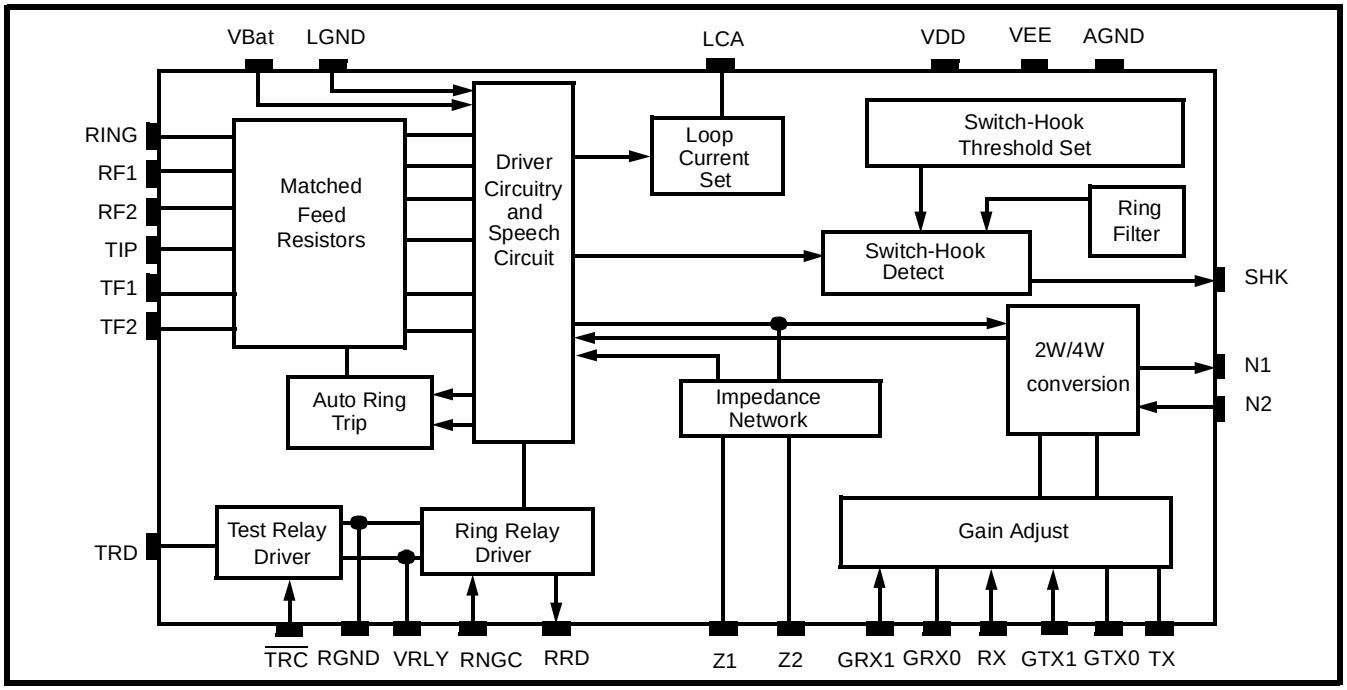


Figure 3 - Functional Block Diagram

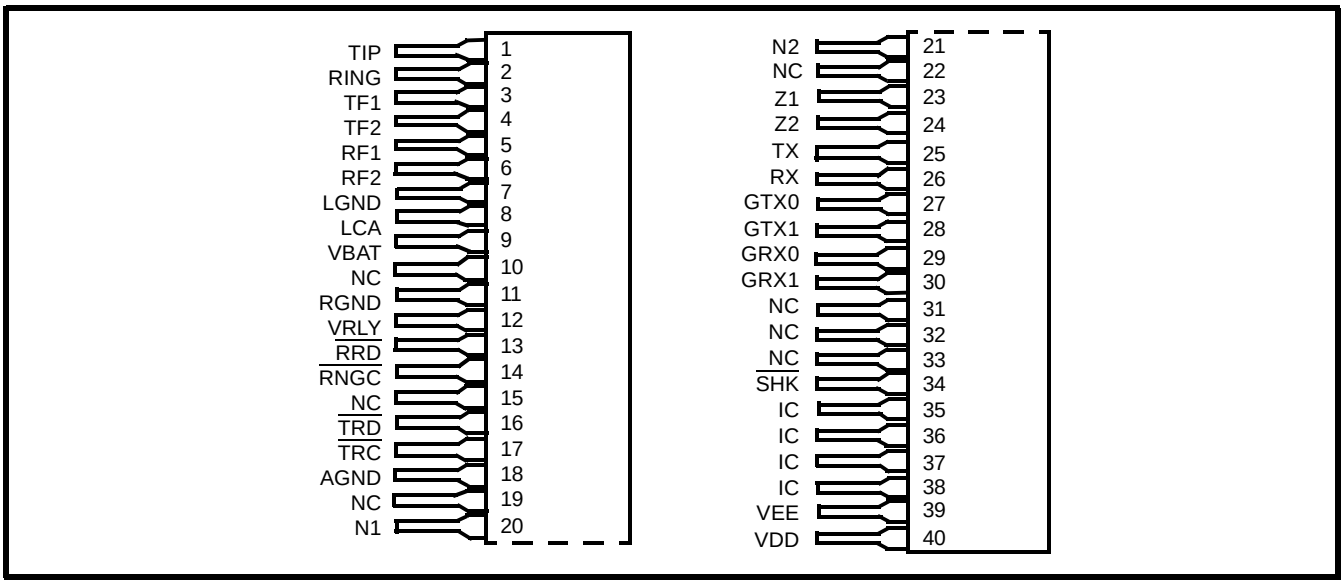


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TIP	**Tip Lead.** Connects to the TIP lead of the subscriber line
2	RING	**Ring Lead:** Connects to the Ring lead of the subscriber line.
3	TF1	**Tip Feed 1:** Access point for balanced ringing. Normally connects to TF2.
4	TF2	**Tip Feed 2:** Access point for balanced ringing. Normally connects to TF1.
5	RF1	**Ring Feed 1:** Access point for balanced ringing. Normally connects to RF2.
6	RF2	**Ring Feed 2:** Access point for balanced ringing. Normally connects to RF1.
7	LGND	**Battery Ground.** V_{BAT} return path. Connected to system's energy dumping ground.
8	LCA	**Current Limit Set (Input):** The current limit is set by connecting an external resistor as shown in Table 5. For 70mA default current, this pin is tied to -5V.
9	V_{Bat}	**Battery Voltage:** Typically -48V dc is applied to this pin.
10	RS1	**Ring Sense Resistor Connection 1.** See Figure 7a.
11	RGND	**Ring Driver Ground Connection.**
12	VRLY	**Relay Supply Voltage Connection**
13	$\overline{\text{RRD}}$	**Ring Relay Drive (Output).** Connects to ring relay coil
14	$\overline{\text{RNGC}}$	**Ring Relay Control (Input)**
15	RS2	**Ring Sense Resistor Connection 2.** See Figure 7a
16	TRD	**Test Relay Drive (Output):** Connects to test relay coil.
17	$\overline{\text{TRC}}$	**Test Relay Control (Input).**
18	AGND	**Analog Ground:** V_{DD} and $V_{EE.}$ return path
19	NC	**No Connection:** Reserved.
20	N1	**Network Balance Node 1.** An external network balance impedance can be connected between N1 and AGND. See Fig 4. for complex impedances. N2 no connection.
21	N2	**Network Balance Node 2.** See Fig 4. N2 connects to GND for 600Ω balance. N1 no connection.

Pin Description (Continued)

Pin #	Name	Description
22	NC	**No Connection.** Reserved
23	Z1	**Line impedance Node 1.** Normally connects to Z2. See Fig. 3.
24	Z2	**Line impedance Node 2.** Normally connects to Z1. See Fig 3.
25	TX	**Transmit (Output).** 4-wire (AGND) referenced audio output.
26	RX	**Receive (Input).** 4-wire (AGND) referenced audio input.
27	GTX0	**Transmit Gain Node 0.** Connects to GTX1 for 0dB transmit gain.
28	GTX1	**Transmit Gain Node 1.** Connects to a resistor to AGND for transmit gain adjustment.
29	GRX0	**Receive Gain Node 0.** Connects to GRX1 for 0dB gain
30	GRX1	**Receive Gain Node 1.** Connect to a resistor to AGND for receive gain adjustment
31	NC	**No Connection.** Reserved
32	NC	**No Connection.** Reserved.
33	NC	**No Connection.** Reserved.
34	$\overline{\text{SHK}}$	**Off-Hook Indication (Output).** A logic low output indicates when the subscriber equipment has gone Off-Hook.
35.38	IC	**Internal Connection.**
39	VEE	**Negative Supply Voltage.** -5V dc.
40	VDD	**Positive Supply voltage.** +5V dc

Absolute Maximum Ratings * All voltages are with respect to GNDA unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltages	LGND -V_{Bat} V_{DD} -GND GND - V_{EE}		65 6 6	V V V
2	Storage Temperature	T_S	-40	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions† - Voltages are with respect to GNDA unless otherwise stated.

	Characteristics	Sym	Min	Typ*	Max	Units	Comments
1	Operating Temperature	T_{OP}	0		70	°C	
2	Supply Voltages	V_{Bat*} V_{DD} V_{EE}	-44 4.75 -4.75	-48 +5.0 -5.0	-60 5.25 -5.25	V V V	

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
† Voltages specified are with respect to LGND.

DC Electrical Characteristics*

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Comments
1		Operating Loop Current	I_{Loop}			70	mA	R_{Loop} = 0Ω, LCA = -5V
				17			mA	1500Ω
				16			mA	2000Ω V_{Bat} = -48V
		Variation in Loop current from nominal	I_{Loop}		±2		mA	
2		Operating Current						
			I_{Bat}		2		mA	R_{Loop} = Open (On-hook)
			I_{DD}		15		mA	On-Hook or Off-Hook
			I_{EE}		15		mA	On-Hook or Off-Hook
		Power Dissipation	PDo		2		W	Active
			PD1		250		mW	Stand-by/Idle
3	$\overline{SHK}$	Low Level Output Voltage	V_{OL}			0.5	V	I_{OL} = 400µA
		High Level Output Voltage	V_{OH}	3.7			V	I_{OH} = 40µA
4	$\overline{RNGC}$ $\overline{TRC}$	Low Level Input Voltage	V_{IL}			0.8	V	
		High Level Input Voltage	V_{IH}	2.4			V	
5		Low Level Input Current	I_{IH}			20	µA	V_{IH} = 5.0V
		High Level Input Current	I_{IL}			20	µA	V_{IL} = 0.0V

* DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

AC Electrical Characteristics*

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Comments
1	Analog Tx Gain (T-R to TX)			0		dB	Externally adjustable
2	Analog Rx Gain (RX to T-R)			0		dB	Externally adjustable
3	Ringing Capability		25			V_{RMS}	R_{Loop} = 1400Ω Term. 6.8µF +200Ω
4	On-hook Transmission Signal input level Gain		 4		 2.0 8	 V_{RMS} dB	 V_{Bat} = -48V T-R load = 10Ωk min.
5	$\overline{SHK}$ Rise Time Fall time	t_R t_F		1 1		msec msec	Dial Pulse Detection
6	2 Wire Termination Impedance			600		Ω	Adjustable
7	Off-Hook Detect Threshold			10		mA	
8	2-Wire Return Loss 600Ω at T-R		20 26 20			dB dB dB	300-500Hz 500-2500Hz 2500-3400Hz
9	Longitudinal Balance Longitudinal to Metallic		 58 55 53			 dB dB dB	 2000Hz, 1000Hz 2000Hz, 3000Hz 3400Hz
10	Longitudinal Current Capability				40	mA	20mA per lead
11	Idle Channel Noise Rx to T-R T-R to Tx	 N_{CR} N_{CX}		 8 12		 dBrnC dBrnC	
12	Transhybrid Loss Tx gain 0dB Rx gain 0dB	THL	 16 20 16			 dB dB dB	 300-500Hz 500-2500Hz 2500-3400Hz
13	Analog Signal Overload Level at TIP and RING				4	dBm	T-R = 900Ω V_{BAT} = -48V
14	Ringing Signal Voltage		70	80	90	V_{RMS}	
15	Ringing Frequency		20	25	30	Hz	
16	Ring Trip Delay			100		ms	
17	Absolute Gain variation		-25	0	+.25	dB	0dBm at T-R, 1kHz
18	Relative Gain, reference to 1kHz		-2	0	+.2	dB	300-3400Hz
19	Power Supply Rejection Ratio V_{BAT} V_{DD} V_{EE}	PSRR	 24 24 24	 30 30 30		dB	1kHz, 100mVpp

* AC Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25C with nominal ± 5V supplies and are for design aid only.

Note: Test Conditions use a transmit and receive gain set to 0dB default and a Z_{in} value of 600Ω unless otherwise stated.

"Ref" indicates reference impedance which is equivalent to the termination impedance.

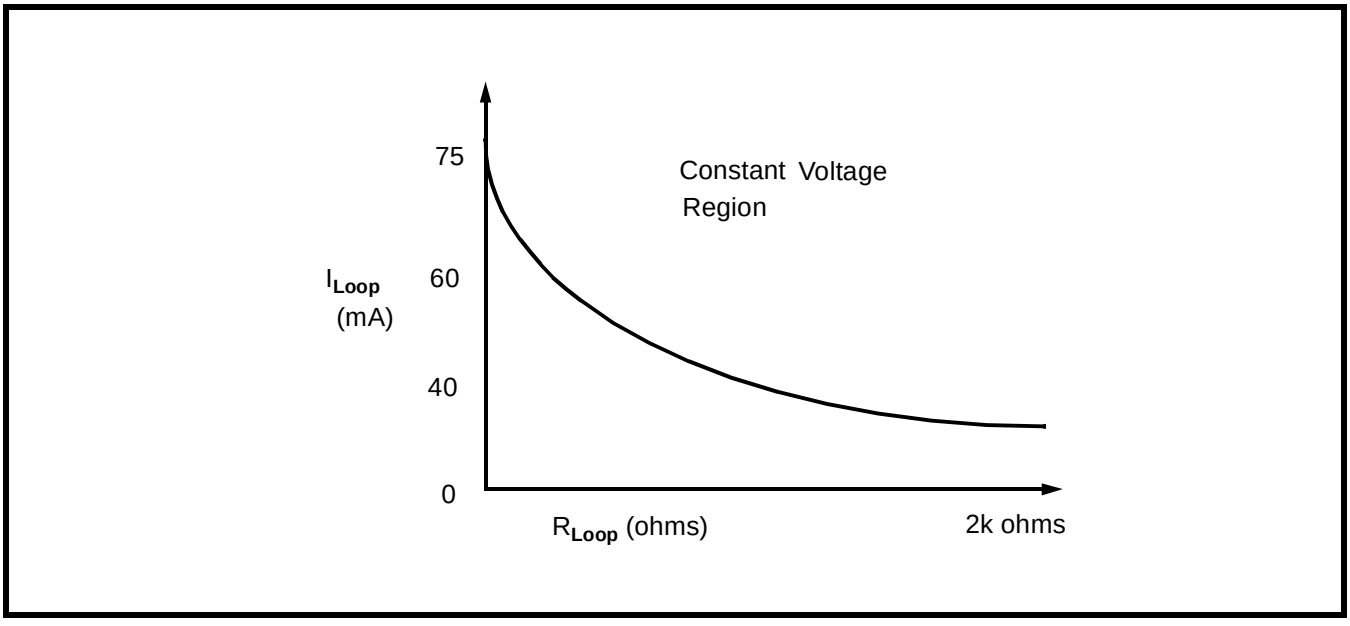
"Net" indicates network balance impedance.

Transmit Gain (dB) 2-Wire to Tx 20log (Tx/2-Wire)	RTX Resistor (1%) Value (Ω)	Notes
+6.0	No Resistor	
+4.0	38.3k	Results in 0dB overall gain when used with Mitel A-law codec (i.e. MT8965)
+3.7	32.4k	
0.0	Connect GTX0 to GTX1	
-3.0	5.49k	
-6.0	3.32k	
-12.0	1.43k	

Note 1: Overall gain refers to the receive path of PCM to 2-Wire.
Note 2: See Figure 2 for Application Circuit.

Receive Gain (dB) Rx to 2-Wire 20log (2-Wire/ Rx)	RRX Resistor (1%) Value (Ω)	Notes
+6.0	No Resistor	
0.0	Connect GRX0 to GRX1	
-3.0	5.49k	
-3.7	4.87k	
-4.0	4.64k	Results in 0dB overall gain when used with Mitel A-law codec (i.e. MT8965)
-6.0	3.32k	
-12.0	1.43k	

Note 1: Overall gain refers to the receive path of PCM to 2-Wire.
Note 2: See Figure 2 for Application Circuit.



Graph 1 - I_{Loop}/R_{Loop} Characteristics

Functional Description

The SLIC uses a Transformerless electronic 2-4 wire converter which can be connected to a Codec to interface the 2 wire subscriber loops to a time division multiplexed (TDM) pulse code modulated (PCM) digital switching network. For analog applications, the TXRX of the 2 wire converter can be connected directly to an analog crosspoint switch, such as the MT8816. Powering of the line is provided through precision battery feed resistors. The MH88620IN also contains control, signalling and status circuitry which combines to provides a complete functional solution, simplifying the manufacture of line cards. This circuitry is illustrated in the functional block diagram in Fig 1. The MH88620IN is designed to be pin compatible with Mitel's MH88632, MH88625, MH88620, and MH88628. This allows a common PCB design with common gain, input impedance and network balance.

Approvals

FCC part 68, CCITT, DOS CS-03, UL 1459, CAN/ CSA-22.2 N0. 225-M90 and ANSI/EIA/TIA-464-A are system level safety standards and performance requirements. As a component of a system, the MH88620IN is designed to comply with the applicable requirements of these specifications.

Battery Feed

The loop current for the subscriber equipment is sourced through a pair of matched 200 ohm resistors connected to the TIP and RING. The two wire loop is biased such that the Ring lead is 2V above VBAT (typically -46V) and the Tip lead is 2V below LGND (typically -2V) during constant voltage mode.

The SLIC is designed for a nominal battery voltage of -48Vdc and can provide the maximum loop current of 75mA under this condition.

The interface circuit is designed to be operated down to a maximum of 16mA dc, with a battery voltage of -44V. The Tip and Ring output drivers can operate within 2V of V_{Bat} and LGND rails.

Loop Current Setting

The MH88620IN SLIC is a constant resistance with constant voltage fallback design. This design feature provides for long loop capability regardless of the current setting. Refer to graph 1.

The LCA (Loop Current Adjust) pin is an input to an internal resistor driver network which generates a bias voltage. The loop current is proportional to this voltage. The loop current can be set between 30 and 75 mA by various connections to the LCA pin as illustrated in Table 5 and Figure 5. The loop current during a fault condition will be limited to the constant loop current programmed. Primary over current protection is inherent in the current limiting feature of the 200 ohm battery feed resistor. Refer to Graph 1.

Receive and Transmit Audio Path

The audio signal of the 2-wire is sensed differentially across the 200 ohm feed resistor and is passed on to a second differential amplifier stage in the 2W/4W conversion block. This block sets the transmit gain on the 4-wire side and cancels signals originating from the receive input.

Programmable Transmit and Receive Gain

Transmit Gain (Tip-Ring to Tx) and Receive Gain (Rx to Tip-Ring) are programmed by connecting external resistors (RRX and RTX) from GRX1 to AGND and from GTX1 to AGND as indicated in Figure 2 and Table 1 and 2. The programmable gain range is from -12dB to +6dB; this wide range will accommodate any loss plan. Alternatively, the default Receive Gain of 0dB and Transmit Gain of 0dB can be obtained by connecting GRX0 and GRX1 and GTX0 to GTX1. In addition, a Receive Gain of +6dB and Transmit Gain of +6dB can be obtained by not connecting resistors RRX and RTX. For correct gain programming. the MH88620IN's Tip-Ring impedance (Z_{in}) must match the line termination impedance.

For optimum performance, resistors RRX should be physically located as close as possible to the GRX1 input pin, and resistor RTX should be physically located as close as possible to the GTX1 input pin.

Two Wire Port Termination Impedance

The AC termination of 600 ohms, of the 2W port is set using active feedback paths to give the desired relationship between the line voltage and the line current. The loop current is sensed differentially across the two feed resistors and converted to a single ended signal. This signal is fed back to the

Tip/Ring driver circuitry such that impedance in the feedback path gets reflected to the two wire port.

The MH88620IN's Tip-ring impedance (Z_{in}) is designed to be 600Ω, when used with 25Ω PTC's as protection circuitry. For this requirement, Z1 and Z2 should be connected together on the PCB. To accommodate the use of lower value PTC's a series resistance can be connected between Z1 and Z2. For example, if two 8Ω PTCs are used, connect 340Ω between Z1 and Z2.

The design uses a 0.1 times impedance amplifier so the 340Ω actually adds 34Ω of additional impedance to the 550Ω (16 + 34 +550 = 600). For complex impedance setting, a capacitor and/or resistor can be connected between Z1 and Z2. For example, if Return Loss is to be maximized for a Z_{in} of 600 +2.2µF, a 0.22µF cap can be connected between Z1 and Z2.

Network Balance

Transhybrid loss is maximised when the line termination impedance and SLIC network balance are matched. The MH88620IN's network balance impedance can be set to Zin, or to a user selectable value. Thus, the network balance impedance can be set to any Indian or other international requirement. An external Network Balance impedance is selected which 0.1 times the impedance between N1 and AGND. N2 to GND balances to 600 ohms.

Off-Hook and Dial Pulse Detection

The $\overline{SHK}$ pin goes low when the DC-loop current exceeds a specified level. The threshold level is internally set by the bias voltage of the switch-hook detect circuitry. Dial pulses can be detected by monitoring the interruption rate at the $\overline{SHK}$ pin. These dial pulses would be debounced by the system software.

Ring Trip Detection

The interface permits detection of an Off-Hook condition during ringing. If the subscriber set goes Off-Hook when the ringing signal has been applied, the DC loop current flow will be detected within approximately 100msecs and the $\overline{SHK}$ output will go low. The Ring relay is automatically disabled by the internal hardware.

Longitudinal Balance

The longitudinal balance specifies the degree of common mode rejection in the 2 to 4 wire direction. Precision laser trimming of internal resistors in the hybrid ensures good overall longitudinal balance.

The interface circuitry can operate in the presence of induced longitudinal currents of up to 40 mA RMS at 60 Hz.

DTMF

The DTMF tones are transmitted and received at the 4-wire port.

High voltage Capability

Inherent in the thick-film process is the ability of the substrate to handle high voltage. The standard Mitel thick-film process provides dielectric strengths of greater than 1000 VAC or 1500 VDC. The thick-film process allows easy integration of surface mount components such as the high voltage bipolar power transistor line drivers. This allows for simpler, less elaborate and less expensive protection circuitry required to handle high voltage transients and fault conditions caused by lightning, induced voltages and power line crossings.

On-Hook Transmission

The MH88620IN provides for on-hook transmission which supports features such as Automatic Number Identification (ANI). The ANI information is a FSK or DTMF signal originating from and sent by the C.O. during the off period of the ringing voltage being sent to the subscriber's set. The subscriber's set decodes the identification signal and displays the calling party's number.

Applications

As shown in the application diagram, Figure 7a, the ringing voltage, typically 80 V_{RMS} 25Hz biased at -48 VDC, is applied to the subscriber line through an external relay, K1, Enabling of the relay is performed by applying a logic high level to the relay driver control input, RRC.

Figure 7b, shows how balanced ringing can be accommodated if required.

Protection Circuitry

Primary protection, from lightning strikes and AC line faults, is normally located in the MDF (main distribution feeder) which is located external to the PABX or CO switching system. The primary protection circuitry is normally housed in a 5-pin connector and consists of either carbon blocks, with spark gaps (older technology), gas discharge tubes or high current semiconductor suppressors and series heat coils. The 5-pin module usually limits the high voltage to approximately 300 to 500 volts before entering the switching system.

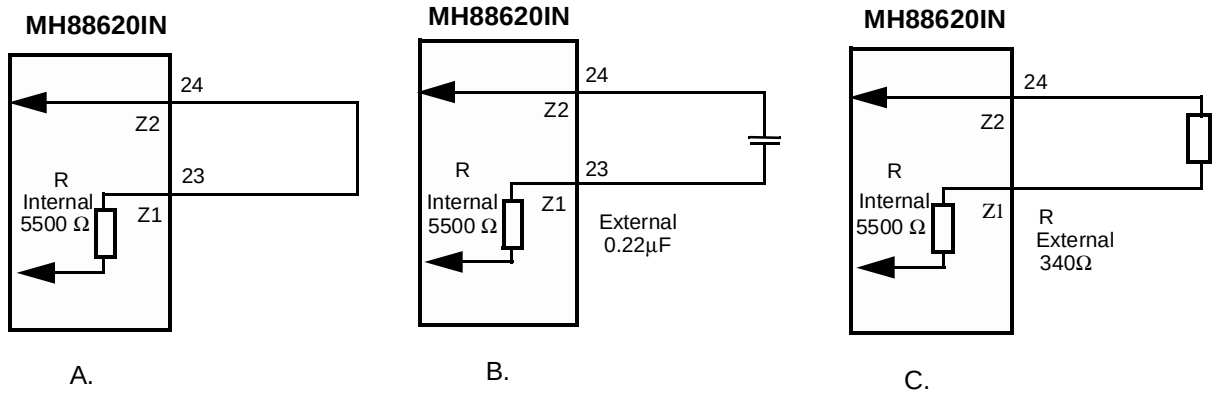
Secondary protection, in the switching system, is required to further limit these high voltages/currents.

Secondary protection is normally implemented on each line card and is designed to protect the SLICs from permanent damage. The basic secondary high voltage protection circuitry for the MH88620IN, as illustrated in Figure 7, consists of PTC1, PTC2 and clamping diodes D1 to D4. During a fault condition, the diodes clamp the overvolt Ground and $-V_{Bat}$. PTC1 and PTC2 current limit as their resistance increases with power dissipation caused by the over-a voltage/over-current condition. The ground that D1 and D3 are connected to, must be an EDG (energy dumping ground) which is connected to the chassis or system ground. This is a seperate conductor from LPGND or AGND on the line care PCB. D2 and D4 conduct the energy into a $-V_{Bat}$ supply which is a seperate conductor from the $-V_{Bat}$ feed supply to the SLICs. A power MOSFET circuit as shown in Figure 8, can be used to divert the energy normally dumped into $-V_{Bat}$, the EDG conductor. Usually one MOSFET circuit can be used for 16 SLICs or per line card.

Depending on the additional level of protection required, PRO1 and/or PRO2 protectors may be used. These are used to protect the SLICs Ring sense resistor and/or Ring generator from being damaged if a fault condition occurs during the application of Ringing to the line. PRO2 can be implemented using two back to back zener diodes, or an equivalent transient suppressor. The clamping voltage should be >16 Vdc and <26Vdc. PRO2 may not be required depending on the value and power dissipation of PRO1.

Loop Length

The MH88620IN can accommodate loop lengths of up to 2000 ohms minimum (including the subscriber equipment). This corresponds to approximately 8km using #26 AWG twisted pair or 15km using #24 AWG twisted pair.



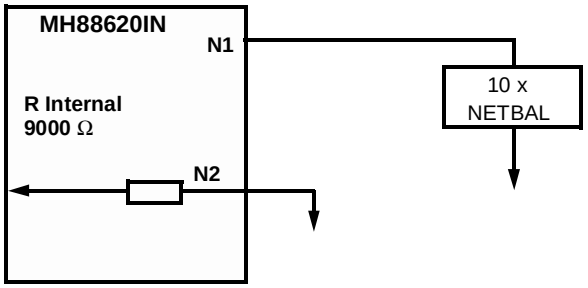
Notes

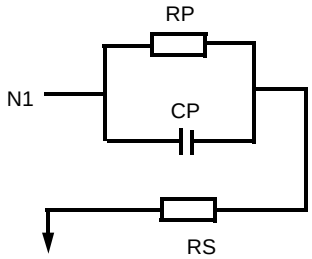
a) to accommodate the use of 2 x 25Ω PTCs, connect Z1 and Z2 together, Z_{in} = 600Ω.

b) to accommodate the use of 2 x 8Ω PTCs, connect 340Ω between Z1 and Z2 = 600Ω.

c) to accommodate the use of 2 x 25Ω PTCs, connect 0.22µF between Z1 and Z2 = 6.0Ω + 2.2µF.

Figure 3 - Input Impedance (Z_{in}) setting





$$ZNETBAL = 0.1 \times \left[RS + \frac{1}{1/RP + (S \times CP)} \right]$$

where S = j x w
and w = 2 x π x f

Notes:

1) The $10xZ_{in}$ network must be set to 10 x the desired input Z_{in} (impedance).
2) The 10 x NETBAL network must be set to10x the desired network balance.
3) Make connection between N1 and component as short as possible.

Example:

If RS =0Ω, RP = 800Ω, CP=.5nF
Then the network balance is 800Ω in parallel with 50nF.

Figure 4 - External Network Balance Setting

Loop Current	LCA Pin Connection	Reference Fig#
20	Connect 10kΩ from LCA to +5V.	5a
25	Connect 16kΩ from LCA to +5V.	5a
30	Connect 36kΩ from LCA to +5V.	5a
35	Leave LCA open circuit.	5c
40	Connect 24kΩ from LCA to -5V.	5b
45	Connect 10kΩ from LCA to -5V.	5b
50	Connect 5.6kΩ from LCA to -5V.	5b
55	Connect 2.4kΩ from LCA to -5V.	5b
60	Connect 1.3kΩ from LCA to -5V.	5b
65	Connect 680kΩ from LCA to -5V.	5b
70	Connect from LCA to -5V.	5d

Table 5 - Loop Current Setting

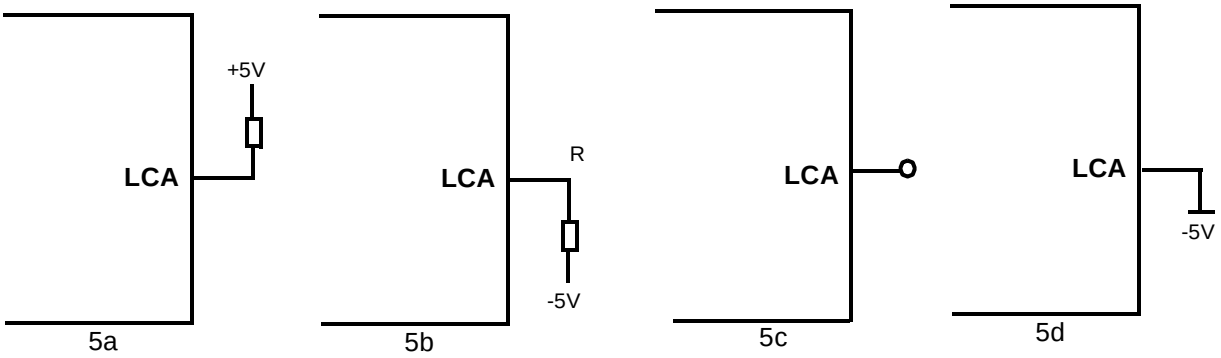


Figure 5 - Loop Current Setting

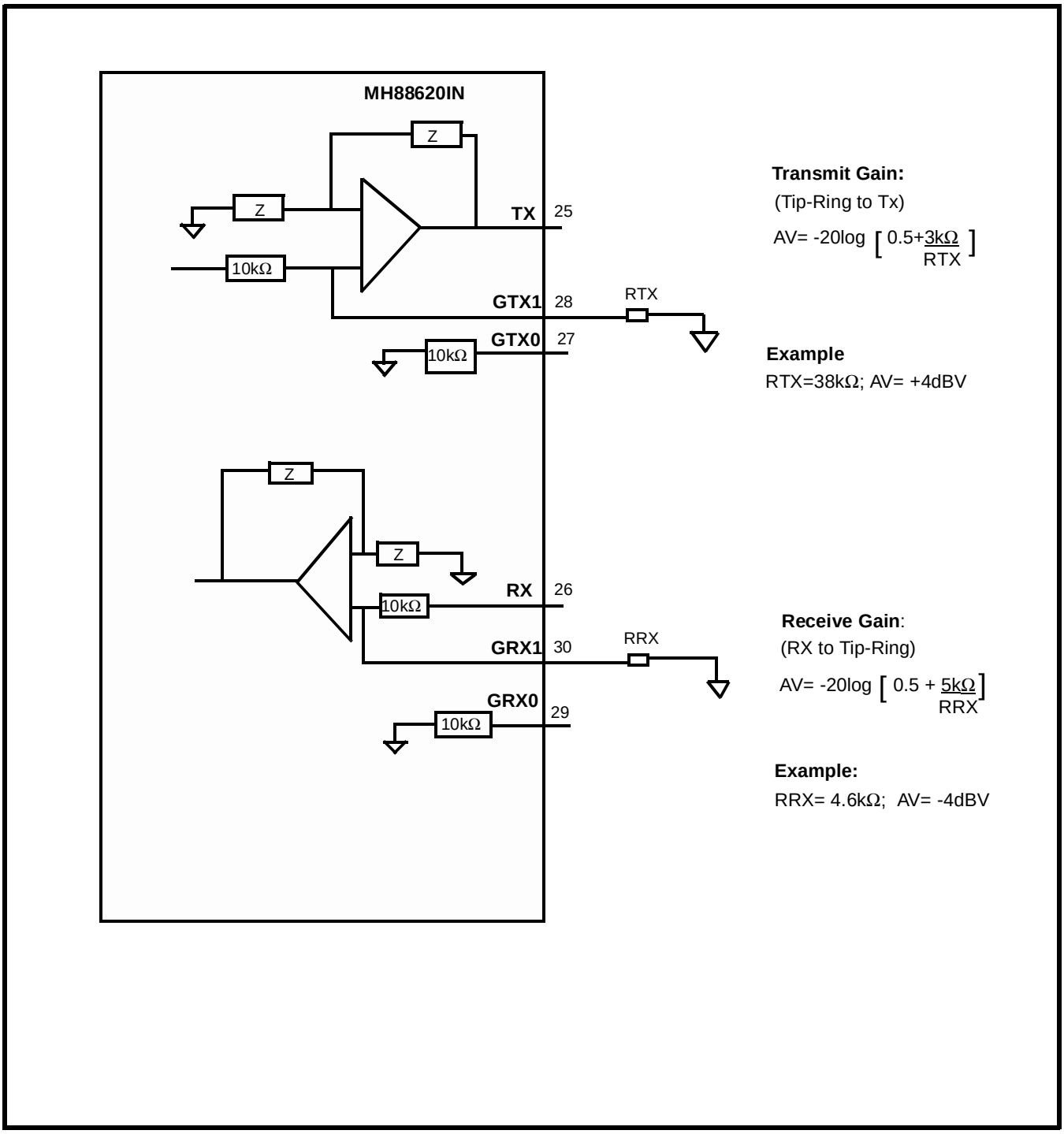


Figure 6 - Gain Programming with External Components

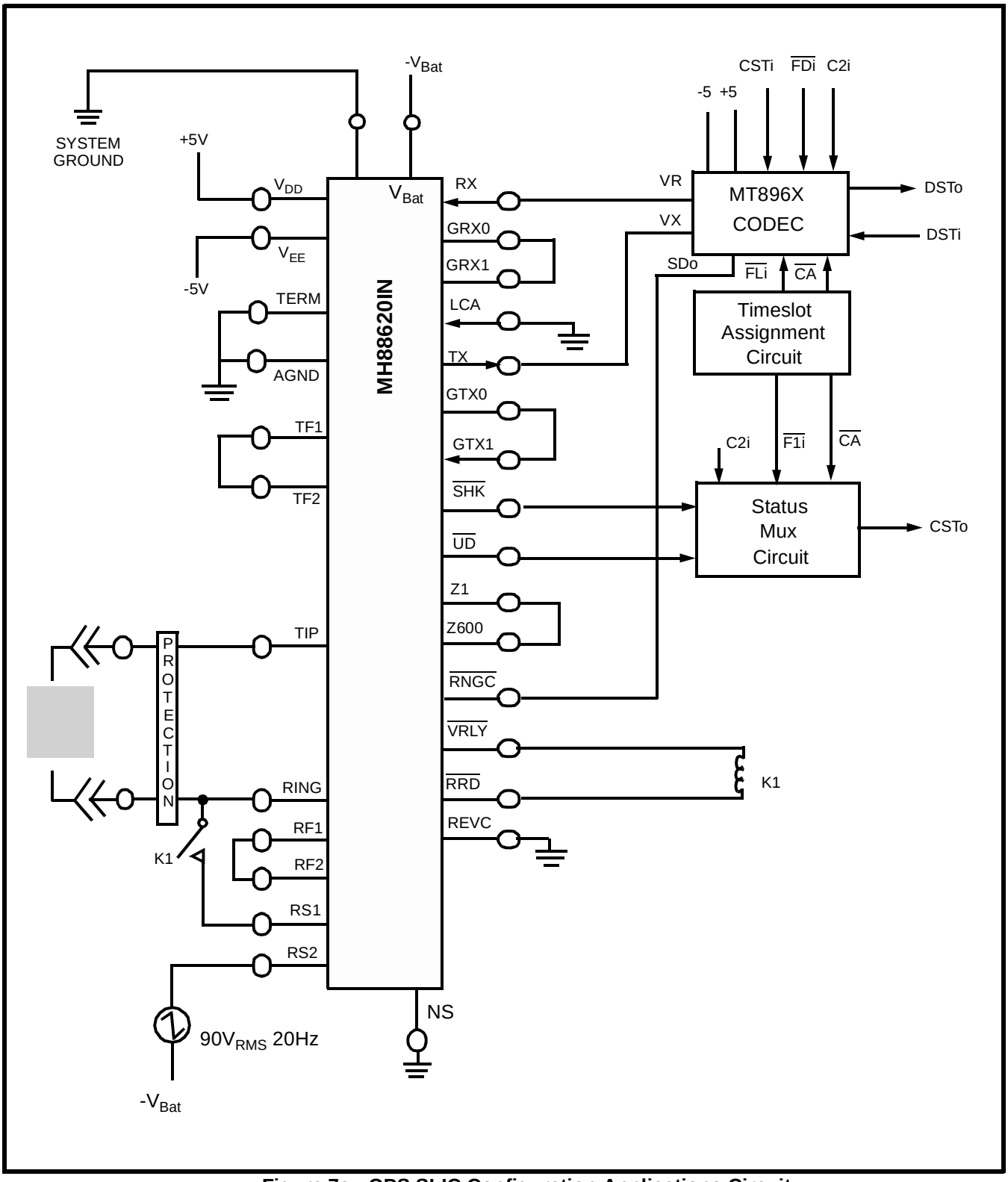


Figure 7a - OPS SLIC Configuration Applications Circuit

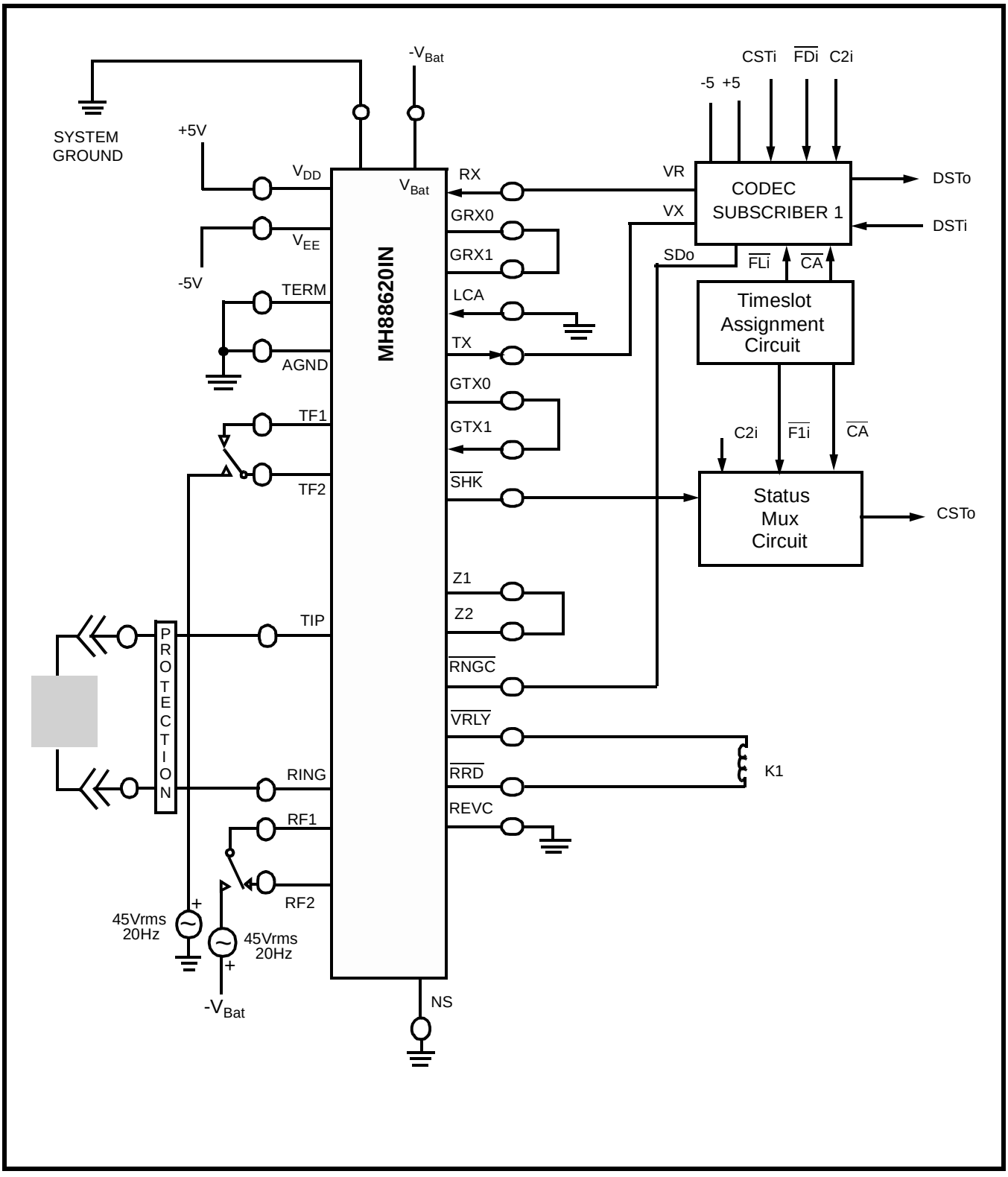
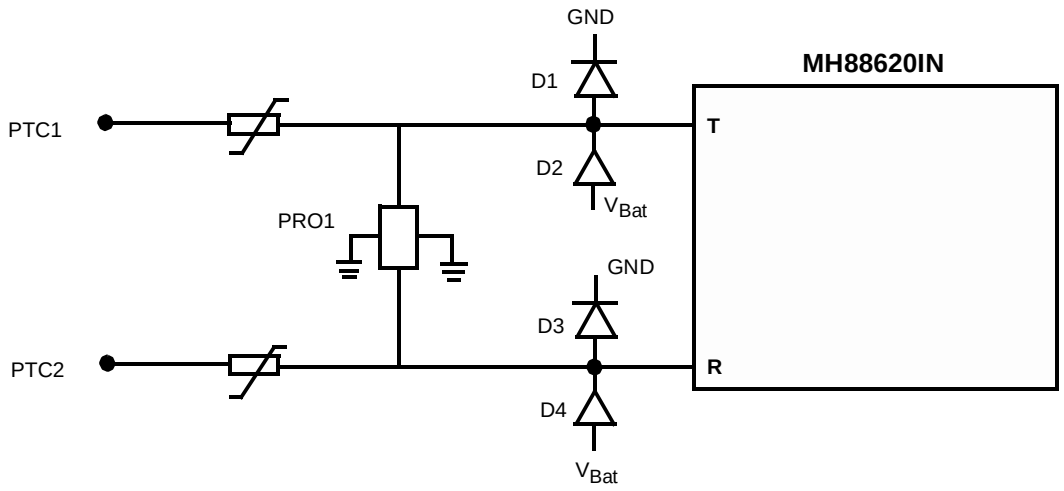


Figure 7b - OPS SLIC Configuration Applications Circuit - Balanced Ringing

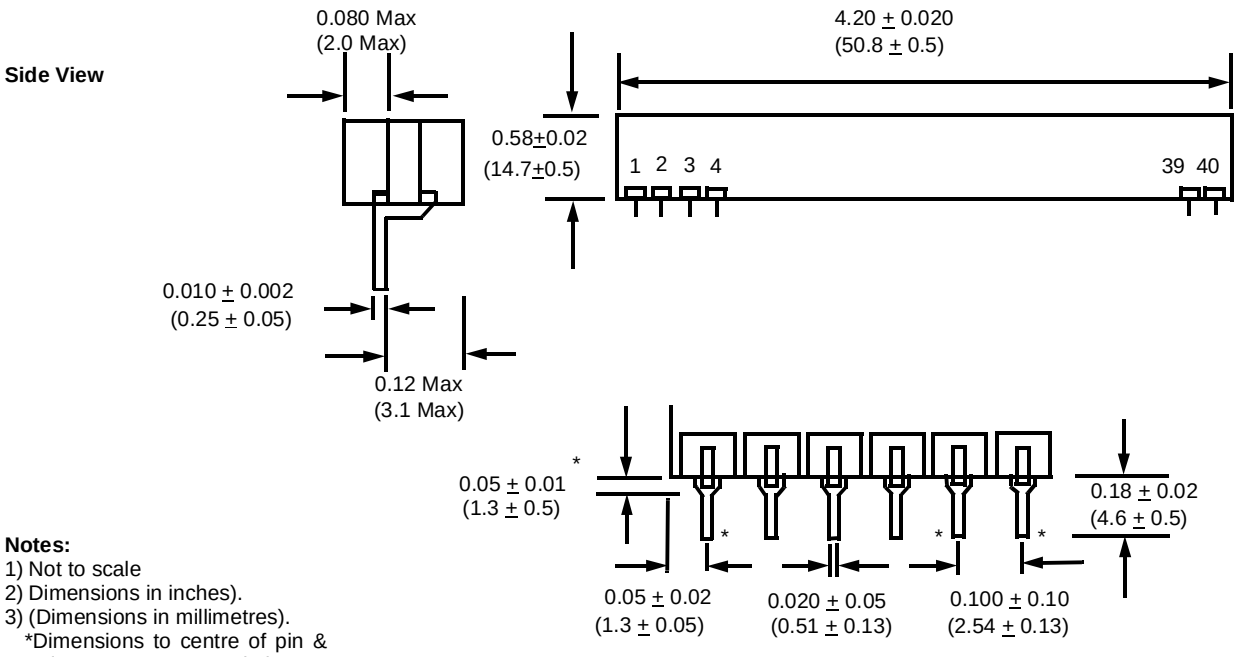


Suggested Components

PRO1 Solid State Transient Suppressor, e.g., TISP2300L, P2703AB, MOV's or diode clamps D1-D4 to V_{Bat} and LPGND

PTC1, PTC2 Typical 25 Ω

Figure 8 - Suggested Protection Circuit



Notes:
1) Not to scale
2) Dimensions in inches).
3) (Dimensions in millimetres).
*Dimensions to centre of pin & tolerance non accumulative.

Figure 9 - Mechanical Data