SP5848

2.2/1.3GHz 3-Wire Bus Dual Low Phase Noise PLL

Preliminary Information

DS5076 Issue 1.6 October 1999

Features

- Dual independent PLL frequency synthesisers in a single package, optimised for double conversion cable tuners, offering improved application
- 2.2GHz up-synthesiser optimised for low phase noise up to comparison frequencies of 4MHz
- 1.3GHz down-synthesiser optimised for low phase noise AND small step size
- Common reference oscillator and divider with independently selectable ratios for each synthesiser
- 10:1 programmable charge pump current ratio in up synthesiser
- 3-Wire bus programmable, each synthesiser indepently addressable
- Low power consumption, typ 100mW at 5V
- ESD protection, (Normal ESD handling procedures should be observed)

Applications

- TV, VCR, and cable tuning systems

Ordering Information

SP5848/KG/QP1S
SP5848/KG/QP1T

Description

The SP5848 is a dual PLL frequency synthesizer controlled by a 3-wire bus optimised for application in double conversion tuners.

Each synthesiser loop within the SP5848 is independently addressable and contains an RF programmable divider, phase/frequency detector and charge pump/loop amplifier section; a common reference frequency oscillator and divider chain is provided, whose ratios for each loop are independently programmable.

Both synthesisers are optimised for low phase noise performance and in addition synthesiser 2 is capable of operation with a low comparison frequency.

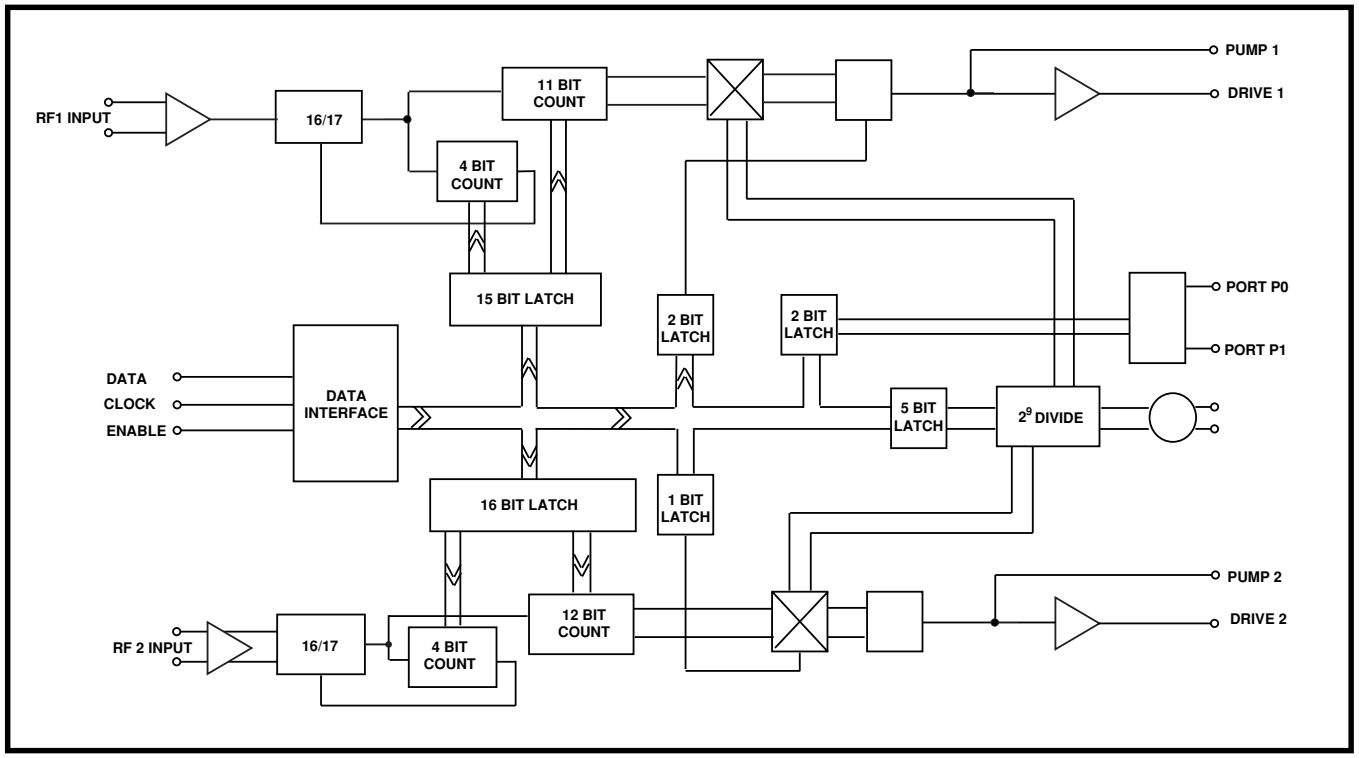


Figure 1 Block Diagram

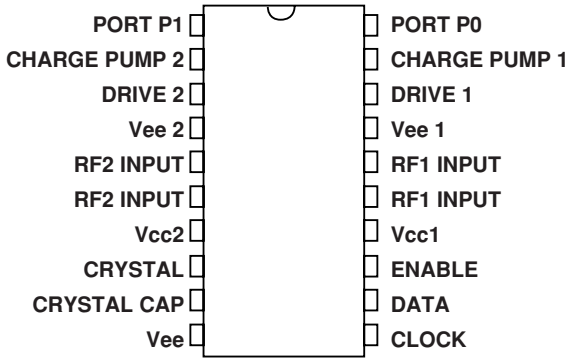


Figure 2 Pin Connections

Electrical Characteristics

T_{amb}= -40°C to +80°C, Vcc = 4.5 to 5.5 V, These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	7, 14	4.5		5.5	V	
Supply current			18	22	mA	
Synthesiser 1 (UP)						
RF1 input voltage	15,16	40		300	mV_{rms}	80 -2200MHz
RF1 input impedance	15,16					See Figure 4
RF1 division ratio		240		32767		
Reference division 1 ratio						See Table 1
Comparison frequency 1				4	MHz	
Equivalent phase noise at phase detector 1			-148		dBc/Hz	SSB, within loop bandwidth, all comparison frequencies
Charge pump 1 output current	19					See Table 3 Vpin 19=2V
Charge pump 1 output leakage	19		±3	±10	nA	Vpin19 = 2V
Charge pump 1 drive output current	18	0.5			mA	Vpin 18 = 0.7V

Electrical Characteristics (continued)

T_{amb}= -40°C to +80°C, Vcc = 4.5 to 5.5 V, These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Synthesiser 2 (DOWN)						
RF2 input voltage	5,6	30		300	mV_{rms}	80 -1300MHz
RF2 input impedance	5,6					See Figure 5
RF2 division ratio		240		65535		
Reference division 2 ratio						See Table 2
Comparison frequency 2		16.25		4000	KHz	Phase noise degrades above 250KHz
Equivalent phase noise at phase detector 2			-144		dBc/Hz	SSB, within loop bandwidth, all comparison frequencie up to 250KHz
Charge pump 2 output current	2					See Table 4 Vpin 2=2V
Charge pump 2 output leakage	2		±3	±10	nA	Vpin2 = 2V
Charge pump 2 drive output curent	3	0.5			mA	Vpin 3 = 0.7V
Data, clock and enable	12,11,13					
Input high voltage		3		Vcc	V	
Input low voltage		0		0.7	V	
Input current		-10		10	µA	All input conditions
hysterysis			0.8		Vpp	
Clock rate	11			500	KHz	
Bus timing -						
Data set up		300			ns	
Data hold		600			ns	
Enable setup		300			ns	
Enable hold		600			ns	
Clock to enable		300			ns	
Reference Oscillator						
Crystal frequency	8, 9	2		16	MHz	See Figure 6 for application
External reference input frequency	8	2		20	MHz	Sinewave coupled through 10nF blocking capacitor
External reference drive	8	0.2		0.5	Vpp	Sinewave coupled through 10nF blocking capacitor
Outputs ports P0 - P1	1, 20					See note 1
sink current		2			mA	Vport = 0.7V
leakage current				10	µA	Vport = Vcc

Note 1 Output ports high impedance on power up, with data, clock and enable at logic 0

Absolute maximum Ratings

All voltages referred to Vee at 0V

Characteristic	Value			Conditions
	Min	Max	Units	
Supply voltages	-0.3	7	V	
RF1 input voltage		2.5	Vp-p	Differential
RF2 input voltage		2.5	Vp-p	Differential
All I/O ports DC offset	-0.3	Vcc+0.3	V	
Storage temperature	-55	+125	°C	
Junction temperature		150	°C	
Package thermal resistance				
chip to ambient		100	°C/W	
chip to case		30	°C/W	
Power consumption with all Vcc =5.5V		121	mW	All ports off
ESD protection	2		kV	Mil std 883 latest revision methood 3015 class 1

Functional Description

The SP5848 contains two PLL frequency synthesiser loops, each independently programmable from a 3-wire bus. The device is optimised for application in double conversion tuners where synthesiser 1 would form part of the upconverter and synthesiser 2 part of the down converter. Both loops are optimised for application in low phase noise loops and furtherly synthesiser 2 offers low comparison frequencies. A block diagram is contained in Figure 1.

The device is programmed via a 3-wire bus where data is fed on serial data and clock lines and is gated by an enable line. Figure 3 indicates the format of the data. The sequence and timing of data load is described below in 'programming mode' description. Each synthesiser is independently addressable and is defined by the LSB bit within the data transmission.

A common reference frequency source and reference divider is used to derive the comparison frequency for both PLL loops. The reference division ratio is programmable via the data bus as defined in Tables1 and 2.

The charge pump current for each loop is also programmable via the data bus as defined in Tables 3 and 4

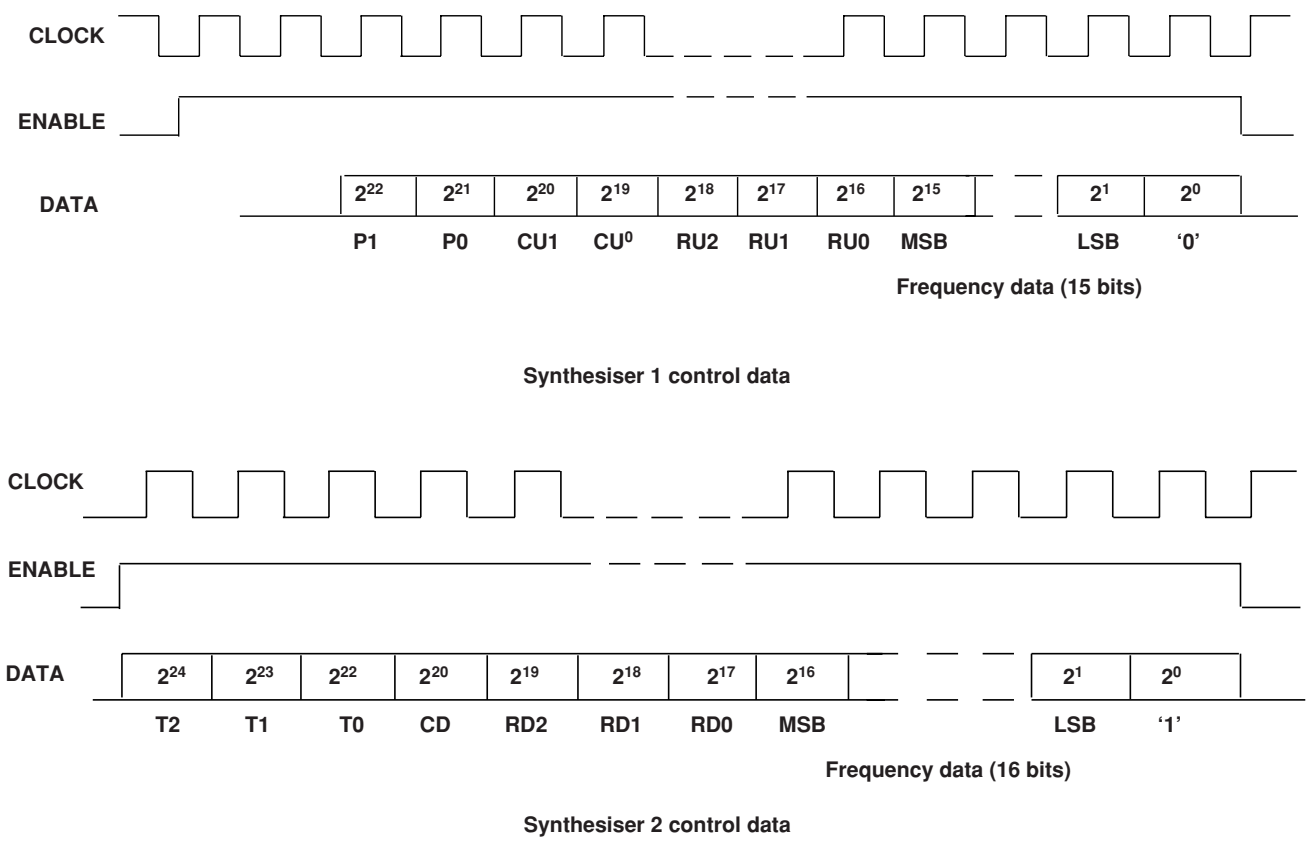
Two switching ports are provided to control switching functions within the tuner. These ports also access test signals within the PLL as defined in Figure 7. Ports power up in high impedance state.

Programming Mode

The SP5848 is designed to be programmed from a standard 3-wire bus consisting of clock, data and enable, where the serial clock and data lines can be shared with other devices and the enable line is a unique line for individual device selection. To simplify programming each synthesiser is independently addressed, with the required loop being selected by the LSB bit , which functions as the address, therefore to fully program the device two complete data transmissions must be sent.

The data format for each transmission is contained in Figure 3.

Test modes as described in Figure 7, can be invoked by setting bit T0 in synthesiser 2 data word to a '1' and sending control data for bits T1-T2. In normal operation where T0 is set to a '0' bits T1 and T2 do not need to be transmitted



CU0 - CU1	:	Synthesiser 1 charge pump
RU0 - RU2	:	Synthesiser 1 reference division ration
CD	:	Synthesiser 2 charge pump
RD0 - RD2	:	Synthesiser 2 reference division ratio
T0 - T2	:	Test modes
P0 - P1	:	Switching ports P0 - P1

Figure 3 Control data

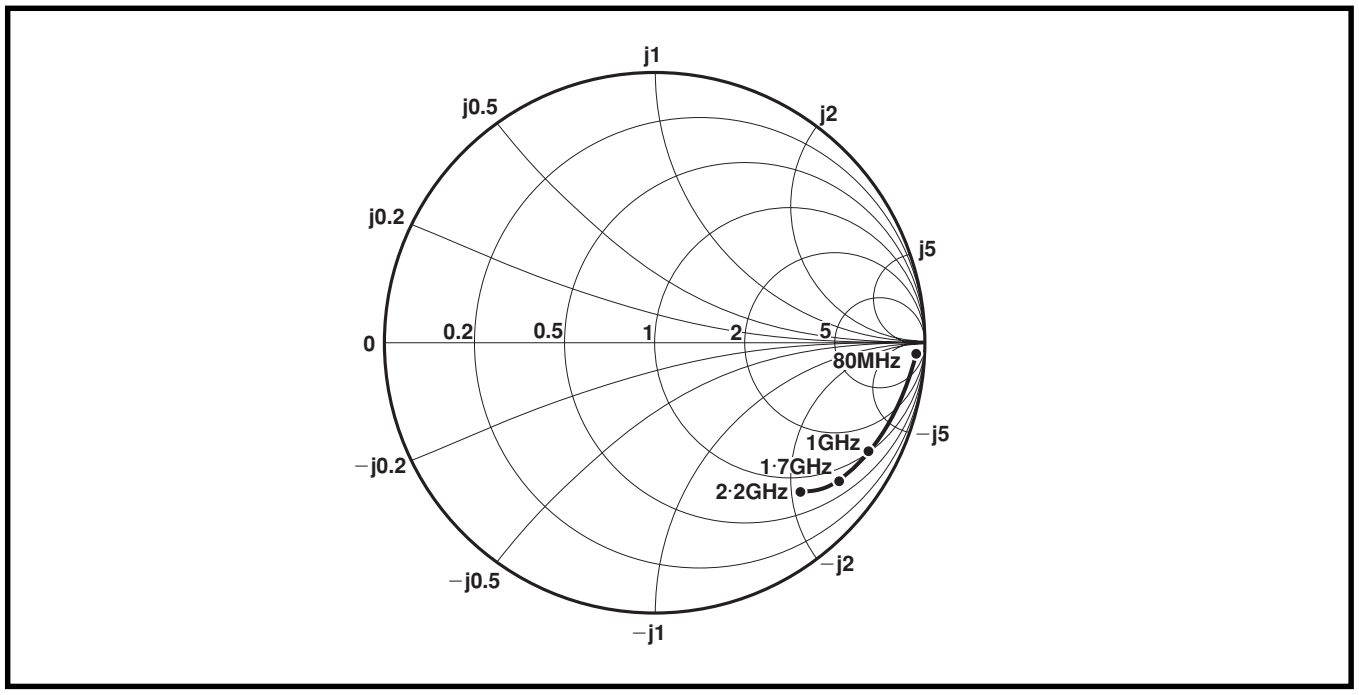


Figure 4 Synthesiser 1 RF input impedance

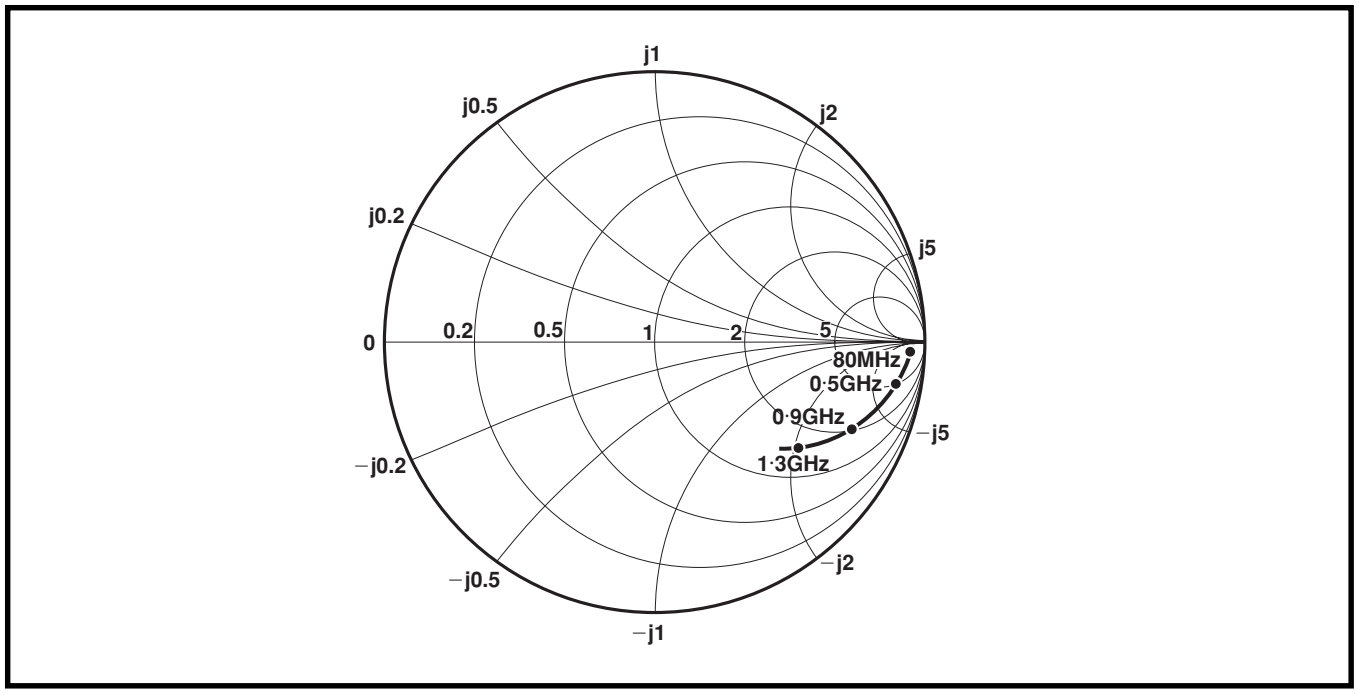


Figure 5 Synthesiser 2 RF input impedance

RU2	RU1	RU0	Ratio
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 1 Synthesiser 1 reference division ratio

RU2	RU1	RU0	Ratio
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

Table 2 Synthesiser 2 reference division ratio

CU1	CU0	Current (typical in mA)
0	0	0.12
0	1	0.26
1	0	0.55
1	1	1.2

Table 3 Synthesiser 1 charge pump current

CD	Current (typical in mA)
0	0.05
1	0.2

Table 4 Synthesiser 2 charge pump current

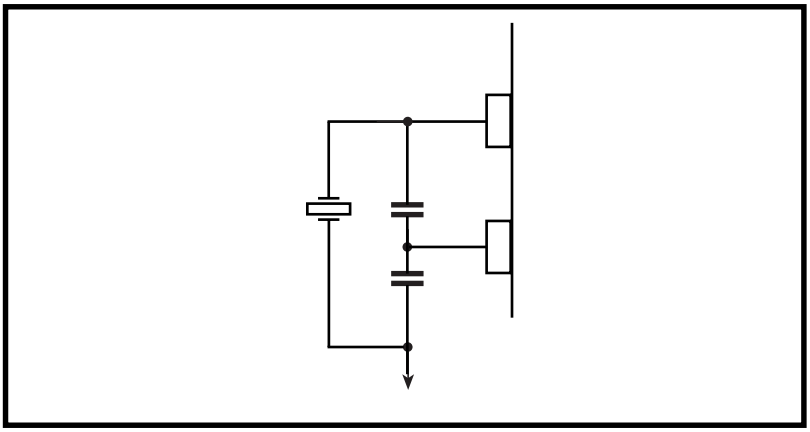


Figure 6 Crystal oscillator application

T2	T1	T0	Functional Description
X	X	0	Normal operation
0	0	1	Both charge pumps in sink mode
0	1	1	Both charge pumps in source mode
1	0	1	Port P1 = Fcomp1, P0 = Fcomp2 and charge pumps disabled
1	1	1	Port P1 = (Fpd1)/2, P0 = (Fpd2)/2

X = dont care

Figure 7 Test modes

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