MT90863

3V Rate Conversion Digital Switch

Advance Information

DS5034 ISSUE 3 March 1999

Features

- 2,048 × 512 and 512 x 512 switching among backplane and local streams
- Rate conversion between 2.048, 4.096 and 8.192Mb/s
- Optioal sub-rate switch configuration for 2.048 Mb/s streams
- Per-channel variable or constant throughput delay
- Compatible to HMVIP and H.100 specifications
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel message mode
- Per-channel direction control
- Per-channel high impedance output control
- Non-multiplexed microprocessor interface
- Connection memory block programming
- 3.3V local I/O with 5V tolerant inputs and TTL-compatible outputs
- IEEE-1149.1 (JTAG) Test Port

Applications

- Medium and large switching platforms
- CTI application
- Voice/data multiplexer
- Support ST-BUS, HMVIP and H.100 interfaces

Ordering Information

MT90863AL1	128 Pin MQFP
MT90863AG1	144 Pin BGA

-40 to +85 C

Description

The MT90863 Rate Conversion Switch provides switching capacities of 2,048 × 512 channels between backplane and local streams, and 512 x 512 channels for local streams. The connected serial inputs and outputs may have 32, 64 and 128 64kb/s channels per frame with data rates of 2.048Mb/s, 4.096Mb/s and 8.192Mb/s respectively.

The MT90863 also offers a sub-rate switching configuration which allows 2-bit wide 16kb/s data channels to be switched within the device.

The device has features (such as: message mode; input and output offset delay; direction control; and, high impedance output control) that are programmable on per-stream or per-channel basis.

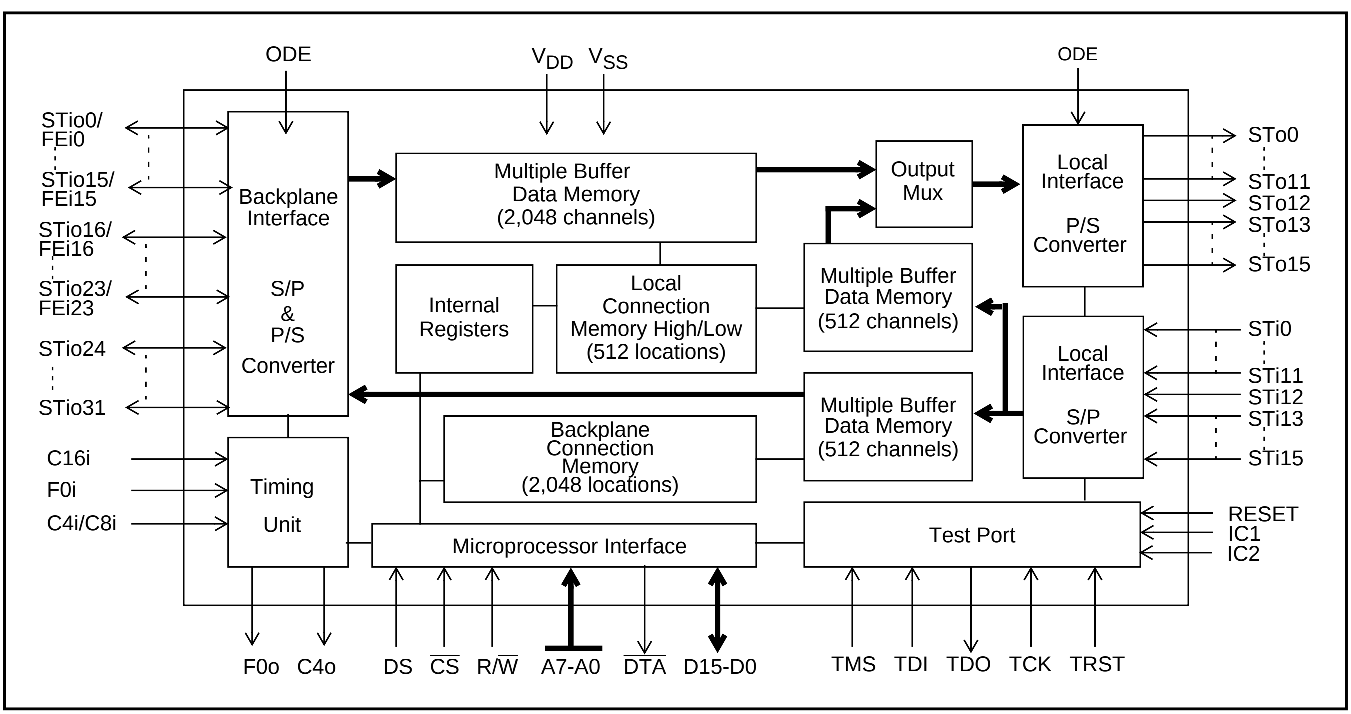


Figure 1 - Functional Block Diagram

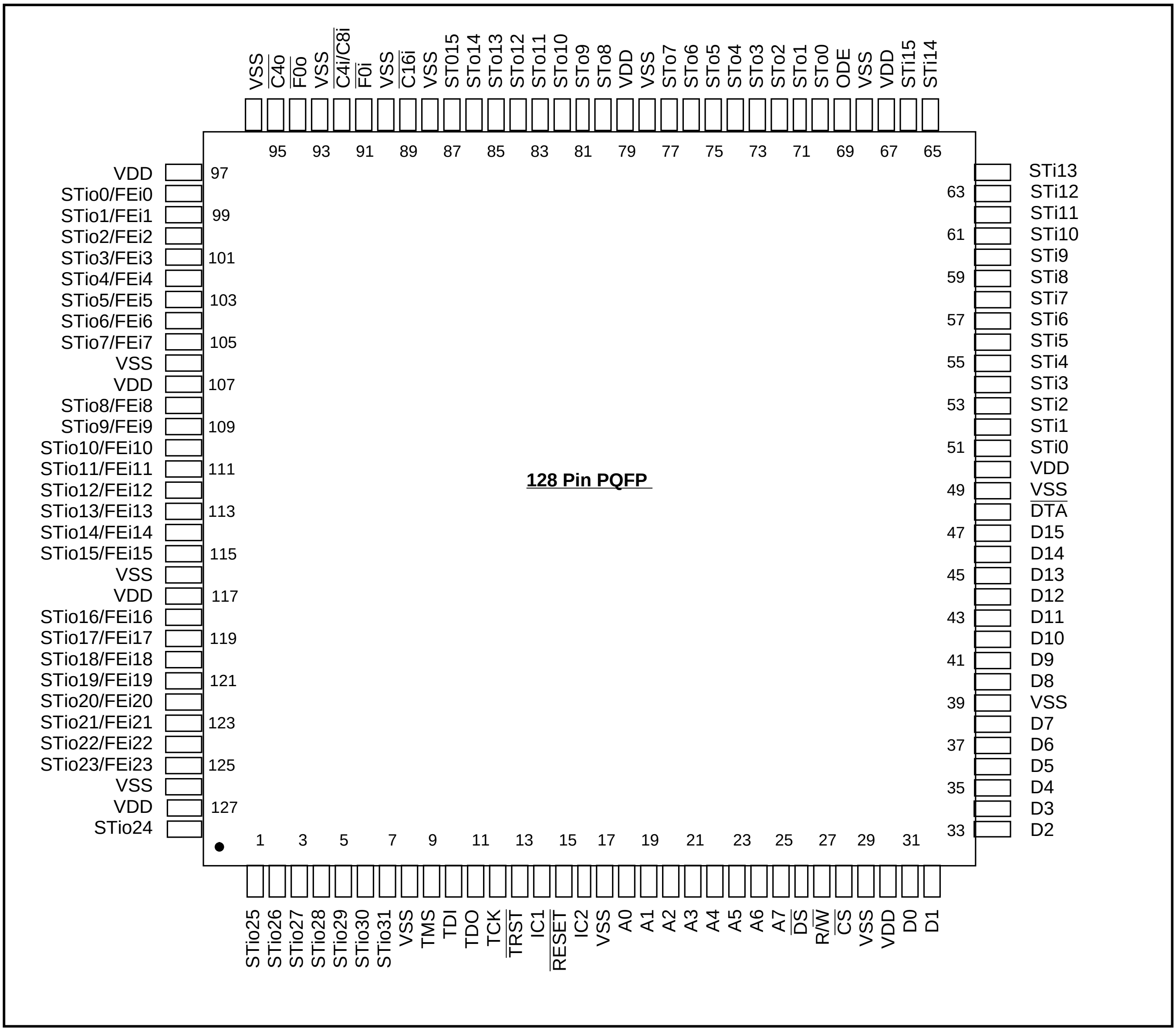


Figure 2 - MQFP Pin Connections

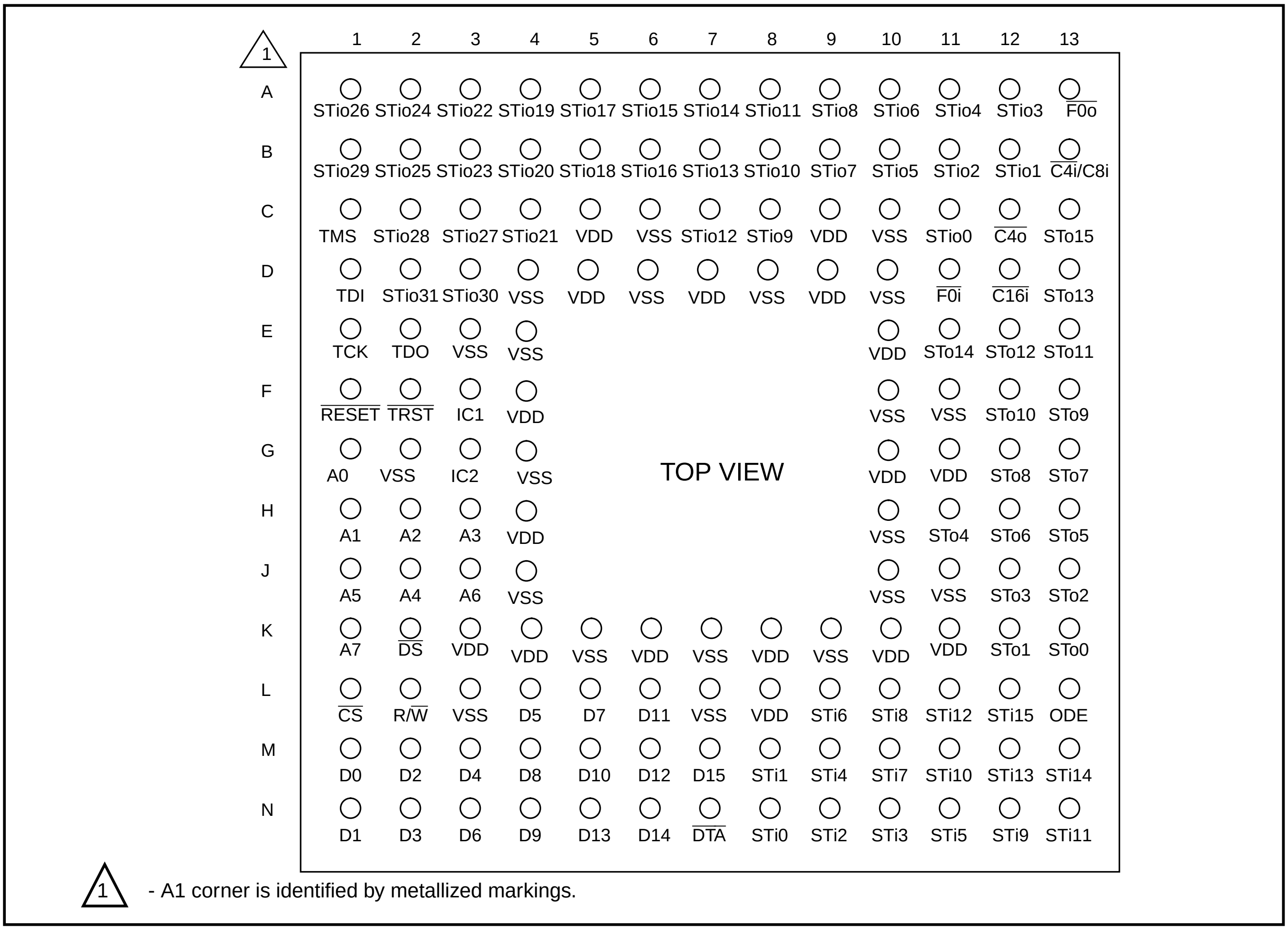


Figure 3 - BGA Pin Connections

Pin Description

128 MQFP Pin#	144 BGA Pin#	Name	Description
30,50,67, 79,97,107, 117,127	C5,C9,D5,D7, D9,E10,F4,G10 ,G11,H4, K3,K4,K6,K8 K10,K11,L8	V_{DD}	**+3.3 Volt Power Supply**
8,17,29,39, 49,68,78,8 8,90,93,96, 106, 116,126	C6,C10,D4,D6, D8,D10,E3,E4, F10,F11,G2, G4,H10,J4, J10,J11,K5 K7,K9,L3,L7	V_{SS}	**Ground**
89	D12	C16i	**Master Clock (5V Tolerant Input):** Serial clock for shifting data in/out on the serial streams. This pin accepts a 16.384 MHz clock.
91	D11	$\overline{\text{F0i}}$	**Master Frame Pulse (5V Tolerant Input):** In ST-BUS mode, this input accepts a 61ns wide negative frame pulse. In CT Bus mode, it accepts a 122ns wide negative frame pulse. In HMVIP mode, it accepts a 244ns wide negative frame pulse.

Pin Description (continued)

128 MQFP Pin#	144 BGA Pin#	Name	Description
92	B13	C4i/C8i	**HMVIP/CT Bus Clock (5V Tolerant Input):** When HMVIP mode is enabled, this pin accepts a 4.096MHz clock for HMVIP frame pulse alignment. When CT Bus mode is enabled, it accepts a 8.192MHz clock for CT frame pulse alignment.
94	A13	$\overline{\text{F0o}}$	**Frame Pulse (5V Tolerant Output):** A 244ns wide negative frame pulse that is phase locked to the master frame pulse (F0i).
95	C12	C4o	**C4 Clock (5V Tolerant Output):** A 4.096MHz clock that is phase locked to the master clock (C16i).
98-105, 108-115	C11, B12, B11, A12, A11, B10, A10, B9, A9, C8, B8, A8, C7, B7, A7, A6,	STio0 - 15 FEi0 - 15	**Serial Input Streams 0 to 15 / Frame Evaluation Inputs 0 to 15 (5V Tolerant I/O).** In 2Mb/s and HMVIP modes, these pins accept serial TDM data streams at 2.048 Mb/s with 32 channels per stream. In 4Mb/s or 8Mb/s mode, these pins accept serial TDM data streams at 4.096 or 8.192 Mb/s with 64 or 128 channels per stream respectively. In Frame Evaluation Mode (FEM), they are frame evaluation inputs.
118-125	B6, A5, B5, A4, B4, C4, A3, B3	STio16 - 23 FEi16 - 23	**Serial Input Streams 16 to 23 (5V Tolerant I/O).** In 2Mb/s or 4Mb/s mode, these pins accept serial TDM data streams at 2.048 or 4.096 Mb/s with 32 or 64 channels per stream respectively. In HMVIP mode, these pins have a data rate of 8.192Mb/s with 128 channels per stream. In Frame Evaluation Mode (FEM), they are frame evaluation inputs.
128, 1-7	A2, B2, A1, C3, C2, B1, D3, D2	STio24 - 31	**Serial Input Streams 24 to 31 (5V Tolerant I/O).** These pins are only used for 2Mb/s or 4Mb/s mode. They accept serial TDM data streams at 2.048 or 4.096 Mb/s with 32 or 64 channels per stream respectively.
9	C1	TMS	**Test Mode Select (3.3V Input with internal pull-up):** JTAG signal that controls the state transitions of the TAP controller.
10	D1	TDI	**Test Serial Data In (3.3V Input with internal pull-up):** JTAG serial test instructions and data are shifted in on this pin.
11	E2	TDO	**Test Serial Data Out (3.3V Output):** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG scan is not enabled.
12	E1	TCK	**Test Clock (5V Tolerant Input):** Provides the clock to the JTAG test logic.
13	F2	TRST	**Test Reset (3.3 V Input with internal pull-up):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up, or held low continuously, to ensure that the MT90863 is in the normal operation mode.
14	F3	IC1	**Internal Connection 1 (3.3V Input with internal pull-down):** Connect to V_{SS} for normal operation.
15	F1	RESET	**Device Reset (5V Tolerant Input):** This input (active LOW) puts the MT90863 in its reset state. This clears the device's internal counters and registers. It also brings microport data bus STio0 - 31 and STo0 - 15 to a high impedance state.
16	G3	IC2	**Internal Connection 2 (3.3V Input):** Connect to V_{SS} for normal operation.

Pin Description (continued)

128 MQFP Pin#	144 BGA Pin#	Name	Description
18-25	G1, H1, H2, H3, J2, J1,J3, K1	A0 - A7	**Address 0 - 7 (5V Tolerant Input):** These lines provide the A0 to A7 address lines to the internal memories.
26	K2	DS	**Data Strobe (5V Tolerant Input):** This active low input works in conjunction with $\overline{CS}$ to enable the read and write operations.
27	L2	R/$\overline{W}$	**Read/Write (5V Tolerant Input):** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
28	L1	CS	**Chip Select (5V Tolerant Input):** Active low input used by a microprocessor to activate the microprocessor port.
31-38, 40-47	M1, N1, M2, N2, M3, L4, N3, L5, M4, N4, M5, L6, M6, N5, N6, M7,	D0 - 7, D8 - D15	**Data Bus 0 -15 (5V Tolerant I/O):** These pins form the 16-bit data bus of the microprocessor port.
48	N7	DTA	**Data Transfer Acknowledgment (5V Tolerant Three-state Output):** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated.
51-54	N8, M8, N9, N10	STi0 - 3	**Serial Input Streams 0 to 3 (5V Tolerant Inputs):** In 2Mb/s or Subrate Switching mode, these inputs accept data rates of 2.048 Mb/s with 32 channels per stream. In 8Mb/s mode, these inputs accept data rates of 8.192 Mb/s with 128 channels per stream.
55-62	M9, N11, L9, M10, L10, N12, M11, N13	STi4 - 11	**Serial Input Streams 4 to 11 (5V Tolerant Inputs):** In 2Mb/s or Sub-rate Switching mode, these inputs accept data rates of 2.048Mb/s with 32 channels per stream.
63	L11	STi12	**Serial Input Streams 12 (5V Tolerant Input):** In 2Mb/s mode, this input accepts data rate of 2.048Mb/s with 32 channels per stream respectively. In Sub-rate Switching mode, this pin accepts 2.048Mb/s with 128 channels per stream for Sub-rate switching application.
64-66	M12, M13, L12	STi13 - 15	**Serial Input Streams 13 to 15 (5V Tolerant Inputs):** In 2Mb/s mode, these inputs accept a data rate of 2.048Mb/s with 32 channels per stream.
69	L13	ODE	**Output Drive Enable (5V Tolerant Input):** This is the output enable control for the STo0 to STo15 serial outputs and STio0 to STio31 serial bidirectional outputs.
70-73	K13, K12, J13, J12	STo0 - 3	**Serial Output Streams 0 to 3 (5V Tolerant Three-state Outputs):** In 2Mb/s or Sub-rate Switching mode, these outputs have data rates of 2.048 Mb/s with 32 channels per stream respectively. In 8Mb/s mode, these outputs have data rates of 8.192 Mb/s with 128 channels per stream
74-77, 80-83	H11, H13, H12, G13, G12, F13, F12, E13	STo4 - 7, STo8 - 11	**Serial Output Streams 4 to 11 (5V Tolerant Three-state Outputs):** In 2Mb/s or Sub-rate Switching mode, these outputs have data rates of 2.048Mb/s with 32 channels per stream

Pin Description (continued)

128 MQFP Pin#	144 BGA Pin#	Name	Description
84	E12	STo12	**Serial Output Streams 12 (5V Tolerant Three-state Output):** In 2Mb/s mode, this output has data rate of 2.048Mb/s with 32 channels per stream. In Sub-rate Switching mode, this pin has data rate of 2.048Mb/s with 128 channels per stream for Sub-rate switching application.
85-87	D13, E11, C13	STo13 - 15	**Serial Output Streams 13 to 15 (5V Tolerant Three-state Outputs):** In 2Mb/s mode, these outputs have a data rate of 2.048Mb/s with 32 channels per stream.

Device Overview

The Rate conversion Switch (MT90863) can switch up to 2,048 × 512 channels while also providing a rate conversion capability. It is designed to switch 64 kb/s PCM or N X 64 kb/s data between the backplane and local interfaces. When the device is in the sub-rate switching mode, 2-bit wide 16 kb/s data channels can be switched within the device. The device maintains frame integrity in data applications and minimum throughput delay for voice application on a per channel basis.

The backplane interface can operate at 2.048, 4.096 or 8.192 Mb/s, arranged in 125µs wide frames that contain 32, 64 or 128 channels, respectively. A built-in rate conversion circuit allows users to interface between backplane interface and the local interface which operates at 2.048 Mb/s or 8.192 Mb/s.

By using Mitel’s message mode capability, the microprocessor can access input and output time-slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-Bus devices.

The frame offset calibration function allows users to measure the frame offset delay for streams STio0 to STio23. The offset calibration is activated by a frame evaluation bit in the frame evaluation register. The evaluation result is stored in the frame evaluation registers and can be used to programme the input offset delay for individual streams using internal frame input offset registers.

Functional Description

A functional Block Diagram of the MT90863 is shown in Figure 1. One end of the MT90863 is used to interface with backplane applications, such as HMVIP or H.100 environments, while the other end supports the local switching environments.

Frame Alignment Timing

The Device Mode Selection (DMS) register allows users to select three different frame alignment timing modes. In ST-BUS modes, the master clock ($\overline{\text{C16i}}$) is always at 16.384 MHz. The frame pulse ($\overline{\text{F0i}}$) input accepts a negative frame pulse at 8kHz. The frame pulse goes low at the frame boundary for 61ns. The frame pulse output $\overline{\text{F0o}}$ provides a 244ns wide negative frame pulse and the $\overline{\text{C4o}}$ output provides a 4.094MHz clock. These two signals are used to support local switching applications. See Figure 4 for the ST-BUS timings.

In CT Bus mode, the $\overline{\text{C4i}}$/C8i pin accepts 8.192MHz clock for the CT Bus frame pulse alignment. The $\overline{\text{F0i}}$ is the CT bus frame pulse input. The CT frame pulse goes low at the frame boundary for 122ns. See Figure 5 for the CT Bus timing.

In HMVIP mode, the $\overline{\text{C4i}}$/C8i pin accepts 4.096MHz clock for the HMVIP frame pulse alignment. The $\overline{\text{F0i}}$ is the HMVIP frame pulse input. The HMVIP frame pulse goes low at the frame boundary for 244ns. See Figure 6 for the HMVIP timing.

Table 1 describes the input timing requirements for ST-BUS, CT Bus and HMVIP modes.

Switching Configuration

The device has four operation modes for the backplane interface and three operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent. See Table 2 and Table 3 for the selection of various operation modes via the programming of the DMS register.

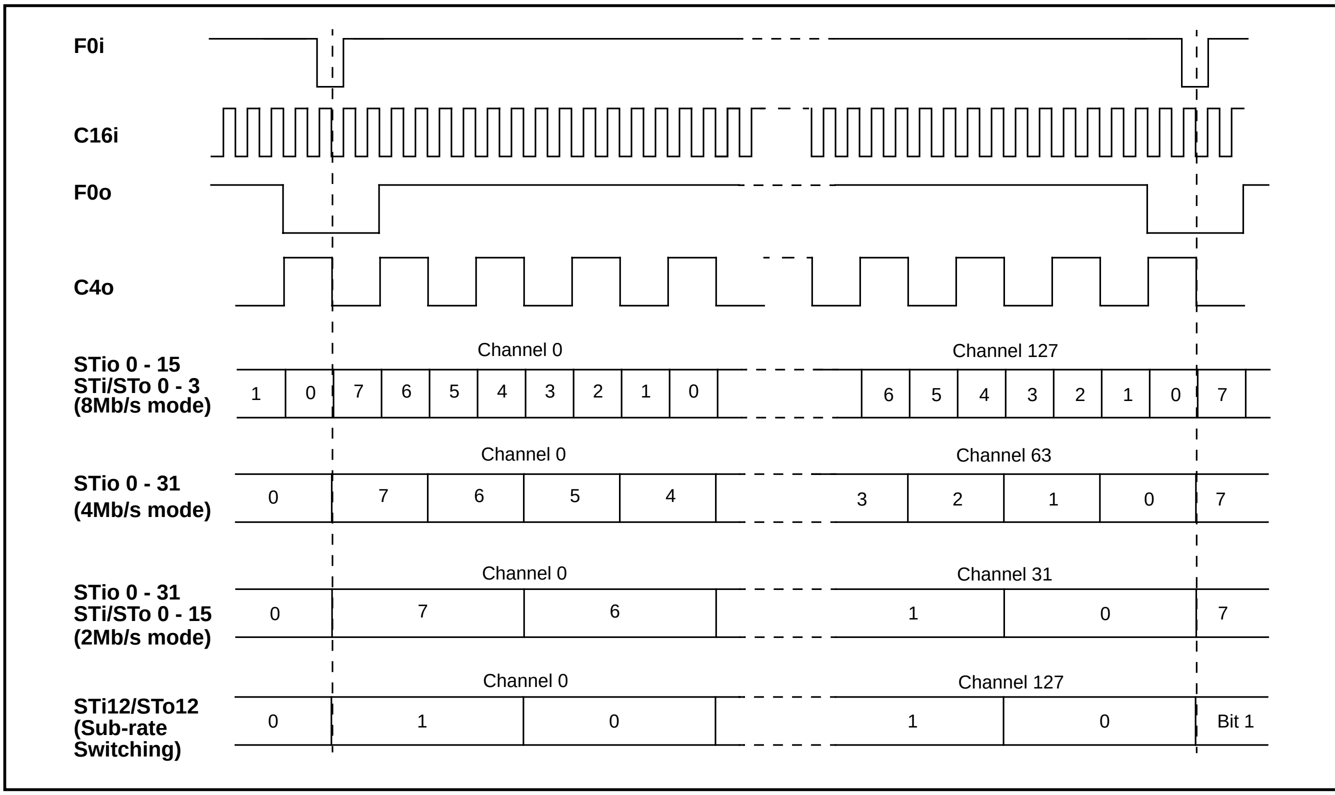


Figure 4 - ST-BUS Timing for 2, 4 and 8 Mb/s Data Streams

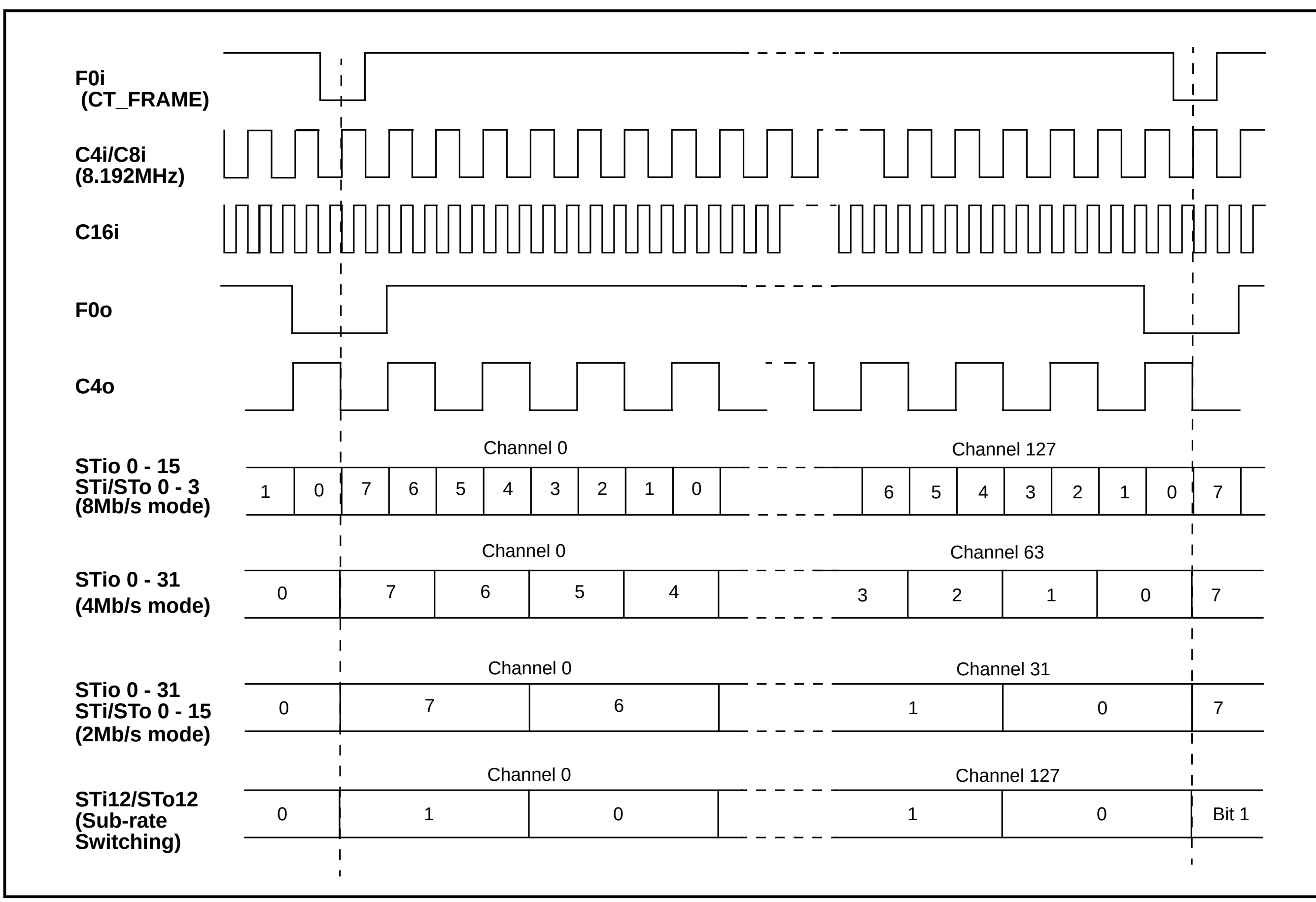


Figure 5 - CT Bus Mode Timing for 2, 4 and 8 Mb/s Data Streams

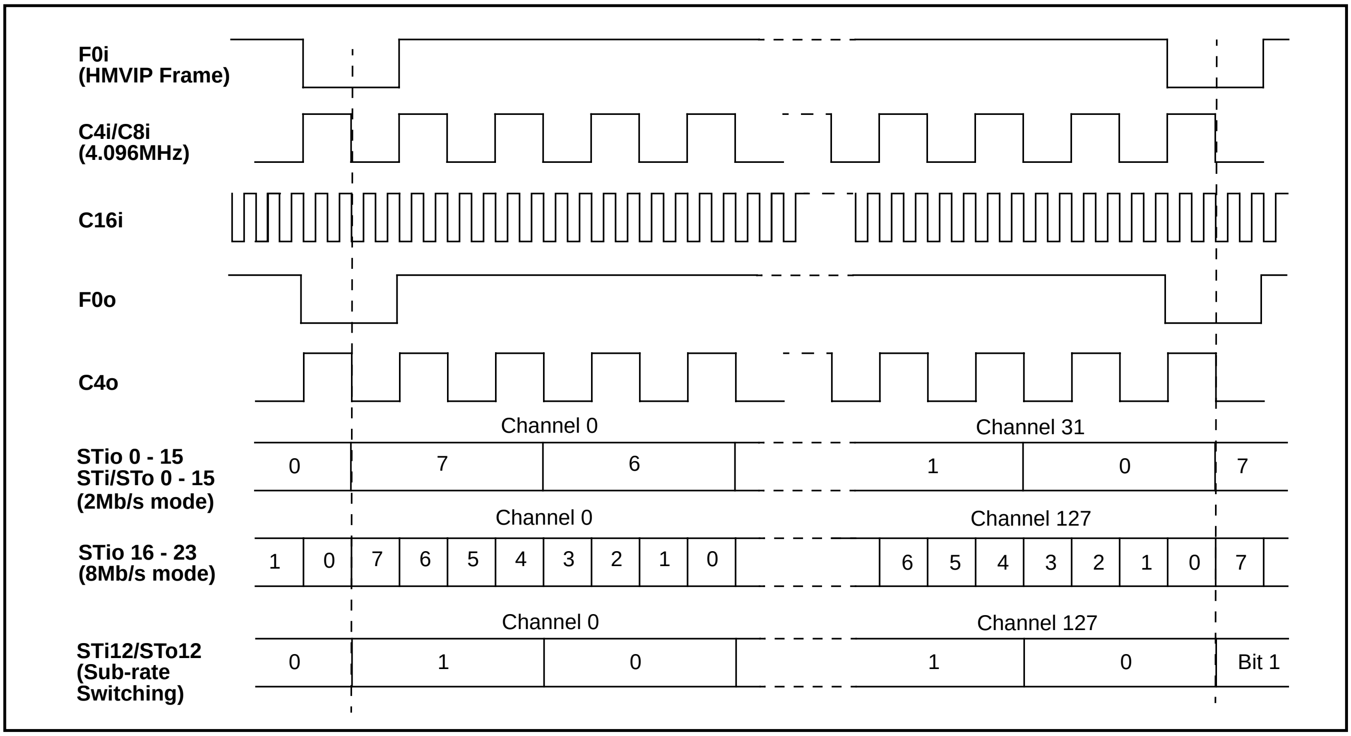


Figure 6- HMVIP Mode Timing for 2 and 8 Mb/s Data Streams

Backplane Interface

The backplane interface can be programmed to accept data streams of 2Mb/s, 4Mb/s or 8Mb/s. When 2Mb/s mode is enabled, STio0 to STio31 have a data rate of 2.048Mb/s. When 4Mb/s mode is enabled, STio0 to STio31 have a data rate of 4.096Mb/s. When 8Mb/s mode is enabled, STio0 to STio15 have a data rate of 8.192Mb/s. When HMVIP mode is enabled, STio0 to STio15 have a data rate of 2.048Mb/s and STio16 to STio23 have a data rate of 8.192Mb/s.

Table 2 describes the data rates and mode selection for the backplane interface.

Local Interface

Three operation modes, 2Mb/s, 8Mb/s and Sub-rate Switching mode, can be selected for the local interface. When 2Mb/s mode is selected, STi0 to STi15 and STo0 to STo15 have a 2.048Mb/s data rate. When 8Mb/s mode is selected, STi0 to STi3 and STo0 to STo3 have an 8.192Mb/s data rate. When Sub-rate Switching mode is selected, STi0 to STi11 and STo0 to STo11 have 2.048Mb/s data with 64kb/s data channels and STi12 and STo12 have a 2.048Mb/s data rate with 16kb/s data channels. Table 3 describes the data rates and mode selection for the local interface.

Input Frame Offset Selection

Input frame offset selection allows the channel alignment of individual backplane input streams, that operate at 8.192Mb/s (STio0-23), to be shifted against the input frame pulse ($\overline{\text{F0i}}$). This feature compensates for the variable path delays caused by serial backplanes of variable length. Such delays can be occur in large centralized and distributed switching systems.

Each backplane input stream can have its own delay offset value by programming the input delay offset registers (DOS0 to DOS5). Possible adjustment can range up to +4 master clock ($\overline{\text{C16i}}$) periods forward with resolution of half master clock period. See Table 10 and Table 11, and Figure 9, for frame input delay offset programming.

Output Advance Offset Selection

The MT90863 allows users to advance individual backplane output streams which operate at 8.192Mb/s (STio0-23) by half a master clock ($\overline{\text{C16i}}$) cycle. This feature is useful in compensating for variable output delays caused by various output loading conditions. The frame output offset registers (FOR0 & FOR1) control the output offset delays for each backplane output stream via the OFn bit programming. Table 12 and Figure 10 detail frame output offset programming.

Serial Input Frame Alignment Evaluation

The MT90863 provides the frame evaluation inputs, FEi0 to FEi23, to determine different data input delays with respect to the frame pulse $\overline{\text{F0i}}$. By using the frame evaluation input select bits (FE0 to FE4) of

Timing Signals	ST-BUS Mode	CT Bus Mode	HMVIP Mode
$\overline{\text{F0i}}$ Width	61ns	122ns	244ns
$\overline{\text{C4i}}$/C8i	Not Required	8.192MHz	4.096MHz
$\overline{\text{C16i}}$		16.384MHz	
$\overline{\text{F0o}}$ Width		244ns	
$\overline{\text{C4o}}$		4.096MHz	

Table 1 - Timing Signals Requirements for Various Operation Modes

DMS Register Bits			Modes	Backplane Interface	Data Rate
BMS2	BMS1	BMS0			
0	0	0	2Mb/s, ST-BUS Mode	STio0 - 31	2.048 Mb/s
0	0	1	2Mb/s, CT Bus Mode	STio0 - 31	2.048 Mb/s
0	1	0	4Mb/s, ST-BUS Mode	STio0 - 31	4.096 Mb/s
0	1	1	4Mb/s, CT Bus Mode	STio0 - 31	4.096 Mb/s
1	0	0	8Mb/s, ST-BUS Mode	STio0 - 15	8.192 Mb/s
				STio16 - 31	Not available
1	0	1	8Mb/s, CT Bus Mode	STio0 - 15	8.192 Mb/s
				STio16 - 31	Not available
1	1	0	HMVIP Mode	STio0 - 15	2.048 Mb/s
				STio16 - 23	8.192 Mb/s
				STio24 - 31	Not available

Table 2 - . Mode Selection for Backplane interface

DMS Register Bits		Modes	Local Interface	Data Rate
LMS1	LMS0			
0	0	2Mb/s Mode	STi0 - 15	2.048 Mb/s
			STo0 - 15	2.048 Mb/s
0	1	Sub-Rate Switching Mode	STi0 - 11	2.048 Mb/s
			STi12	Sub-rate Switching Input Stream at 2.048 Mb/s
			STi13 - 15	Not available
			STo0 - 11	2.048 Mb/s
			STo12	Sub-rate Switching Output Stream at 2.048Mb/s
			STo13 - 15	Not available
1	0	8Mb/s Mode	STi0 - 3	8.192 Mb/s
			STi4 - 15	Not available
			STo0 - 3	8.192 Mb/s
			STo4 - 15	Not available

Table 3 - . Mode Selection for Local Interface

the frame alignment register (FAR), users can select one of the twenty-four frame evaluation inputs for the frame alignment measurement.

A measurement cycle is started by setting the start frame evaluation (SFE) bit low for at least one frame. Then the evaluation starts when the SFE bit in the Internal Mode Selection (IMS) register is changed from low to high. One frame later, the complete frame evaluation (CFE) bit of the frame alignment register changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 9 of the FAR register. The SFE bit must be set to zero before a new measurement cycle is started.

The falling edge of the frame measurement signal (FEi) is evaluated against the falling edge of the frame pulse ($\overline{\text{F0i}}$). Table 8 and Figure 8 describe the frame alignment register.

Memory Block Programming

The MT90863 has two connection memories: the backplane connection memory and the local connection memory. The local connection memory is partitioned into high and low parts. The IMS register provides users with the capability of initializing the local connection memory low and the backplane connection memory in two frames. Bit 11 to bit 13 of every backplane connection memory location will be programmed with the pattern stored in bit 7 to bit 9 of the IMS register. Bit 12 to 15 of every local connection memory low location will be programmed with the pattern stored in bits 3 to 6 of the IMS register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable (BPE) bit of the IMS register is set to high, the block programming data will be loaded into bits 11 to 13 of every backplane connection memory and bits 12 to 15 of every local connection memory low. The other connection memory bits are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero. See Figure 7 for the connection memory contents when the device is in block programming mode.

Delay Through the MT90863

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the L$\overline{\text{V}}$/C and B$\overline{\text{V}}$/C bits of the local and backplane connection memory as described in Table 16 and Table 19.

Variable Delay Mode (L$\overline{\text{V}}$/C or B$\overline{\text{V}}$/C bit = 0)

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams.

Constant Delay Mode (L$\overline{\text{V}}$/C bit or B$\overline{\text{V}}$/C= 1)

In this mode a multiple data memory buffer is used to maintain frame integrity in all switching configurations.

Microprocessor Interface

The MT90863 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed buses. The required microprocessor signals are the 16-bit data bus (D0-D15), 8-bit address bus (A0-A7) and 4 control lines ($\overline{\text{CS}}$, DS, R/$\overline{\text{W}}$ and $\overline{\text{DTA}}$). See Figure 16 for Motorola non-multiplexed bus timing.

The MT90863 microprocessor port provides access to the internal registers, connection and data memories. All locations provide read/write access except for the Data Memory and the Data Read Register which are read only.

Memory Mapping

The address bus on the microprocessor interface selects the internal registers and memories of the MT90863. If the A7 address input is low, then the registers are addressed by A6 to A0 as shown in Table 4.

If the A7 is high, the remaining address input lines are used to select the serial input or output data streams corresponding to the subsection of memory positions. For data memory reads, the serial inputs are selected. For connection memory writes, the serial outputs are selected.

The control, device mode selection and internal mode selection registers control all the major functions of the device. The device mode selection register and internal mode selection register should be programmed immediately after system power-up

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BBPD 2	BBPD 1	BBPD 0	0	0	0	0	0	0	0	0	0	0	0

Backplane Connection Memory (BCM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBPD 3	LBPD 2	LBPD 1	LBPD 0	0	0	0	0	0	0	0	0	0	0	0	0

Local Connection Memory Low (LCML)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Local Connection Memory High (LCMH)

Figure 7 - Block Programming Data in the Connection Memories

A7 (Note 1)	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	Control Register, CR
0	0	0	0	0	0	0	1	Device Mode Selection Register, DMS
0	0	0	0	0	0	1	0	Internal Mode Selection Register, IMS
0	0	0	0	0	0	1	1	Frame Alignment Register, FAR
0	0	0	0	0	1	0	0	Input Offset Selection Register 0, DOS0
0	0	0	0	0	1	0	1	Input Offset Selection Register 1, DOS1
0	0	0	0	0	1	1	0	Input Offset Selection Register 2, DOS2
0	0	0	0	0	1	1	1	Input Offset Selection Register 3, DOS3
0	0	0	0	1	0	0	0	Input Offset Selection Register 4, DOS4
0	0	0	0	1	0	0	1	Input Offset Selection Register 5, DOS5
0	0	0	0	1	0	1	0	Frame Output Offset Register, FOR0
0	0	0	0	1	0	1	1	Frame Output Offset Register, FOR1
0	0	0	0	1	1	0	0	Address Buffer Register, ABR
0	0	0	0	1	1	0	1	Data Write Register, DWR
0	0	0	0	1	1	1	0	Data Read Register, DRR
1 1 1 1 1	0 0 0 0 0	0 0 0 0 0	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 0 Ch 1 . Ch 30 Ch 31 (Note 2)
1 1 . 1 1	0 0 . 1 1	1 1 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 32 Ch 33 . Ch 126 Ch 127 (Note 3)

Notes:
1. Bit A7 must be high for access to data and connection memory positions. Bit A7 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2Mb/s.
3. Channels 0 to 127 are used when serial stream is at 8Mb/s

Table 4 - Address Memory Map

to establish the desired switching configuration as explained in the Frame Alignment Timing and Switching Configurations sections.

The control register is used to control the switching operations in the MT90863. It selects the internal memory locations that specify the input and output channels selected for switching.

Control register data consists of: the memory block programming bit (MBP): the memory select bits (MS0-2); and, the stream address bits (STA0-4). The memory block programming bit allows users to program the entire connection memory block, (see Memory Block Programming section). The memory select bits control the selection of the connection memory or the data memory. The stream address bits define an internal memory subsections corresponding to serial input or serial output streams.

The data in the DMS register consists of the local and backplane mode selection bits (LMS0-1 and BMS0-2) to enable various switching modes for local and backplane interfaces respectively.

The data in the IMS register consists of block programming bits (LBPD0-3 and BBPD0-2), block programming enable bit (BPE), output standby bit (OSB) and start frame evaluation bit (SFE). The block programming enable bit allows users to program the entire backplane and local connection memories, (see Memory Block Programming section). If the ODE pin is low, the OSB bit enables (if high) or disables (if low) all ST-BUS output drivers. If the ODE pin is high, the contents of the OSB bit is ignored and all ST-BUS output drivers are enabled.

See Table 5 for the output high impedance control.

Address Buffer Mode

The implementation of the address buffer, data read and data write registers allows faster memory read/ write operation for the microprocessor port. See Table 6 and following for bit assignments.

The address buffer mode is controlled by the AB bit in the control register. The targeted memory for data read/write is selected by the MS0-2 bits in the control register.

The data write register (DWR) contains the data to be transferred to the memory. The data read register (DRR) contains the data transferred from the memory.

The address buffer register (ABR) allow users to specify the read or write address by programming the stream address bits (SA0-4) and the channel address bits (CA0-6). Data transfer from/to the memory is controlled by the read/write select bits (RS, WS). The complete data access (CDA) bit indicates the completion of data transfer between the memory and DWR or DRR register.

Write Operation Using Address Buffer Mode

Enable the address buffer mode by setting the AB bit from low to high. Program the DWR register with data to be transferred to memory. Load the ABR register with proper channel and stream information. Change the WS bit in the ABR register from low to high to initiate the data transfer from the DWR register to the memory. After several master clock cycles, the CDA bit in the ABR register changes from low to high to signal the completion of data transfer and resets the WS bit to low. Repeat the above steps for subsequent memory write operations. Disable the address buffer write operation by setting the AB bit to low.

Read Operation Using Address Buffer Mode

Enable the address buffer mode by setting the AB bit from low to high. Program the ABR register with proper channel and stream information. Change the RS bit in the ABR register from low to high to initiate the data transfer from the memory to the DRR

ODE pin	OSB bit in IMS register	DC bit in Backplane CM	STio0-31 Output Driver Status	OE bit in Local CM	STo0-15 Output Driver Status
Don’t Care	Don’t Care	0	Per Channel High Impedance	0	Per Channel High Impedance
0	0	Don’t care	High Impedance	Don’t care	High Impedance
0	1	1	Enable	1	Enable
1	Don’t care	1	Enable	1	Enable

Table 5 -. Output High Impedance Control

Read/Write Address: 00_H, Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	AB	CT	MBP	MS2	MS1	MS0	STA4	STA3	STA2	STA1	STA0

Bit	Name	Description
15-11	Unused	Must be zero for normal operation.
10	AB	**Address Buffer.** When 1, enables the address buffer, data write and data read registers for accessing various memory locations for fast microport access. When 0, disables the address buffer, data write & data read registers.
9	CT	**Channel Tri-state.** When 1, the last bit of each output channel is tri-stated for -22ns against the channel boundary. When 0, the last bit of each channel is not tri-stated.
8	MBP	**Memory Block Program.** When 1, the connection memory block programming feature is ready for the programming of bit 11 to 13 for backplane connection memory, bit 12 to 15 for local connection memory low. When 0, this feature is disabled.
7 - 5	MS2-0	**Memory Select Bits.** These three bits are used to select connection and data memory functions as follows: <u>MS2-0</u> <u>Memory Selection</u> 000 Local Connection Memory Low Read/Write, 001 Local Connection Memory High Read/Write, 010 Backplane Connection Memory Read/Write, 011 Local Data Memory Read, 100 Backplane Data Memory Read,
4 - 0	STA4-0	**Stream Address Bits**. The binary value expressed by these bits refers to the input or output data stream, which corresponds to the subsection of memory made accessible for subsequent operations. (STA4 = MSB, STA0 = LSB)

Table 6 - Control (CR) Register Bits

Read/Write Address: 01_H, Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	LMS1	LMS0	BMS2	BMS1	BMS0

Bit	Name	Description
15 - 5	unused	Reserved
4 - 3	LMS	**Local Mode Selection Bit.** The binary value expressed by these bits refers to the following backplane interface switching modes: <u>LMS1-0</u> <u>Local Switching Mode</u> 00 2Mb/s ST-BUS Mode 01 2Mb/s Sub-rate Switching Mode 10 8Mb/s ST-Bus Mode
2 - 0	BMS2-0	**Backplane Mode Selection Bits**. The binary value expressed by these bits refers to the following backplane interface switching modes: <u>BMS2-0</u> <u>Backplane Switching Mode</u> 000 2Mb/s ST-BUS Mode 001 2Mb/s CT Bus Mode 010 4Mb/s ST-BUS Mode 011 4Mb/s CT Bus Mode 100 8Mb/s ST-BUS Mode 101 8Mb/s CT Bus Mode 110 HMVIP Mode

Table 7 - Device Mode Selection (DMS) Register Bits

register. After several master clock cycles, the CDA bit in the ABR register changes from low to high to signal the completion of data transfer and resets the RS bit to low. Read the DRR register to obtain the data transferred from the memory. Repeat the above steps for subsequent memory read operations. Disable the address buffer read operation by setting the AB bit to low.

Backplane Connection Memory Control

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular STio output streams.

The B$\overline{\text{V}}$/C (Variable/Constant Delay) bit of each backplane connection memory location allows the per-channel selection between variable and constant throughput delay modes for all STio channels.

In message mode, the message channel (BMC) bit of the backplane connection memory enables (if high) an associated STio output channel. If the BMC bit is low, the contents of the backplane connection memory stream address bit (BSAB) and channel address bit (BCAB) defines the source information (stream and channel) of the time-slot that will be switched to the STio streams. When message mode is enabled, only the lower half (8 least significant bits) of the backplane connection memory is transferred to the STio pins.

Local Connection Memory Control

The local connection memory controls the local interface switching configuration. Local connection memory is split into high and low parts. Locations in local connection memory are associated with particular STo output streams.

The L/B (Local/Backplane Select) bit of each local connection memory location allows per-channel selection of source streams from local or backplane interface.

The L$\overline{\text{V}}$/C (Variable/Constant Delay) bit of each local connection memory location allows the per-channel selection between variable and constant throughput delay modes for all STo channels.

In message mode, the local connection memory message channel (LMC) bit enables (if high) an associated STo output channel. If the LMC bit is low, the contents of the stream address bit (LSAB) and the channel address bit (LCAB) of the local connection memory defines the source information (stream and channel) of the time-slot that will be switched to the STo streams. When message mode is enabled, only the lower half (8 least significant bits) of the local connection memory low bits are transferred to the STo pins.

When sub-rate switching is enabled, the LSR0-1 bits in the local connection memory high define which bit position contains the sub-rate data.

$\overline{\text{DTA}}$ Data Transfer Acknowledgment Pin

The $\overline{\text{DTA}}$ pin is driven LOW by internal logic to indicate (to the CPU) that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then switches to the high-impedance state. If a short or signal contention prevents the $\overline{\text{DTA}}$ pin from reaching a valid logic HIGH, it will continue to drive for approximately 15nsec before switching to the high-impedance state.

Initialization of the MT90863

During power up, the $\overline{\text{TRST}}$ pin should be pulsed low, or held low continuously, to ensure that the MT90863 is in the normal operation mode. A 5KΩ pull-down resistor can be connected to this pin so that the device will not enter the JTAG test mode during power up.

After power up, the contents of the connection memory can be in any state. The ODE pin should be held low after power up to keep all serial outputs in a high impedance state until the microprocessor has initialized the switching matrix. This procedure prevents two serial outputs from driving the same stream simultaneously.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the switch. The memory block programming feature can also be used to quickly initialize the DC and OE bit in the backplane and local connection memory respectively.

When this process is complete, the microprocessor controlling the matrices can either bring the ODE pin high or enable the OSB bit in IMS register to relinquish the high impedance state control.

Read/Write Address: 02_H,
Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	BBPD 2	BBPD 1	BBPD 0	LBPD 3	LBPD 2	LBPD 1	LBPD 0	BPE	OSB	SFE

Bit	Name	Description
15-10	Unused	Must be zero for normal operation.
9-7	BBPD2-0	**Backplane Block Programming Data.** These bits carry the value to be loaded into the backplane connection memory block when the Memory Block Programming feature is active. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of bits BBPD2-0 are loaded into the bit 13 to bit 11 position of the backplane connection memory. Bit 15, bit 14 and bit 10 to bit 0 of the backplane connection memory are zeroed.
6-3	LBPD3-0	**Local Block Programming Data.** These bits carry the value to be loaded into the local connection memory block when the Memory Block Programming feature is active. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of bits LBPD3-0 are loaded into the bit 15 to bit 12 position of the local connection memory. Bit 11 to bit 0 of the local connection memory low are zeroed. Bit 15 to bit 0 of local connection memory high are zeroed.
2	BPE	**Begin Block Programming Enable.** A zero to one transition of this bit enables the memory block programming function. The BPE, BBPD2-0 and LBPD3-0 bits in the IMS register must be defined in the same write operation. Once the BPE bit is set high, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE or MBP can be set to 0 to abort the programming operation. When BPE = 1, the other bits in the IMS register must not be changed for two frames to ensure proper operation.
1	OSB	**Output Stand By.** This bit controls the device output drivers. OSB bit / ODE pin / OE bit / STio0 - 31, STo0 - 15 0 / 0 / 1 / High impedance state 1 / 0 / 1 / Enable X / 1 / 1 / Enable X / X / 0 / Per-channel high impedance
0	SFE	**Start Frame Evaluation.** A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. Set this bit to zero for at least one frame (125µs) to start another frame evaluation.

Table 8 - Internal Mode Selection (IMS) Register Bits

Read/Write Address: 03_H,
Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE4	FE3	FE2	FE1	FE0	CFE	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Bit	Name	Description
15-11	FE4-0	**Frame Evaluation Input Select.** The binary value expressed in these bits refers to the frame evaluation inputs, FEi0 to FEi23.
10	CFE	**Complete Frame Evaluation.** When CFE = 1, the frame evaluation is completed and bits FD9 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the IMS register is changed from 1 to 0. This bit is read-only.
9	FD9	**Frame Delay Bit 11.** The falling edge of FE is sampled during the CLK-high phase (FD9 = 1) or during the CLK-low phase (FD9 = 0). This bit allows the measurement resolution to 1/2 CLK cycle. This bit is read-only.
8-0	FD8-0	**Frame Delay Bits.** The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the IMS register changes from 1 to 0. (FD8 = MSB, FD0 = LSB). These bits are also read-only

Table 9 - Frame Alignment (FAR) Register Bit

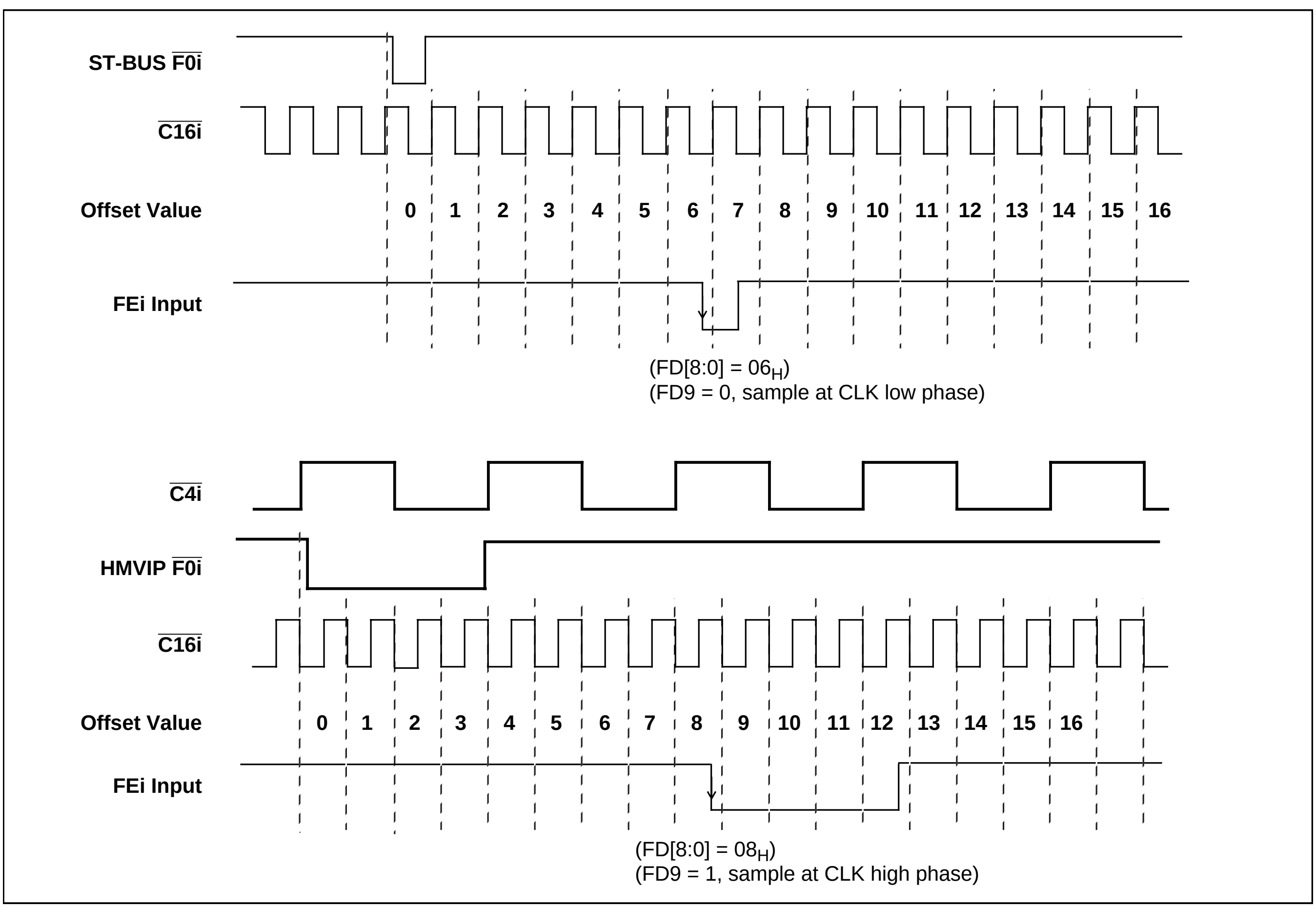


Figure 8 - Example for Frame Alignment Measurement

Read/Write Address:	04_H for DOS0 register,
	05_H for DOS1 register,
	06_H for DOS2 register,
	07_H for DOS3 register,
	08_H for DOS4 register,
	09_H for DOS5 register,
Reset value:	0000_H for all DOS registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF32	IF31	IF30	**DLE3**	IF22	IF21	IF20	**DLE2**	IF12	IF11	IF10	**DLE1**	IF02	IF01	IF00	**DLE0**

DOS0 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF72	IF71	IF70	**DLE7**	IF62	IF61	IF60	**DLE6**	IF52	IF51	IF50	**DLE5**	IF42	IF41	IF40	**DLE4**

DOS1 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF112	IF111	IF110	**DLE11**	IF102	IF101	IF100	**DLE10**	IF92	IF91	IF90	**DLE9**	IF82	IF81	IF80	**DLE8**

DOS2 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF152	IF151	IF150	**DLE15**	IF142	IF141	IF140	**DLE14**	IF132	IF131	IF130	**DLE13**	IF122	IF121	IF120	**DLE12**

DOS3 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF192	IF191	IF190	**DLE19**	IF182	IF181	IF180	**DLE18**	IF172	IF171	IF170	**DLE17**	IF162	IF161	IF160	**DLE16**

DOS4 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF232	IF231	IF230	**DLE23**	IF222	IF221	IF220	**DLE22**	IF212	IF211	IF210	**DLE21**	IF202	IF201	IF200	**DLE20**

DOS5 register

Name (Note 1)	Description
IFn2, IFn1, IFn0	**Input Offset Bits 2,1 & 0.** These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the STio pin: i.e., to start a new frame. The input frame offset can be selected to +4 clock periods from the point where the external frame pulse input signal is applied to the $\overline{\text{F0i}}$ inputs of the device.
DLEn	**Data Latch Edge.** ST-BUS mode: DLEn =0, if clock rising edge is at the 3/4 point of the bit cell. DLEn =1, if clock falling edge is at the 3/4 point of the bit cell.
Note 1: n denotes a STio stream number from 0 to 23.	

Table 10 - Frame Delay Offset (DOS) Register Bits

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD9	FD2	FD1	FD0	IFn2	IFn1	IFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+ 0.5 clock period shift	0	0	0	0	0	0	0	1
+1.0 clock period shift	1	0	0	1	0	0	1	0
+1.5 clock period shift	0	0	0	1	0	0	1	1
+2.0 clock period shift	1	0	1	0	0	1	0	0
+2.5 clock period shift	0	0	1	0	0	1	0	1
+3.0 clock period shift	1	0	1	1	0	1	1	0
+3.5 clock period shift	0	0	1	1	0	1	1	1
+4.0 clock period shift	1	1	0	0	1	0	0	0
+4.5 clock period shift	0	1	0	0	1	0	0	1

Table 11 - Offset Bits (IFn2, IFn1, IFn0, DLEn) & Input Offset Bits (FD9, FD2-0)

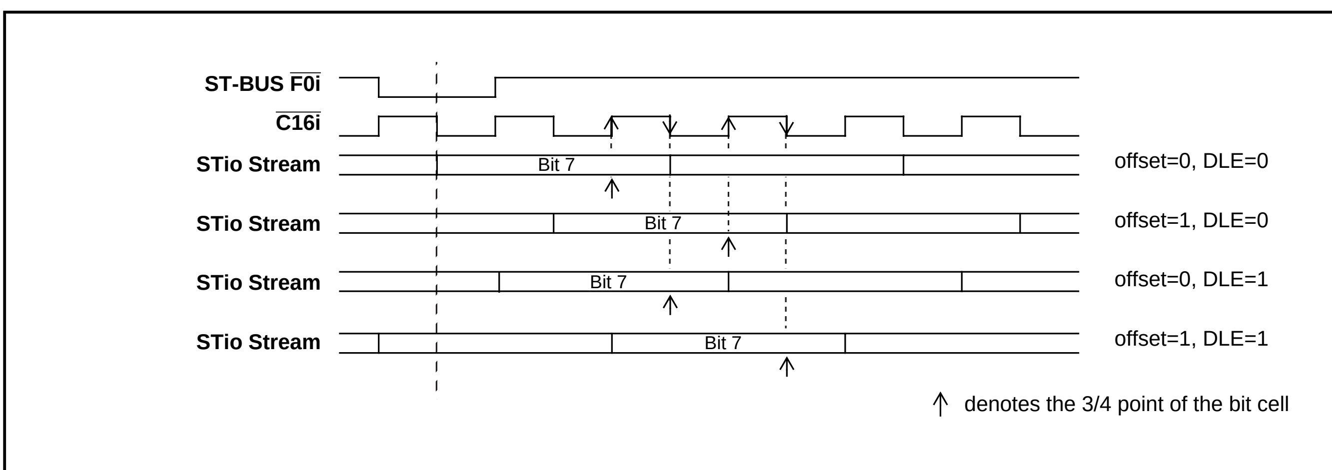


Figure 9 - Examples for Input Offset Delay Timing

Read/Write Address: $0A_H$ for FOR0 register,
$0B_H$ for FOR1 register,
Reset value: 0000_H for all FOR registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OF15	OF14	OF13	OF12	OF11	OF10	OF09	OF08	OF07	OF06	OF05	OF04	OF03	OF02	OF01	OF00

FOR0 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	OF23	OF22	OF21	OF20	OF19	OF18	OF17	OF16

FOR1 register

Bit	Name (Note 1)	Description
15-0 (FOR0) 7-0 (FOR1)	OFn	**Output Offset Bit.** When 0, the first bit of the serial output stream has normal alignment with the frame pulse. When 1, the first bit of the serial output stream is advanced by 1/2 CLK cycle with respect to the frame pulse. See .
15-8 (FOR1)	Unused	Must be zero for normal operation.
Note 1: n denotes a STio stream number from 0 to 23		

Table 12 - Frame Output Offset (FOR) Register Bits

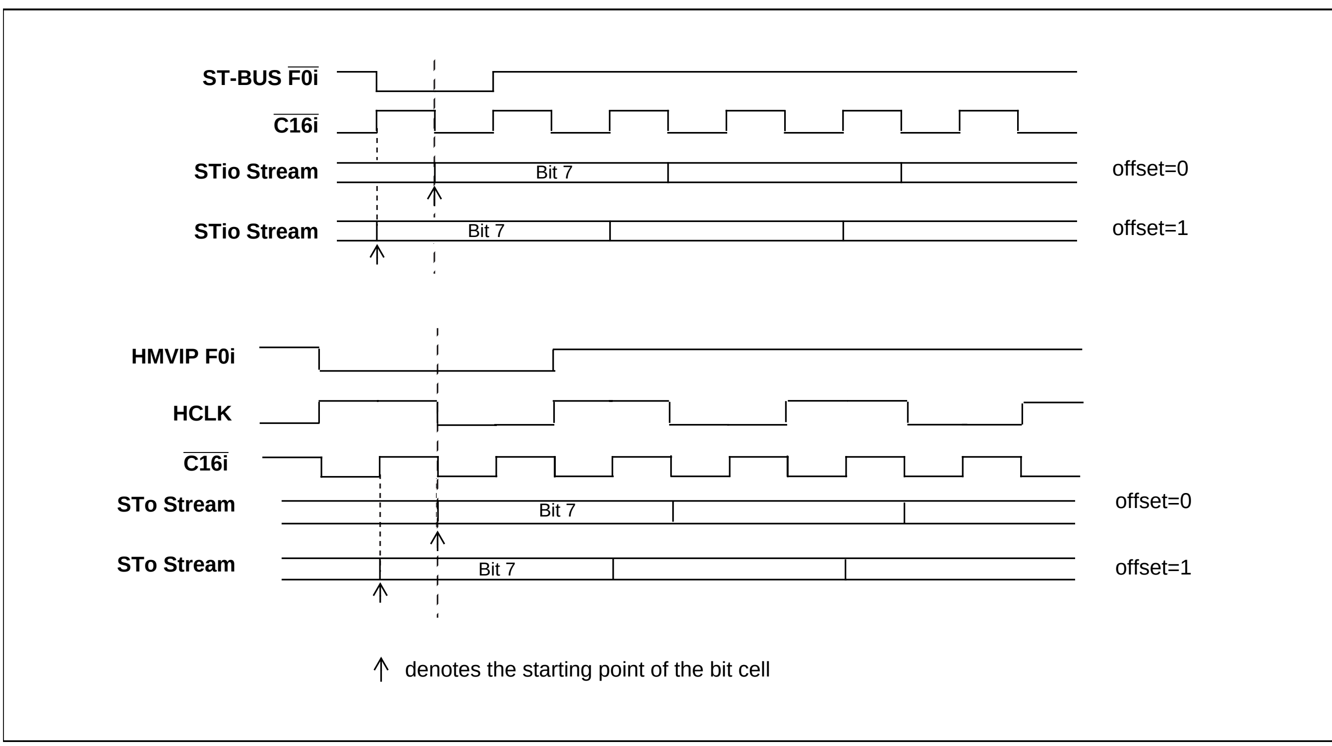


Figure 10 - Examples for Frame Output Offset Timing

Read/Write Address: $0C_H$ for ABR register,
Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CDA	RS	WS	CA6	CA5	CA4	CA3	CA2	CA1	CA0	SA4	SA3	SA2	SA1	SA0

Bit	Name	Description
15	unused	Reserved
14	CDA	**Complete Data Access.** This bit is read only. This bit changes from 0 to 1 when data transfer is completed between memory and the data read register or data write register. When the RS or WS bit in this register is changed from 1 to 0, this bit is reset to zero.
13	RS	**Read Select.** A zero to one transition of this bit initiates the data transfer from memory to the data read register. This bit is reset to zero when the CDA bit changes from 0 to 1.
12	WS	**Write Select.** A zero to one transition of this bit initiates the data transfer from the data write register to memory. This bit is reset to zero when the CDA bit changes from 0 to 1.
11 - 5	CA6 - CA0	**Channel Address Bits.** These bits perform the same function as the external address bits when used to access various memory locations. The number (expressed in binary notation) on these bits refers to the input or output data stream channel that corresponds to the subsection of memory.
4 - 0	SA4 - SA0	**Stream Address Bits.** These bits perform the same function as the STA bits in the control register. The number (expressed in binary notation) on these bits refers to the input or output data stream which corresponds to the subsection of memory.

Table 13 -. Address Buffer (ABR) Register Bits

Read/Write Address: $0D_H$ for DWR register,
Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WR15	WR14	WR13	WR12	WR11	WR10	WR9	WR8	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0

Bit	Name	Description
15 - 0	WR15 - WR0	**Write Data Bits.** Data to be transferred to one of the internal memory locations.

.Table 14 - Data Write (DWR) Register Bits

Read Address:	$0E_H$ for DRR register,
Reset value:	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Bit	Name	Description
15 - 0	RD15 - RD0	**Read Data Bits.** Data transferred from one of the internal memory locations.

Table 15 -. Data Read (DRR) Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BV/C	BMC	DC	BSAB 3	BSAB 2	BSAB 1	BSAB 0	BCAB 6	BCAB 5	BCAB 4	BCAB 3	BCAB 2	BCAB 1	BCAB 0

Bit	Name	Description
15,14	Unused	Must be zero for normal operation.
13	B$\overline{V}$/C	**Variable /Constant Throughput Delay.** This bit is used to select either variable (low) or constant delay (high) modes on a per-channel basis for the local interface streams.
12	BMC	**Message Channel.** When 1, the backplane connection memory contents are output on the corresponding output channel and stream. Only the lower byte (bit 7 - bit 0) will be output to the backplane interface STio pins. When 0, the local data memory address of the switched STi input channel and stream is loaded into the backplane connection memory.
11	DC	**Directional Control.** This bit enables the STio pindrivers on a per-channel basis. When 1, the STio output driver functions normally. When 0, the STio output driver is in a high-impedance state.
10-7 (Note 1)	BSAB3-0	**Source Stream Address Bits.** The binary value is the number of the data stream for the source of the connection.
6-0 (Note 1)	BCAB6-0	**Source Channel Address Bits.** The binary value identifies the channel for the connection source.
Note 1: If bit 12 (BMC) of the corresponding backplane connection memory location is 1 (device in message mode), then these entire 8 bits (BSAB0, BCAB6 - BCAB0) are output on the output channel and stream associated with this location.		

Table 16 - Blackplane Connection Memory Bits

Data Rate	BSAB3 to BSAB0 Bits Used to Determine the Source Stream of the connection
2.048 Mb/s	STi0 to STi15
8.192 Mb/s	STi0 to STi3
2.048 Mb/s Sub-rate Switching	STi0 to STi12

Table 17 - BSAB Bits Programming for Different Local Interface mode

Data Rate	BCAB Bits Used to Determine the Source Channel of the Connection
2.048 Mb/s	BCAB4 to BCAB0 (32 channel/frame)
8.192 Mb/s	BCAB6 to BCAB0 (128 channel/frame)
2.048 Mb/s Sub-rate Switching	BCAB4 to BCAB0 (32 channel/frame) BCAB6 to BCAB0 (128 channel/frame)

Table 18 -. BCAB Bits Programming for Different Data Rates

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L/B	BV/C	BMC	OE	LSAB 4	LSAB 3	LSAB 2	LSAB 1	LSAB 0	LCAB 6	LCAB 5	LCAB 4	LCAB 3	LCAB 2	LCAB 1	LCAB 0

Bit	Name	Description
15	L/B	Local/Backplane Select When 1, the output channel of STo0-15 comes from STi0-15 (local) When 0, the output channel of STo0-15 comes from: STio0-31 (backplane, 2Mb/s mode) STio0-31 (backplane, 4Mb/s mode) STio0-15 (blackplane, 8Mb/s mode) STio0-23 (blackplane, HMVIP mode)
14	L$\overline{V}$/C	**Variable /Constant Throughput Delay.** This bit is used to select either variable (low) or constant delay (high) modes on a per-channel basis for the source streams.
13	LMC	**Message Channel.** When 1, the contents of the local connection memory are output on the corresponding output channel and stream. Only the lower byte (bit 7 - bit 0) will be output to the STo pins of the local interface. When 0, the backplane or local data memory address of the switched input channel and stream is loaded into the local connection memory.
12	OE	**Output Enable.** This bit enables the drivers of STo pins on a per-channel basis. When 1, the STo output driver functions normally. When 0, the STo output driver is in a high-impedance state.
11-7 (Note 1)	LSAB4-0	**Source Stream Address Bits.** The binary value identifies the data stream for the source of the connection.
6-0 (Note 1)	LCAB6-0	**Source Channel Address Bits.** The binary value identifies the channel for the source of the connection.
Note 1: If bit 12 (LMC) of the corresponding local connection memory location is 1 (device in message mode), then these entire 8 bits (LSAB0, LCAB6 - LCAB0) are output on the output channel and stream associated with this location.		

Table 19 -. Local Connection Memory Low Bits

Data Rate	LSAB3 to LSAB0 Bits Used to Determine the Source Stream of the Connection
2.048 Mb/s	STio0 to STio31 or STi0 to STi15
4.096 Mb/s	STio0 to STio31
8.192 Mb/s	STio0 to STio15 or STi0 to STi3
HMVIP	STio0 to STio23
2.048 Mb/s Sub-rate Switching	STi0 to STi12

Table 20 - LSAB Bits Programming for Different Local Interface Modes

Data Rate	LCAB Bits Used to Determine the Source Channel of the Connection
2.048 Mb/s	LCAB4 to LCAB0 (32 channel/frame)
4.096 Mb/s	LCAB5 to LCAB0 (64 channel/frame)
8.192 Mb/s	LCAB6 to LCAB0 (128 channel/frame)
HMVIP	LCAB4 to LCAB0 (32 channel/frame) LCAB6 to LCAB0 (128 channel/frame)
2.048 Mb/s Sub-rate Switching	LCAB4 to LCAB0 (32 channel/frame) LCAB6 to LCAB0 (128 channel/frame)

Table 21 - LCAB Bits Programming for Different Data Rates

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	LSR1	LSR0

Bit	Name	Description
15-2 (Note1)	Unused	Must be zero for normal operation.
1,0 (Note1)	LSR1, LSR0	Local Sub-rate Switching Bit When 11 Bit7-6 will be the output of the subrate switching stream When 10 Bit5-4 will be the output of the subrate switching stream When 01 Bit3-2 will be the output of the subrate switching stream When 00 Bit1-0 will be the output of the subrate switching stream

Note 1: If bit 12 (LMC) of the corresponding local connection memory location is 1 (device in message mode), then these entire 8 bits (Bit7-0) are output on the output channel and stream associated with this location.

Table 22 - Local Connection Memory High Bits

JTAG Support

The MT90863 JTAG interface conforms to the Boundary-Scan IEEE1149.1 standard. This standard specifies a design-for-testability technique called Boundary-Scan Test (BST). The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

Test Access Port (TAP)

The Test Access Port (TAP) accesses the MT90863 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)**
  TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- **Test Mode Select Input (TMS)**
  The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.

- **Test Data Input (TDI)**
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.

- **Test Data Output (TDO)**
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.

- **Test Reset ($\overline{\text{TRST}}$)**
  Reset the JTAG scan structure. This pin is internally pulled to VDD.

Instruction Register

The MT90863 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG Interface contains a two-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. These instructions are subsequently de-coded to achieve two basic functions: to select the test data register that may operate while the instruction is current; and, to define the serial test data register path that is used to shift data between TDI and DO during data register scan-ning.

Test Data Register

As specified in IEEE 1149.1, the MT90863 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register**
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90863 core logic.

- **The Bypass Register**
  The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO.

- **The Device Identification Register**
  The device identification register is a 32-bit register. The register contents are:

  MSB LSB

  0000 0000 1000 0110 0011 0001 0100 1011

  The LSB bit in the device identification register is the first bit clock out.

The MT90863 scan register contains 212 bits. Bit 0 in Table 23 Boundary Scan Register is the first bit clocked out. All tri-state enable bits are active high.

Device Pin	Boundary Scan Bit 0 to Bit 213		
	Tri-state Control	Output Scan Cell	Input Scan Cell
A0			0
A1			1
A2			2
A3			3
A4			4
A5			5
A6			6
A7			7
DS			8
R/$\overline{W}$			9
CS			10
D0	11	12	13
D1	14	15	16
D2	17	18	19
D3	20	21	22
D4	23	24	25
D5	26	27	28
D6	29	30	31
D7	32	33	34
D8	35	36	37
D9	38	39	40
D10	41	42	43
D11	44	45	46
D12	47	48	49
D13	50	51	52
D14	53	54	55
D15	56	57	58
DTA		59	
STi0			60
STi1			61
STi2			62
STi3			63
STi4			64
STi5			65
STi6			66
STi7			67
STi8			68
STi9			69
STi10			70
STi11			71
STi12			72
STi13			73
STi14			74
STi15			75
ODE			76

Table 23 - Boundary Scan Register Bits

Device Pin	Boundary Scan Bit 0 to Bit 213		
	Tri-state Control	Output Scan Cell	Input Scan Cell
STo0	77	78	
STo1	79	80	
STo2	81	82	
STo3	83	84	
STo4	85	86	
STo5	87	88	
STo6	89	90	
STo7	91	92	
STo8	93	94	
STo9	95	96	
STo10	97	98	
STo11	99	100	
STo12	101	102	
STo13	103	104	
STo14	105	106	
STo15	107	108	
C16i			109
F0i			110
C4i/C8i			111
F0o	112	113	
C4o	114	115	
STio0/FE0	116	117	118
STio1/FE1	119	120	121
STio2/FE2	122	123	124
STio3/FE3	125	126	127
STio4/FE4	128	129	130
STio5/FE5	131	132	133
STio6/FE6	134	135	136
STio7/FE7	137	138	139
STio8/FE8	140	141	142
STio9/FE9	143	144	145
STio10/FE10	146	147	148
STio11/FE11	149	150	151
STio12/FE12	152	153	154
STio13/FE13	155	156	157
STio14/FE14	158	159	160
STio15/FE15	161	162	163
STio16/FE16	164	165	166
STio17/FE17	167	168	169
STio18/FE18	170	171	172
STio19/FE19	173	174	175
STio20/FE20	176	177	178
STio21/FE21	179	180	181
STio22/FE22	182	183	184
STio23/FE23	185	186	187
STio24	188	189	190
STio25	191	192	193
STio26	194	195	196
STio27	197	198	199
STio28	200	201	202
STio29	203	204	205
STio30	206	207	208
STio31	209	210	211
RESET			212

Table 23 - Boundary Scan Register Bits

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.5	5.0	V
2	Input Voltage	V_I	-0.5	V_{DD} +0.5	V
3	Output Voltage	V_o	-0.5	V_{DD} +0.5	V
4	Package power dissipation	P_D		2	W
5	Storage temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	3.0		3.6	V	
3	Input High Voltage	V_{IH}	$0.7V_{DD}$		V_{DD}	V	
4	Input High Voltage on 5V Tolerant Inputs	V_{IH}			5.5	V	
5	Input Low Voltage	V_{IL}	V_{SS}		$0.3V_{DD}$	V	

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		45		mA	Output unloaded
2	INPUTS	Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3	INPUTS	Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	
4	INPUTS	Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			15 50	µA µA	$0 \leq < V \leq V_{DD}$ See Note 1
5	INPUTS	Input Pin Capacitance	C_I			10	pF	
6	OUTPUTS	Output High Voltage	V_{OH}	$0.8V_{DD}$			V	I_{OH} = 10mA
7	OUTPUTS	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10mA
8	OUTPUTS	High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD}$ See Note 1
9	OUTPUTS	Output Pin Capacitance	C_O			10	pF	

Note:
1. Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V)

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V	

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied

AC Electrical Characteristics - Frame Pulse and CLK

	Characteristic	Sym	Min	Typ	Max	Units	Notes
1	Frame pulse width	t_{FPW}		60		ns	ST-BUS mode
2	Frame Pulse Setup time before C16i falling	t_{FPS}		10		ns	
3	Frame Pulse Hold Time from C16i falling	t_{FPH}		10		ns	
4	C16i Period	t_{CP}		60		ns	
5	C16i Pulse Width High	t_{CH}		30		ns	
6	C16i Pulse Width Low	t_{CL}		30		ns	
7	Clock Rise/Fall Time	t_r, t_f		10		ns	ST-BUS, CT Bus or HMVIP mode
8	FPo Frame pulse output width	t_{FPOW}		244		ns	
9	FPo Frame Pulse output setup time before C4o falling	t_{FPOS}	10		150	ns	
10	FPo Frame Pulse output Hold Time from C4o falling	t_{FPOH}	20	10	150	ns	
11	C4o Period	t_{C4OP}		244		ns	
12	C4o Pulse Width High	t_{C40H}		122		ns	
13	C4o Pulse Width Low	t_{C40L}		122		ns	
14	CT frame pulse width	t_{CFPW}		122		ns	CT Bus mode
15	CT Frame Pulse Setup Time before C8i rising	t_{CFPS}	45		90	ns	
16	CT Frame Pulse Hold Time from C8i rising	t_{CFPH}	45		90	ns	
17	C8i Period	t_{HCP}		122		ns	
18	C8i Pulse Width High	t_{HCH}		61		ns	
19	C8i Pulse Width Low	t_{HCL}		61		ns	
20	HMVIP frame pulse width	t_{HFPW}		244		ns	HMVIP mode
21	Frame Pulse Setup Time before C4i falling	t_{HFPS}	50		150	ns	
22	Frame Pulse Hold Time from C4i falling	t_{HFPH}	50		150	ns	
23	C4i Period	t_{HCP}		244		ns	
24	C4i Pulse Width High	t_{HCH}		122		ns	
25	C4i Pulse Width Low	t_{HCL}		122		ns	
26	C4i/C8i Rise/Fall Time	t_{Hr}, t_{Hf}		10		ns	HMVIP or CT Bus mode
27	Delay between falling edge of C4i/ C8i and rising edge of C16i	t_{DIF}	-10		10	ns	
28	Delay between falling edge of C16i and falling edge of C4o	t_{DC4O}	-10		10	ns	

AC Electrical Characteristics - Serial Streams for Backplane and Local Interfaces

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	STio/STi Set-up Time	t_{SIS}		10		ns	
2	STio/STi Hold Time	t_{SIH}		20		ns	
3	STo Delay - Active to Active	t_{SOD}		40		ns	C_L=200pF
4	STo delay - Active to High-Z - High-Z to Active	t_{ZD}		40		ns	R_L=1K, C_L=200pF, See Note 1
5	Output Driver Enable (ODE) Delay	t_{ODE}		40		ns	

Note:

1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

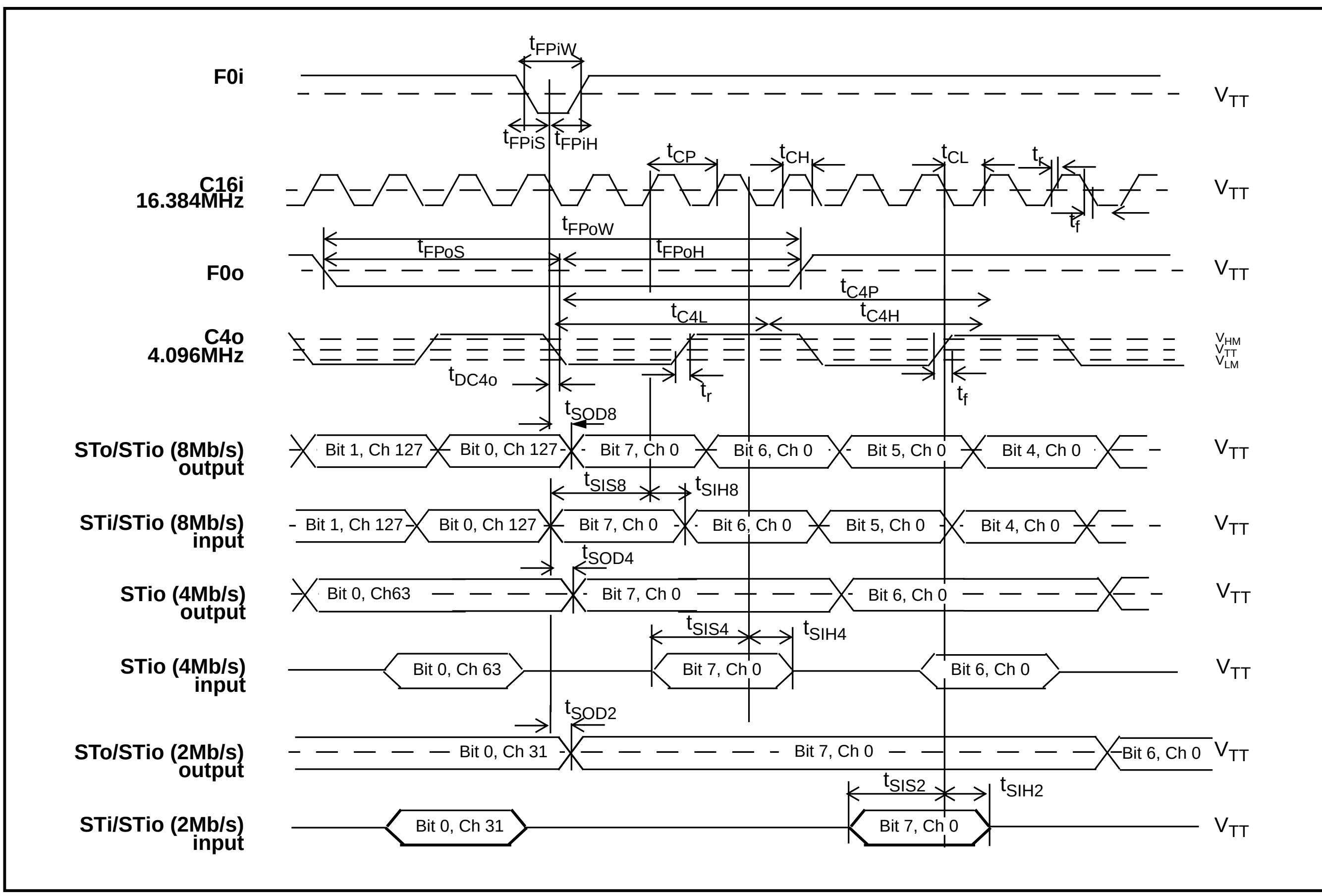


Figure 11 - ST-BUS Timing for Stream rate of 2.048, 4.096 or 8.192 Mb/s

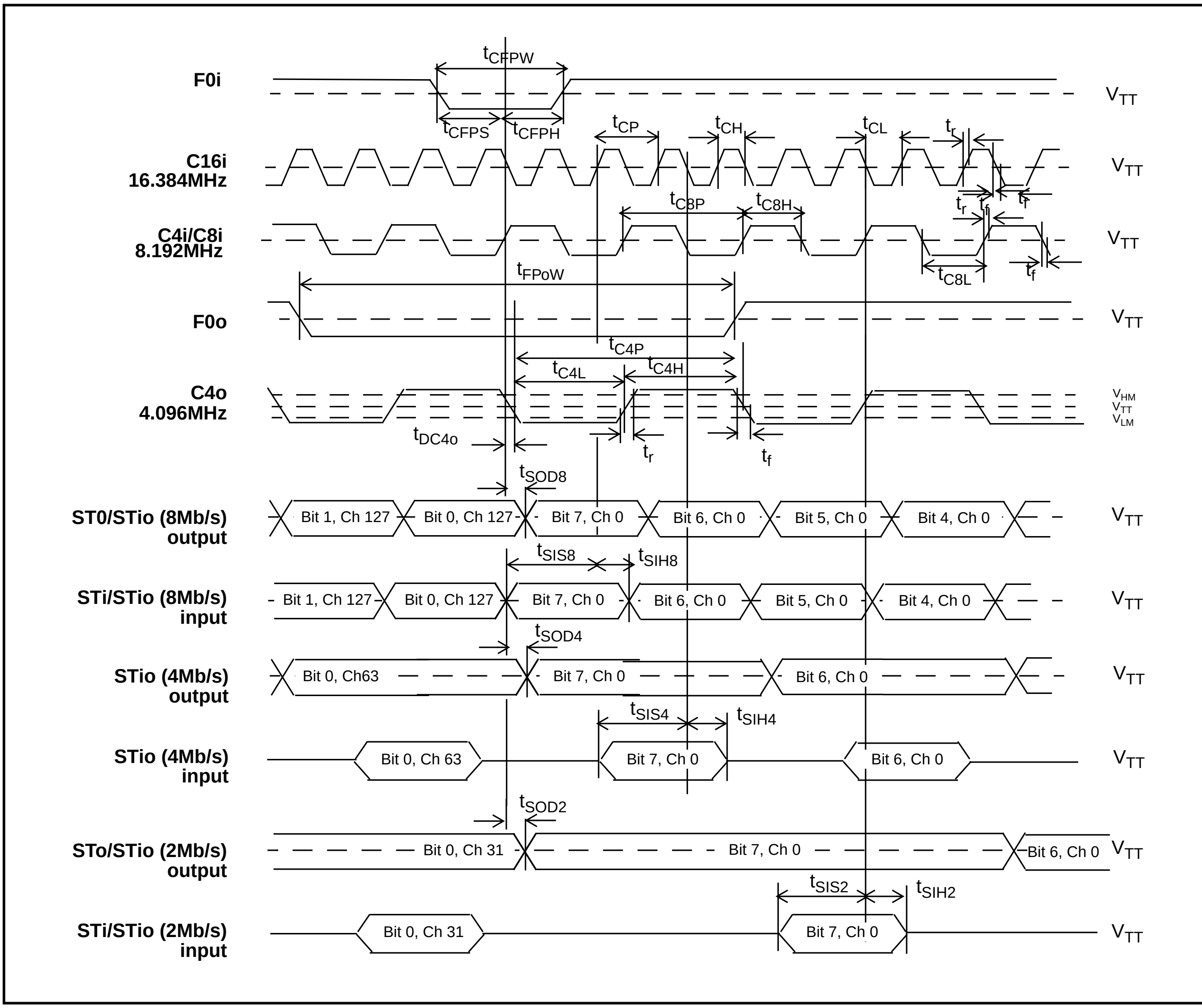


Figure 12 - CT Bus Timing for Stream rate of 2.048, 4.096 or 8.192 Mb/s

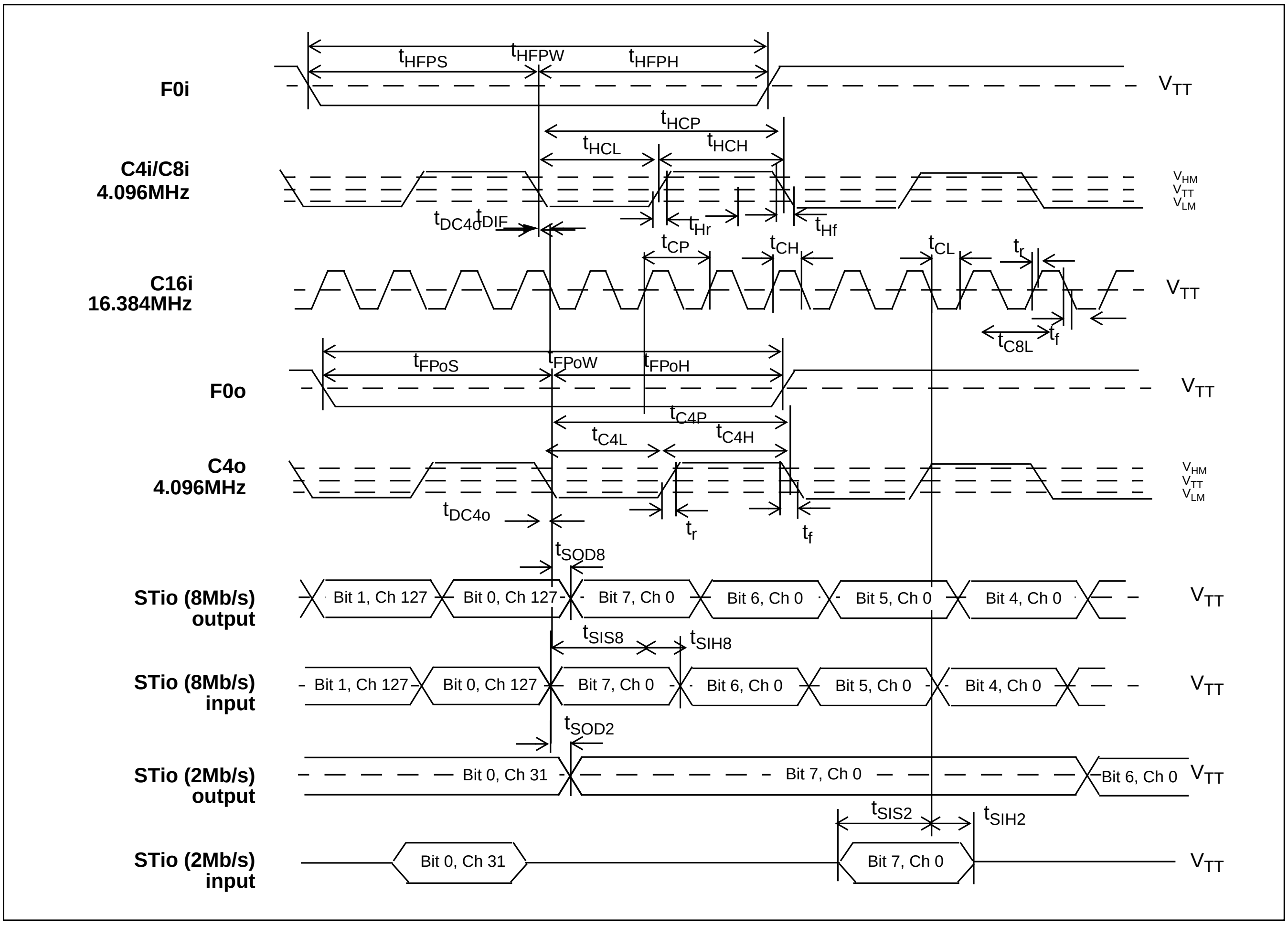


Figure 13 - HMVIP Bus Timing for Stream rate of 2.048 Mb/s or 8.192 Mb/s

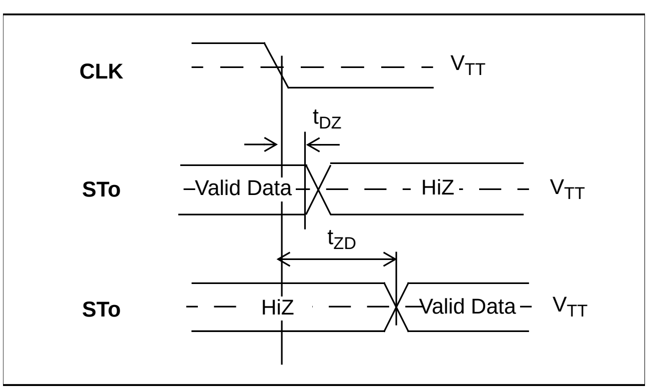


Figure 14 - Serial Output and External Control

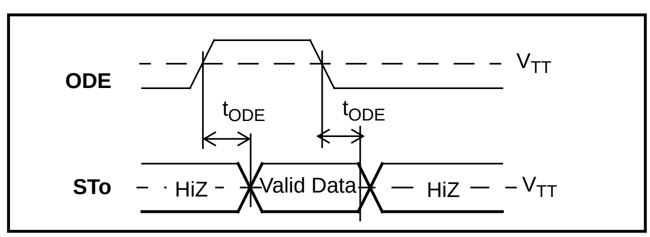


Figure 15 - Output Driver Enable (ODE)

AC Electrical Characteristics - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	CS setup from DS falling	t_{CSS}		0		ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}		10		ns	
3	Address setup from DS falling	t_{ADS}			5	ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}		10		ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}		10		ns	
6	Address hold after DS rising	t_{ADH}			6	ns	
7	Data setup from DTA low on read Reading registers Reading Memory	 t_{DDR_REG} t_{DDR_MEM}			 16 440	ns	C_L=50pF
8	Data hold on read	t_{DHR}			11	ns	C_L=50pF, R_L=1K Note 1
9	Data setup on write (fast write)	t_{DSW_REG}			2	ns	
10	Valid data delay on write (slow write)	t_{SWD}			150	ns	
11	Data hold on write	t_{DHW}	5			ns	
12	Acknowledgment delay: Reading/writing registers Reading/writing memory	 t_{AKD_REG} t_{AKD_MEM}			 40 470	ns	C_L=50pF
13	Acknowledgment hold time	t_{AKH}			17	ns	C_L=50pF, R_L=1K, Note

Note:
1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

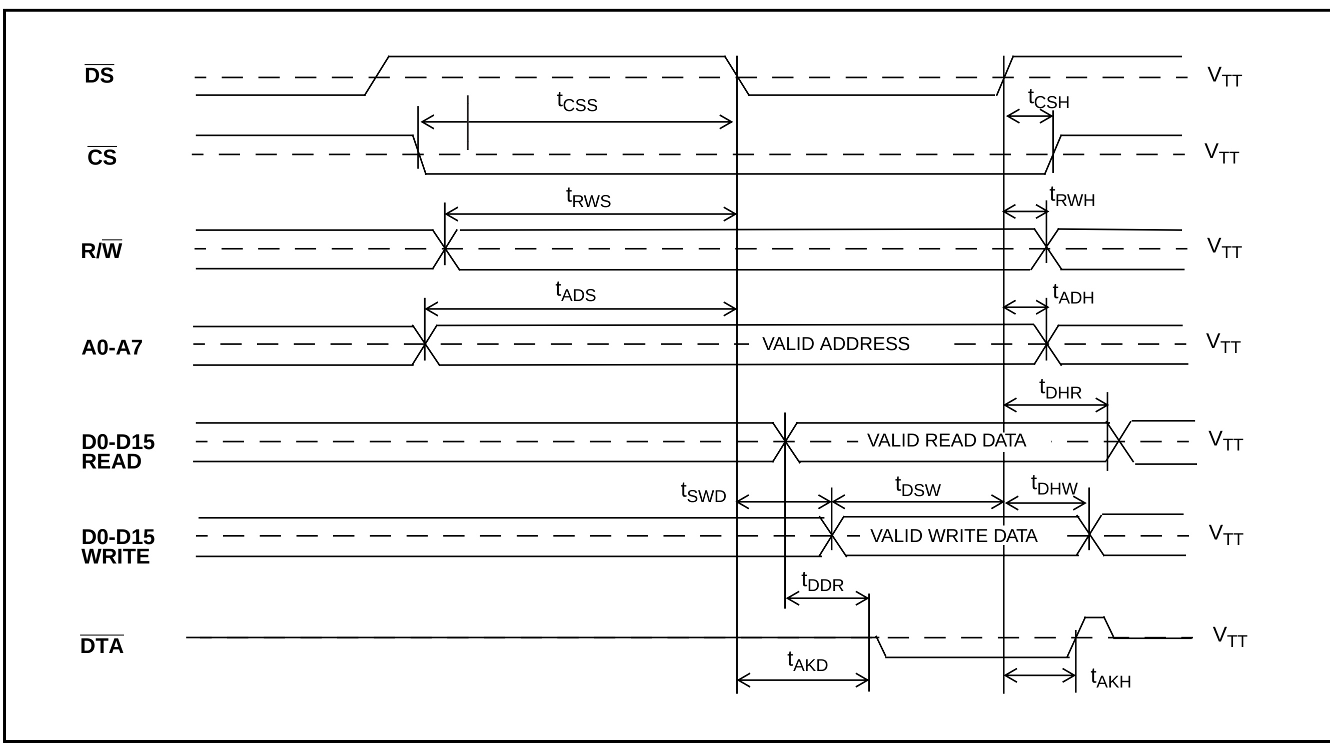
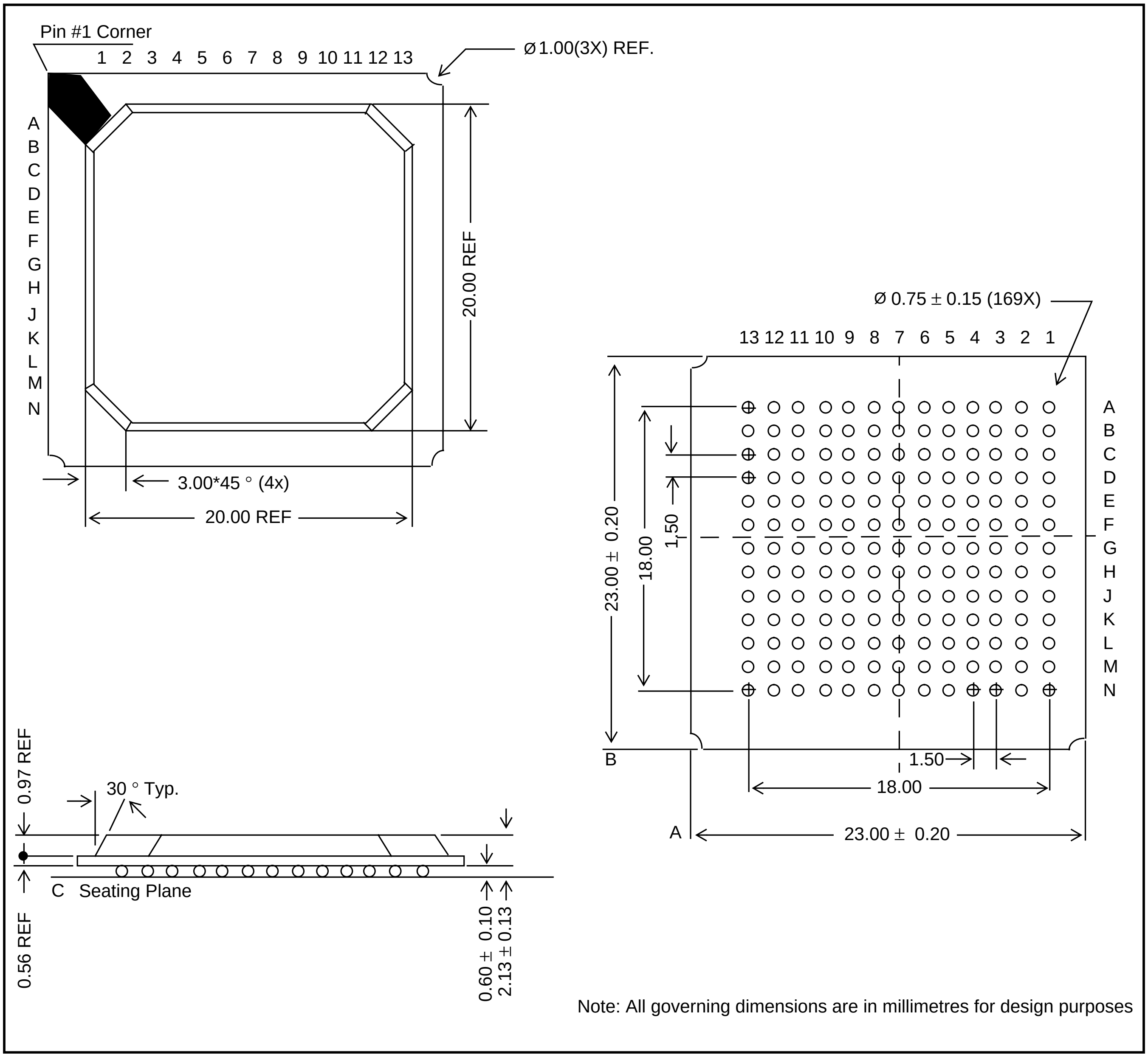
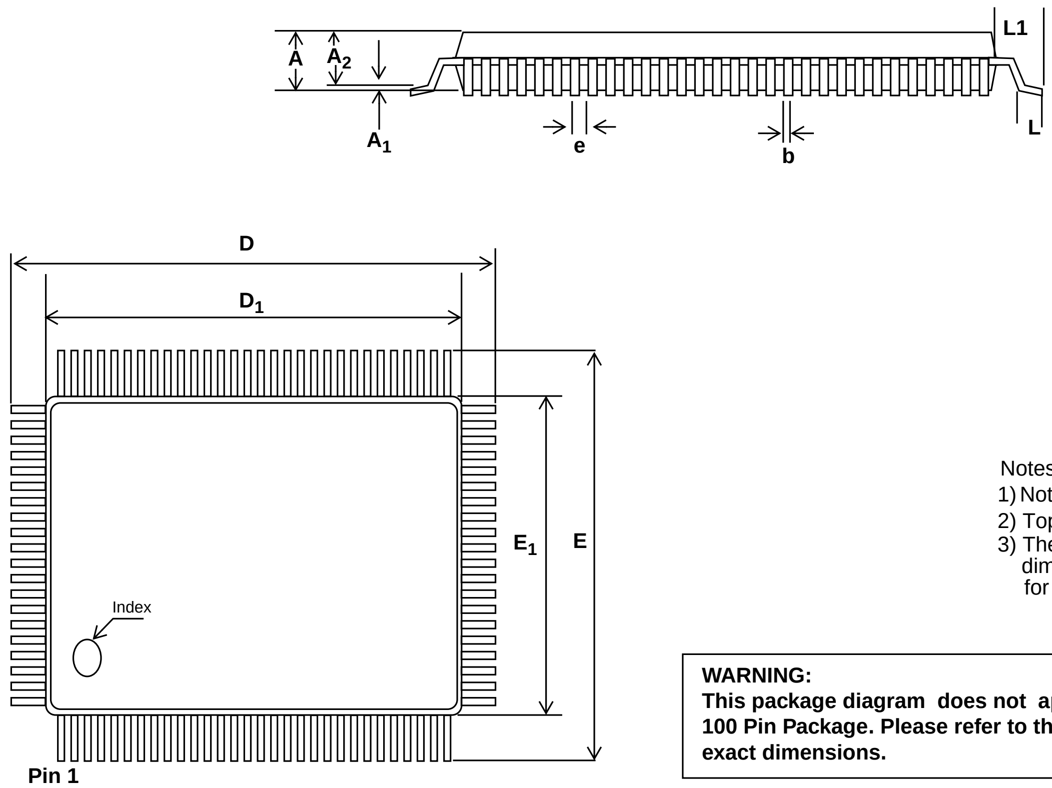


Figure 16 - Motorola Non-Multiplexed Bus Timing



Ball Gate Array

120-BGA	144-BGA	160-BGA
MT90823	MT90863	MT90826



Notes:
1) Not to scale
2) Top dimensions in inches
3) The governing controlling dimensions are in millimeters for design purposes ( )

WARNING:
This package diagram does not apply to the MT90810AK 100 Pin Package. Please refer to the data sheet for exact dimensions.

Metric Quad Flat Pack - L Suffix

Dim	44-Pin		64-Pin		100-Pin		128-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.096 (2.45)	-	0.134 (3.40)	-	0.134 (3.40)	-	0.154 (3.85)
A1	0.01 (0.25)	-	0.01 (0.25)	-	0.01 (0.25)	-	0.00	0.01 (0.25)
A2	0.077 (1.95)	0.083 (2.10)	0.1 (2.55)	0.12 (3.05)	0.1 (2.55)	0.12 (3.05)	0.125 (3.17)	0.144 (3.60)
b	0.01 (0.30)	0.018 (0.45)	0.013 (0.35)	0.02 (0.50)	0.009 (0.22)	0.015 (0.38)	0.019 (0.30)	0.018 (0.45)
D	0.547 BSC (13.90 BSC)		0.941 BSC (23.90 BSC)		0.941 BSC (23.90 BSC)		1.23 BSC (31.2 BSC)	
D_1	0.394 BSC (10.00 BSC)		0.787 BSC (20.00 BSC)		0.787 BSC (20.00 BSC)		1.102 BSC (28.00 BSC)	
E	0.547 BSC (13.90 BSC)		0.705 BSC (17.90 BSC)		0.705 BSC (17.90 BSC)		1.23 BSC (31.2 BSC)	
E_1	0.394 BSC (10.00 BSC)		0.551 BSC (14.00 BSC)		0.551 BSC (14.00 BSC)		1.102 BSC (28.00 BSC)	
e	0.031 BSC (0.80 BSC)		0.039 BSC (1.0 BSC)		0.256 BSC (0.65 BSC)		0.031 BSC (0.80 BSC)	
L	0.029 (0.73)	0.04 (1.03)	0.029 (0.73)	0.04 (1.03)	0.029 (0.73)	0.04 (1.03)	0.029 (0.73)	0.04 (1.03)
L1	0.077 REF (1.95 REF)		0.077 REF (1.95 REF)		0.077 REF (1.95 REF)		0.063 REF (1.60 REF)	

NOTE: Governing controlling dimensions in parenthesis ( ) are in millimeters.

Package Outlines

Dim	160-Pin		208-Pin		240-Pin	
	Min	Max	Min	Max	Min	Max
A	-	0.154 (3.92)		.161 (4.10)	-	0.161 (4.10)
A1		0.01 (0.25)	0.01 (0.25)	0.02 (0.50)	0.01 (0.25)	0.02 (0.50)
A2	0.125 (3.17)	0.144 (3.67)	.126 (3.20)	.142 (3.60)	0.126 (3.2)	0.142 (3.60)
b	0.009 (0.22)	0.015 (0.38)	.007 (0.17)	.011 (0.27)	0.007 (0.17)	0.010 (0.27)
D	1.23 BSC (31.2 BSC)		1.204 (30.6)		1.360 BSC (34.6 BSC)	
D_1	1.102 BSC (28.00 BSC)		1.102 (28.00)		1.26 BSC (32.00 BSC)	
E	1.23 BSC (31.2 BSC)		1.204 BSC (30.6 BSC)		1.360 BSC (34.6 BSC)	
E_1	1.102 BSC (28.00 BSC)		1.102 BSC (28.00 BSC)		1.26 BSC (32.00 BSC)	
e	0.025 BSC (0.65 BSC)		0.020 BSC (0.50 BSC)		0.0197 BSC (0.50 BSC)	
L	0.029 (0.73)	0.04 (1.03)	0.018 (0.45)	0.029 (0.75)	0.018 (0.45)	0.029 (0.75)
L1	0.063 REF (1.60 REF)		0.051 REF (1.30 REF)		0.051 REF (1.30 REF)	

NOTE: Governing controlling dimensions in parenthesis ( ) are in millimeters.

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