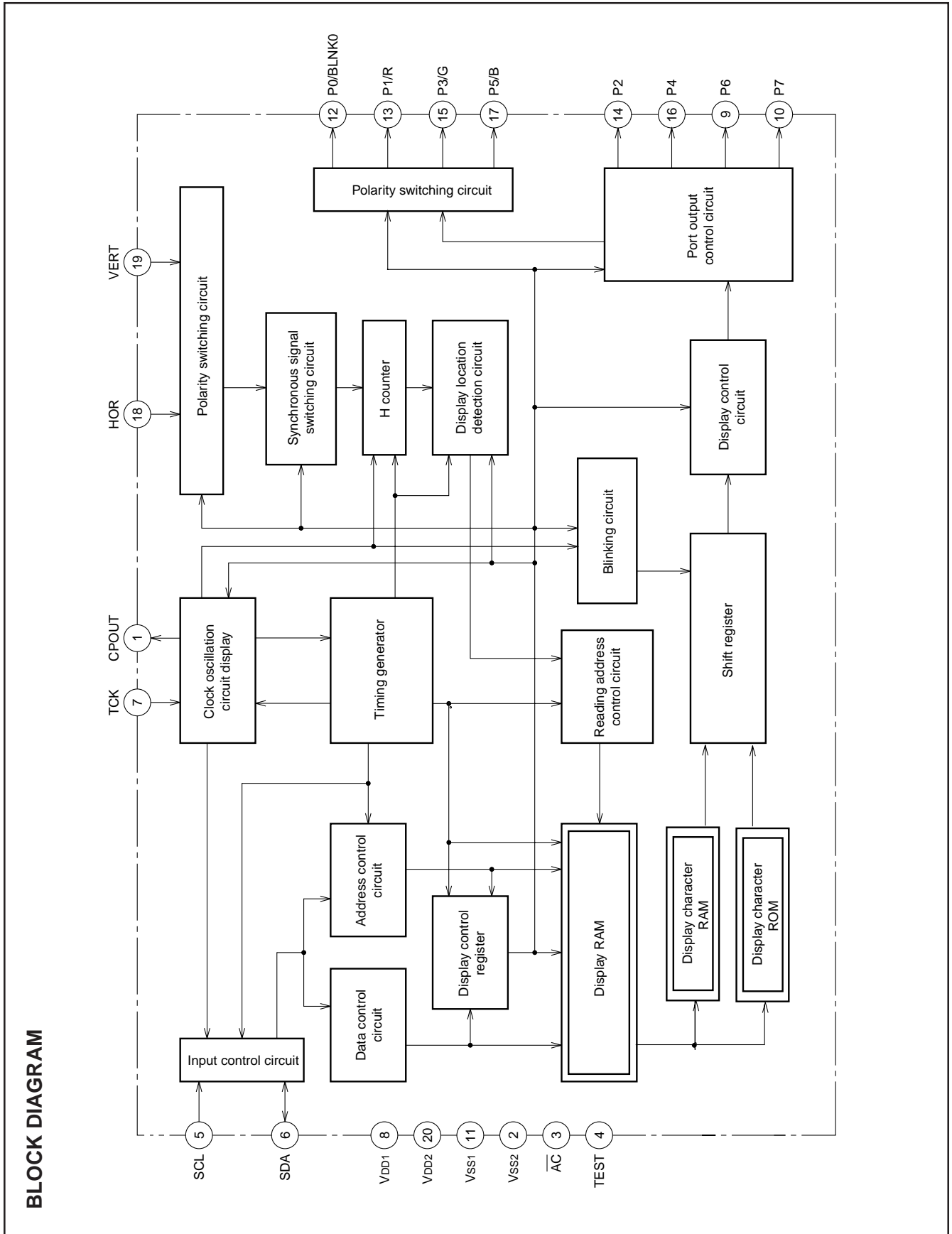


PIN DESCRIPTION

| Pin Number | Symbol | Pin name | Input/Output | Function |
|------------|-----------------|-------------------------------------|--------------|--|
| 1 | CPOUT | Filter output | Output | Filter output. Connect loop filter to this pin. |
| 2 | Vss2 | Earthing pin | – | Connect to GND. |
| 3 | \overline{AC} | Auto-clear input | Input | When "L", this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor. |
| 4 | TEST | Test input | Input | Test pin. Connect to +5V. |
| 5 | SCL | Clock input | Input | SDA pin serial data is taken in when SCL rises. Hysteresis input. |
| 6 | SDA | Data I/O | I/O | This is the pin for serial input of display control register and display RAM data. Also, this pin output acknowledge signal. Hysteresis input. Nch opendrain output. |
| 7 | TCK | External clock | Input | This is the pin for external clock input. |
| 8 | VDD1 | Power pin | – | Please connect to +5V with the power pin. |
| 9 | P6 | Port P6 output | Output | This is the output port. |
| 10 | P7 | Port P7 output | Output | This is the output port. |
| 11 | Vss1 | Earthing pin | – | Please connect to GND using circuit earthing pin. |
| 12 | P0/BLNK0 | Port P0 output | Output | This pin can be toggled between port pin output and BLNK0 signal output. |
| 13 | P1/R | Port P1 output | Output | This pin can be toggled between port pin output and R signal output. |
| 14 | P2 | Port P2 output | Output | This is the output port. |
| 15 | P3/G | Port P3 output | Output | This pin can be toggled between port pin output and G signal output. |
| 16 | P4 | Port P4 output | Output | This is the output port. |
| 17 | P5/B | Port P5 output | Output | This pin can be toggled between port pin output and B signal output. |
| 18 | HOR | Horizontal synchronous signal input | Input | This pin inputs the horizontal synchronous signal. Hysteresis input. |
| 19 | VERT | Vertical synchronous signal input | Input | This pin inputs the vertical synchronous signal. Hysteresis input. |
| 20 | VDD2 | Power pin | – | Please connect to +5V with the power pin. |



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 129₁₆ are assigned to the display control registers and address 200₁₆ to 2F1₁₆ are assigned to the RAM characters. The internal circuit is reset and all display control registers (address 120₁₆ to 129₁₆) are set to "0" when the AC pin level is "L". And

then, RAM is not erased and be undefined. For detail, see "DATA INPUT EXAMPLE". Memory constitution is shown in Figure 1 to 9.

| Addresses | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|-------------------|-----|---------------------|--------|--------|----------|-----------------|--------|--------|----------------|--------|-------|-------|-------|-------|-------|-------|
| 000 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 001 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| ⋮ | ⋮ | Background coloring | | | Blinking | Character color | | | Character code | | | | | | | |
| 11E ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 11F ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 120 ₁₆ | 0 | SPACE2 | SPACE1 | SPACE0 | TEST10 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 |
| 121 ₁₆ | 0 | EXCK1 | EXCK0 | RSEL1 | RSEL0 | DIVS2 | DIVS1 | DIVS0 | PTC7 | PTC6 | PTC5 | PTC4 | PTC3 | PTC2 | PTC1 | PTC0 |
| 122 ₁₆ | 0 | TEST17 | TEST16 | TEST15 | TEST14 | TEST13 | TEST12 | TEST11 | PTD7 | PTD6 | PTD5 | PTD4 | PTD3 | PTD2 | PTD1 | PTD0 |
| 123 ₁₆ | 0 | TEST3 | TEST2 | TEST1 | TEST0 | HP10 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| 124 ₁₆ | 0 | TEST20 | RBLK0 | TEST19 | TEST18 | VP10 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |
| 125 ₁₆ | 0 | TEST23 | TEST22 | TEST21 | DSP11 | DSP10 | DSP9 | DSP8 | DSP7 | DSP6 | DSP5 | DSP4 | DSP3 | DSP2 | DSP1 | DSP0 |
| 126 ₁₆ | 0 | TEST24 | VSZ1H1 | VSZ1H0 | VSZ1L1 | VSZ1L0 | V1SZ1 | V1SZ0 | LIN9 | LIN8 | LIN7 | LIN6 | LIN5 | LIN4 | LIN3 | LIN2 |
| 127 ₁₆ | 0 | TEST25 | VSZ2H1 | VSZ2H0 | VSZ2L1 | VSZ2L0 | V18SZ1 | V18SZ0 | LIN17 | LIN16 | LIN15 | LIN14 | LIN13 | LIN12 | LIN11 | LIN10 |
| 128 ₁₆ | 0 | TEST29 | HSZ21 | HSZ20 | HSZ11 | HSZ10 | BETA14 | TEST28 | TEST27 | TEST26 | FB | FG | FR | RB | RG | RR |
| 129 ₁₆ | 0 | TEST30 | BLINK2 | BLINK1 | BLINK0 | DSPON | STOP | RAMERS | SYAD | BLK1 | BLK0 | POLH | POLV | VMASK | B/F | BCOL |

Fig.1 Memory constitution (Display RAM, Display Control register)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|-----------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 200 ₁₆ | 0 | BS | GS | RS | FR000B | FR000A | FR0009 | FR0008 | FR0007 | FR0009 | FR0005 | FR0004 | FR0003 | FR0002 | FR0001 | FR0000 |
| 201 ₁₆ | 0 | BS | GS | RS | FR001B | FR001A | FR0019 | FR0018 | FR0017 | FR0019 | FR0015 | FR0014 | FR0013 | FR0012 | FR0011 | FR0010 |
| 202 ₁₆ | 0 | BS | GS | RS | FR002B | FR002A | FR0029 | FR0028 | FR0027 | FR0026 | FR0025 | FR0024 | FR0023 | FR0022 | FR0021 | FR0020 |
| 203 ₁₆ | 0 | BS | GS | RS | FR003B | FR003A | FR0039 | FR0038 | FR0037 | FR0036 | FR0035 | FR0034 | FR0033 | FR0032 | FR0031 | FR0030 |
| 204 ₁₆ | 0 | BS | GS | RS | FR004B | FR004A | FR0049 | FR0048 | FR0047 | FR0046 | FR0045 | FR0044 | FR0043 | FR0042 | FR0041 | FR0040 |
| 205 ₁₆ | 0 | BS | GS | RS | FR005B | FR005A | FR0059 | FR0058 | FR0057 | FR0056 | FR0055 | FR0054 | FR0053 | FR0052 | FR0051 | FR0050 |
| 206 ₁₆ | 0 | BS | GS | RS | FR006B | FR006A | FR0069 | FR0068 | FR0067 | FR0066 | FR0065 | FR0064 | FR0063 | FR0062 | FR0061 | FR0060 |
| 207 ₁₆ | 0 | BS | GS | RS | FR007B | FR007A | FR0079 | FR0078 | FR0077 | FR0076 | FR0075 | FR0074 | FR0073 | FR0072 | FR0071 | FR0070 |
| 208 ₁₆ | 0 | BS | GS | RS | FR008B | FR008A | FR0089 | FR0088 | FR0087 | FR0086 | FR0085 | FR0084 | FR0083 | FR0082 | FR0081 | FR0080 |
| 209 ₁₆ | 0 | BS | GS | RS | FR009B | FR009A | FR0099 | FR0098 | FR0097 | FR0096 | FR0095 | FR0094 | FR0093 | FR0092 | FR0091 | FR0090 |
| 20A ₁₆ | 0 | BS | GS | RS | FR00AB | FR00AA | FR00A9 | FR00A8 | FR00A7 | FR00A6 | FR00A5 | FR00A4 | FR00A3 | FR00A2 | FR00A1 | FR00A0 |
| 20B ₁₆ | 0 | BS | GS | RS | FR00BB | FR00BA | FR00B9 | FR00B8 | FR00B7 | FR00B6 | FR00B5 | FR00B4 | FR00B3 | FR00B2 | FR00B1 | FR00B0 |
| 20C ₁₆ | 0 | BS | GS | RS | FR00CB | FR00CA | FR00C9 | FR00C8 | FR00C7 | FR00C6 | FR00C5 | FR00C4 | FR00C3 | FR00C2 | FR00C1 | FR00C0 |
| 20D ₁₆ | 0 | BS | GS | RS | FR00DB | FR00DA | FR00D9 | FR00D8 | FR00D7 | FR00D6 | FR00D5 | FR00D4 | FR00D3 | FR00D2 | FR00D1 | FR00D0 |
| 20E ₁₆ | 0 | BS | GS | RS | FR00EB | FR00EA | FR00E9 | FR00E8 | FR00E7 | FR00E6 | FR00E5 | FR00E4 | FR00E3 | FR00E2 | FR00E1 | FR00E0 |
| 20F ₁₆ | 0 | BS | GS | RS | FR00FB | FR00FA | FR00F9 | FR00F8 | FR00F7 | FR00F6 | FR00F5 | FR00F4 | FR00F3 | FR00F2 | FR00F1 | FR00F0 |
| 210 ₁₆ | 0 | BS | GS | RS | FR010B | FR010A | FR0109 | FR0108 | FR0107 | FR0106 | FR0105 | FR0104 | FR0103 | FR0102 | FR0101 | FR0100 |
| 211 ₁₆ | 0 | BS | GS | RS | FR011B | FR011A | FR0119 | FR0118 | FR0117 | FR0116 | FR0115 | FR0114 | FR0113 | FR0112 | FR0111 | FR0110 |
| 212 ₁₆ ⋮ 21F ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.2 Memory constitution (RAM character 0)

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 220 ₁₆ | 0 | BS | GS | RS | FR100B | FR100A | FR1009 | FR1008 | FR1007 | FR1006 | FR1005 | FR1004 | FR1003 | FR1002 | FR1001 | FR1000 |
| 221 ₁₆ ⋮ 230 ₁₆ | RAM character 1 data | | | | | | | | | | | | | | | |
| 231 ₁₆ | 0 | BS | GS | RS | FR111B | FR111A | FR1119 | FR1118 | FR1117 | FR1116 | FR1115 | FR1114 | FR1113 | FR1112 | FR1111 | FR1110 |
| 232 ₁₆ ⋮ 23F ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.3 Memory constitution (RAM character 1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 240 ₁₆ | 0 | BS | GS | RS | FR200B | FR200A | FR2009 | FR2008 | FR2007 | FR2006 | FR2005 | FR2004 | FR2003 | FR2002 | FR2001 | FR2000 |
| 241 ₁₆ ⋮ 250 ₁₆ | RAM character 2 data | | | | | | | | | | | | | | | |
| 251 ₁₆ | 0 | BS | GS | RS | FR211B | FR211A | FR2119 | FR2118 | FR2117 | FR2116 | FR2115 | FR2114 | FR2113 | FR2112 | FR2111 | FR2110 |
| 252 ₁₆ ⋮ 25F ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.4 Memory constitution (RAM character 2)

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 260 ₁₆ | 0 | BS | GS | RS | FR300B | FR300A | FR3009 | FR3008 | FR3007 | FR3006 | FR3005 | FR3004 | FR3003 | FR3002 | FR3001 | FR3000 |
| 261 ₁₆ ⋮ 270 ₁₆ | RAM character 3 data | | | | | | | | | | | | | | | |
| 271 ₁₆ | 0 | BS | GS | RS | FR311B | FR311A | FR3119 | FR3118 | FR3117 | FR3116 | FR3115 | FR3114 | FR3113 | FR3112 | FR3111 | FR3110 |
| 272 ₁₆ ⋮ 27F ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.5 Memory constitution (RAM character 3)

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 280 ₁₆ | 0 | BS | GS | RS | FR400B | FR400A | FR4009 | FR4008 | FR4007 | FR4006 | FR4005 | FR4004 | FR4003 | FR4002 | FR4001 | FR4000 |
| 281 ₁₆ ⋮ 290 ₁₆ | RAM character 4 data | | | | | | | | | | | | | | | |
| 291 ₁₆ | 0 | BS | GS | RS | FR411B | FR411A | FR4119 | FR4118 | FR4117 | FR4116 | FR4115 | FR4114 | FR4113 | FR4112 | FR4111 | FR4510 |
| 292 ₁₆ ⋮ 29F ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.6 Memory constitution (RAM character 4)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | D00 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 2A0 ₁₆ | 0 | BS | GS | RS | FR500B | FR500A | FR5009 | FR5008 | FR5007 | FR5006 | FR5005 | FR5004 | FR5003 | FR5002 | FR5001 | FR5000 |
| 2A1 ₁₆ ⋮ 2B0 ₁₆ | RAM character 5 data | | | | | | | | | | | | | | | |
| 2B1 ₁₆ | 0 | BS | GS | RS | FR511B | FR511A | FR5119 | FR5118 | FR5117 | FR5116 | FR5115 | FR5114 | FR5113 | FR5112 | FR5111 | FR5110 |
| 2B2 ₁₆ ⋮ 2BF ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.7 Memory constitution (RAM character 5)

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 2C0 ₁₆ | 0 | BS | GS | RS | FR600B | FR600A | FR6009 | FR6008 | FR6007 | FR6006 | FR6005 | FR6004 | FR6003 | FR6002 | FR6001 | FR6000 |
| 2C1 ₁₆ ⋮ 2D0 ₁₆ | RAM character 6 data | | | | | | | | | | | | | | | |
| 2D1 ₁₆ | 0 | BS | GS | RS | FR611B | FR611A | FR6119 | FR6118 | FR6117 | FR6116 | FR6115 | FR6114 | FR6113 | FR6112 | FR6111 | FR6110 |
| 2D2 ₁₆ ⋮ 2DF ₁₆ | Can not be used | | | | | | | | | | | | | | | |

Fig.8 Memory constitution (RAM character 6)

| Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|----------------------|-----|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 2E0 ₁₆ | 0 | BS | GS | RS | FR700B | FR700A | FR7009 | FR7008 | FR7007 | FR7006 | FR7005 | FR7004 | FR7003 | FR7002 | FR7001 | FR7000 |
| 2E1 ₁₆ ⋮ 2F0 ₁₆ | RAM character 7 data | | | | | | | | | | | | | | | |
| 2F1 ₁₆ | 0 | BS | GS | RS | FR711B | FR711A | FR7119 | FR7118 | FR7117 | FR7116 | FR7115 | FR7114 | FR7113 | FR7112 | FR7111 | FR7110 |

Fig.9 Memory constitution (RAM character 7)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM . The screen constitution is shown in Figure 10.

| Row Line | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1 | 00016 | 00116 | 00216 | 00316 | 00416 | 00516 | 00616 | 00716 | 00816 | 00916 | 00A16 | 00B16 | 00C16 | 00D16 | 00E16 | 00F16 | 01016 | 01116 | 01216 | 01316 | 01416 | 01516 | 01616 | 01716 |
| 2 | 01816 | 01916 | 01A16 | 01B16 | 01C16 | 01D16 | 01E16 | 01F16 | 02016 | 02116 | 02216 | 02316 | 02416 | 02516 | 02616 | 02716 | 02816 | 02916 | 02A16 | 02B16 | 02C16 | 02D16 | 02E16 | 02F16 |
| 3 | 03016 | 03116 | 03216 | 03316 | 03416 | 03516 | 03616 | 03716 | 03816 | 03916 | 03A16 | 03B16 | 03C16 | 03D16 | 03E16 | 03F16 | 04016 | 04116 | 04216 | 04316 | 04416 | 04516 | 04616 | 04716 |
| 4 | 04816 | 04916 | 04A16 | 04B16 | 04C16 | 04D16 | 04E16 | 04F16 | 05016 | 05116 | 05216 | 05316 | 05416 | 05516 | 05616 | 05716 | 05816 | 05916 | 05A16 | 05B16 | 05C16 | 05D16 | 05E16 | 05F16 |
| 5 | 06016 | 06116 | 06216 | 06316 | 06416 | 06516 | 06616 | 06716 | 06816 | 06916 | 06A16 | 06B16 | 06C16 | 06D16 | 06E16 | 06F16 | 07016 | 07116 | 07216 | 07316 | 07416 | 07516 | 07616 | 07716 |
| 6 | 07816 | 07916 | 07A16 | 07B16 | 07C16 | 07D16 | 07E16 | 07F16 | 08016 | 08116 | 08216 | 08316 | 08416 | 08516 | 08616 | 08716 | 08816 | 08916 | 08A16 | 08B16 | 08C16 | 08D16 | 08E16 | 08F16 |
| 7 | 09016 | 09116 | 09216 | 09316 | 09416 | 09516 | 09616 | 09716 | 09816 | 09916 | 09A16 | 09B16 | 09C16 | 09D16 | 09E16 | 09F16 | 0A016 | 0A116 | 0A216 | 0A316 | 0A416 | 0A516 | 0A616 | 0A716 |
| 8 | 0A816 | 0A916 | 0AA16 | 0AB16 | 0AC16 | 0AD16 | 0AE16 | 0AF16 | 0B016 | 0B116 | 0B216 | 0B316 | 0B416 | 0B516 | 0B616 | 0B716 | 0B816 | 0B916 | 0BA16 | 0BB16 | 0BC16 | 0BD16 | 0BE16 | 0BF16 |
| 9 | 0C016 | 0C116 | 0C216 | 0C316 | 0C416 | 0C516 | 0C616 | 0C716 | 0C816 | 0C916 | 0CA16 | 0CB16 | 0CC16 | 0CD16 | 0CE16 | 0CF16 | 0D016 | 0D116 | 0D216 | 0D316 | 0D416 | 0D516 | 0D616 | 0D716 |
| 10 | 0D816 | 0D916 | 0DA16 | 0DB16 | 0DC16 | 0DD16 | 0DE16 | 0DF16 | 0E016 | 0E116 | 0E216 | 0E316 | 0E416 | 0E516 | 0E616 | 0E716 | 0E816 | 0E916 | 0EA16 | 0EB16 | 0EC16 | 0ED16 | 0EE16 | 0EF16 |
| 11 | 0F016 | 0F116 | 0F216 | 0F316 | 0F416 | 0F516 | 0F616 | 0F716 | 0F816 | 0F916 | 0FA16 | 0FB16 | 0FC16 | 0FD16 | 0FE16 | 0FF16 | 10016 | 10116 | 10216 | 10316 | 10416 | 10516 | 10616 | 10716 |
| 12 | 10816 | 10916 | 10A16 | 10B16 | 10C16 | 10D16 | 10E16 | 10F16 | 11016 | 11116 | 11216 | 11316 | 11416 | 11516 | 11616 | 11716 | 11816 | 11916 | 11A16 | 11B16 | 11C16 | 11D16 | 11E16 | 11F16 |

* The hexadecimal numbers in the boxes show the display RAM address.

Fig.10 Screen constitution

RAM Character CONSTITUTION

The dot lines and dot rows of the character RAM are determined from each address and bit of the character RAM . The RAM character constitution is shown in Figure 11.

| Dot Dot | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 1 | FRn00B | FRn00A | FRn009 | FRn008 | FRn007 | FRn006 | FRn005 | FRn004 | FRn003 | FRn002 | FRn001 | FRn000 |
| 2 | FRn01B | FRn01A | FRn019 | FRn018 | FRn017 | FRn016 | FRn015 | FRn014 | FRn013 | FRn012 | FRn011 | FRn010 |
| 3 | FRn02B | FRn02A | FRn029 | FRn028 | FRn027 | FRn026 | FRn025 | FRn024 | FRn023 | FRn022 | FRn021 | FRn020 |
| 4 | FRn03B | FRn03A | FRn039 | FRn038 | FRn037 | FRn036 | FRn035 | FRn034 | FRn033 | FRn032 | FRn031 | FRn030 |
| 5 | FRn04B | FRn04A | FRn049 | FRn048 | FRn047 | FRn046 | FRn045 | FRn044 | FRn043 | FRn042 | FRn041 | FRn040 |
| 6 | FRn05B | FRn05A | FRn059 | FRn058 | FRn057 | FRn056 | FRn055 | FRn054 | FRn053 | FRn052 | FRn051 | FRn050 |
| 7 | FRn06B | FRn06A | FRn069 | FRn068 | FRn067 | FRn066 | FRn065 | FRn064 | FRn063 | FRn062 | FRn061 | FRn060 |
| 8 | FRn07B | FRn07A | FRn079 | FRn078 | FRn077 | FRn076 | FRn075 | FRn074 | FRn073 | FRn072 | FRn071 | FRn070 |
| 9 | FRn08B | FRn08A | FRn089 | FRn088 | FRn087 | FRn086 | FRn085 | FRn084 | FRn083 | FRn082 | FRn081 | FRn080 |
| 10 | FRn09B | FRn09A | FRn099 | FRn098 | FRn097 | FRn096 | FRn095 | FRn094 | FRn093 | FRn092 | FRn091 | FRn090 |
| 11 | FRn0AB | FRn0AA | FRn0A9 | FRn0A8 | FRn0A7 | FRn0A6 | FRn0A5 | FRn0A4 | FRn0A3 | FRn0A2 | FRn0A1 | FRn0A0 |
| 12 | FRn0BB | FRn0BA | FRn0B9 | FRn0B8 | FRn0B7 | FRn0B6 | FRn0B5 | FRn0B4 | FRn0B3 | FRn0B2 | FRn0B1 | FRn0B0 |
| 13 | FRn0CB | FRn0CA | FRn0C9 | FRn0C8 | FRn0C7 | FRn0C6 | FRn0C5 | FRn0C4 | FRn0C3 | FRn0C2 | FRn0C1 | FRn0C0 |
| 14 | FRn0DB | FRn0DA | FRn0D9 | FRn0D8 | FRn0D7 | FRn0D6 | FRn0D5 | FRn0D4 | FRn0D3 | FRn0D2 | FRn0D1 | FRn0D0 |
| 15 | FRn0EB | FRn0EA | FRn0E9 | FRn0E8 | FRn0E7 | FRn0E6 | FRn0E5 | FRn0E4 | FRn0E3 | FRn0E2 | FRn0E1 | FRn0E0 |
| 16 | FRn0FB | FRn0FA | FRn0F9 | FRn0F8 | FRn0F7 | FRn0F6 | FRn0F5 | FRn0F4 | FRn0F3 | FRn0F2 | FRn0F1 | FRn0F0 |
| 17 | FRn10B | FRn10A | FRn109 | FRn108 | FRn107 | FRn106 | FRn105 | FRn104 | FRn103 | FRn102 | FRn101 | FRn100 |
| 18 | FRn11B | FRn11A | FRn119 | FRn118 | FRn117 | FRn116 | FRn115 | FRn114 | FRn113 | FRn112 | FRn111 | FRn110 |

* The number in the boxes show the bit address of the RAM character : n. ("n" is RAM number : 0 to 7)

Fig.11 RAM character constitution

Note. When the RAM character is used, it is necessary to clear all areas of the RAM character first.

DISPLAY RAM

Address 000₁₆ to 11F₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----|----------|----------|---|--|----|--------------------|--------------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|---|---|-----------------|---|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | C0 | 0 | Set the displayed ROM character code. *RAM character is selected using the 8 bits from C7 to C0. When C7 to C0=(11111110 ₂) is set. And, RAM character code is set to R, G and B. | Set display character | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | C1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | C2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | C3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | C4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | C5 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | C6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | C7 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | R | 0 | <table border="1"> <thead> <tr> <th>B</th> <th>G</th> <th>R</th> <th>RAM character code</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>RAM character 0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>RAM character 1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>RAM character 2</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>RAM character 3</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>RAM character 4</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>RAM character 5</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>RAM character 6</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>RAM character 7</td></tr> </tbody> </table> | B | G | R | RAM character code | 0 | 0 | 0 | RAM character 0 | 0 | 0 | 1 | RAM character 1 | 0 | 1 | 0 | RAM character 2 | 0 | 1 | 1 | RAM character 3 | 1 | 0 | 0 | RAM character 4 | 1 | 0 | 1 | RAM character 5 | 1 | 1 | 0 | RAM character 6 | 1 | 1 | 1 | RAM character 7 | Set character color (character unit) * When set C7 to C0=(11111110 ₂), can be set RAM character code. |
| | | B | | G | R | RAM character code | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | RAM character 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | RAM character 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | RAM character 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | RAM character 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | RAM character 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | RAM character 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | RAM character 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | | RAM character 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | G | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | B | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | BLINK | 0 | Do not blink. | Set blinking See register BLINK2 to BLINK0 (address 129 ₁₆) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | BR | 0 | <table border="1"> <thead> <tr> <th>BB</th> <th>BG</th> <th>BR</th> <th>Color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table> | BB | BG | BR | Color | 0 | 0 | 0 | Black | 0 | 0 | 1 | Red | 0 | 1 | 0 | Green | 0 | 1 | 1 | Yellow | 1 | 0 | 0 | Blue | 1 | 0 | 1 | Magenta | 1 | 1 | 0 | Cyan | 1 | 1 | 1 | White | Set character background color. (character unit) * When set C7 to C0=(11111110 ₂) and register RBLK0 (address 124 ₁₆)= "1", set coloring prohibition color. Moreover, when the blink is set, the parts other than the color set by this register are blinks. See DISPLAY FORM 2. |
| | | BB | | BG | BR | Color | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | Black | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | Red | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | Green | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | Yellow | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | Blue | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | Magenta | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | Cyan | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | | White | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | BG | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | BB | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note. The display RAM is undefined state at the AC pin.

REGISTERS DESCRIPTION

(1) Address 120₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----|----------|----------|--|---|---|--|---|---|---|---|----|---|---|---|----------------|---|---|---|---------------|---|---|---|---------------|---|---|---|---------------|---|---|---|---------------|---|---|---|---------------|---|---|---|---------|---|---|---|------------|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | DIV0 | 0 | Set division value (multiply value) of horizontal oscillation frequency. | Set display frequency by division value (multiply value) setting. For details, see REGISTER SUPPLEMENTARY DESCRIPTION (1). Also, set the display frequency range by registers DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1(address 121 ₁₆) in accordance with the display frequency. Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | DIV1 | 0 | $N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1 : division value (multiply value) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | DIV2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | DIV3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | DIV4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | DIV5 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | DIV6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | DIV7 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | DIV8 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | DIV9 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | DIV10 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | TEST10 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | SPACE0 | 0 | <table border="1"> <thead> <tr> <th colspan="3">SPACE</th> <th>Number of Lines and Space <(S) represents space></th> </tr> </thead> <tbody> <tr> <td>2</td> <td>1</td> <td>0</td> <td>12</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1 (S) 10 (S) 1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1 (S) 8 (S) 1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 (S) 8 (S) 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>3 (S) 6 (S) 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4 (S) 4 (S) 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>5 (S) 2 (S) 5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 (S) 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>6 (S)(S) 6</td> </tr> </tbody> </table> (S) represents one line worth of space | SPACE | | | Number of Lines and Space <(S) represents space> | 2 | 1 | 0 | 12 | 0 | 0 | 0 | 1 (S) 10 (S) 1 | 0 | 0 | 1 | 1 (S) 8 (S) 1 | 0 | 1 | 0 | 2 (S) 8 (S) 2 | 0 | 1 | 1 | 3 (S) 6 (S) 3 | 1 | 0 | 0 | 4 (S) 4 (S) 4 | 1 | 0 | 1 | 5 (S) 2 (S) 5 | 1 | 1 | 0 | 6 (S) 6 | 1 | 1 | 1 | 6 (S)(S) 6 |
| | | SPACE | | | Number of Lines and Space <(S) represents space> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | 0 | | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | 1 (S) 10 (S) 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | 1 (S) 8 (S) 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | 2 (S) 8 (S) 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | 3 (S) 6 (S) 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | 4 (S) 4 (S) 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | 5 (S) 2 (S) 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | 6 (S) 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 6 (S)(S) 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | SPACE1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | SPACE2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note. The mark 0 around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 121₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|----|----------|---------------------------------------|---|------------------------------|---------------------|---------------------|---|---|---------------------------------------|---|---|----------------------|---|---|------------|---|---|---------------------------------------|---|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | PTC0 | 0 | P0 output (port P0). | P0 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | BLNK0 output. | | | | | | | | | | | | | | | | |
| 1 | PTC1 | 0 | P1 output (port P1). | P1 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | R signal output. | | | | | | | | | | | | | | | | |
| 2 | PTC2 | 0 | P2 output (port P2). | P2 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| 3 | PTC3 | 0 | P3 output (port P3). | P3 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | G signal output. | | | | | | | | | | | | | | | | |
| 4 | PTC4 | 0 | P4 output (port P4). | P4 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| 5 | PTC5 | 0 | P5 output (port P5). | P5 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | B signal output. | | | | | | | | | | | | | | | | |
| 6 | PTC6 | 0 | P6 output (port P6). | P6 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| 7 | PTC7 | 0 | P7 output (port P7). | P7 pin output control. | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| 8 | DIVS0 | 0 | For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2). | Set display frequency range. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 9 | DIVS1 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| A | DIVS2 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| B | RSEL0 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| C | RSEL1 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| D | EXCK0 | 0 | <table border="1"> <thead> <tr> <th>EXCK1</th> <th>EXCK0</th> <th>Display clock input</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>External synchronous (external clock)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal synchronous</td> </tr> <tr> <td>1</td> <td>0</td> <td>Do not set</td> </tr> <tr> <td>1</td> <td>1</td> <td>External synchronous (internal clock)</td> </tr> </tbody> </table> | EXCK1 | EXCK0 | Display clock input | 0 | 0 | External synchronous (external clock) | 0 | 1 | Internal synchronous | 1 | 0 | Do not set | 1 | 1 | External synchronous (internal clock) | Display clock setting See REGISTER SUPPLEMENTARY DESCRIPTION (1) |
| | | EXCK1 | | EXCK0 | Display clock input | | | | | | | | | | | | | | |
| 0 | 0 | External synchronous (external clock) | | | | | | | | | | | | | | | | | |
| 0 | 1 | Internal synchronous | | | | | | | | | | | | | | | | | |
| 1 | 0 | Do not set | | | | | | | | | | | | | | | | | |
| 1 | 1 | External synchronous (internal clock) | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| E | EXCK1 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |

Note. The mark 0 around the status value means the reset status by the "L" level is input to \overline{AC} pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122₁₆

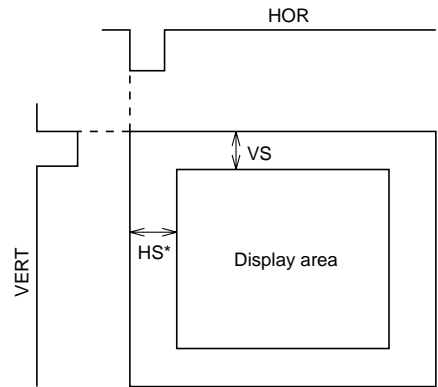
| DA | Register | Contents | | Remarks |
|----|----------|----------|---|----------------------|
| | | Status | Function | |
| 0 | PTD0 | 0 | "L" output or negative polarity output (BLNK0 output). | P0 pin data control. |
| | | 1 | "H" output or positive polarity output (BLNK0 output). | |
| 1 | PTD1 | 0 | "L" output or negative polarity output (R signal output). | P1 pin data control. |
| | | 1 | "H" output or positive polarity output (R signal output). | |
| 2 | PTD2 | 0 | "L" output. | P2 pin data control. |
| | | 1 | "H" output. | |
| 3 | PTD3 | 0 | "L" output or negative polarity output (G signal output). | P3 pin data control. |
| | | 1 | "H" output or positive polarity output (G signal output). | |
| 4 | PTD4 | 0 | "L" output. | P4 pin data control. |
| | | 1 | "H" output. | |
| 5 | PTD5 | 0 | "L" output or negative polarity output (B signal output). | P5 pin data control. |
| | | 1 | "H" output or positive polarity output (B signal output). | |
| 6 | PTD6 | 0 | "L" output. | P6 pin data control. |
| | | 1 | "H" output. | |
| 7 | PTD7 | 0 | "L" output. | P7 pin data control. |
| | | 1 | "H" output. | |
| 8 | TEST11 | 0 | Can not be used. | |
| | | 1 | It should be fixed to "1". | |
| 9 | TEST12 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| A | TEST13 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| B | TEST14 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| C | TEST15 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST16 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| E | TEST17 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

Note. The mark 0 around the status value means the reset status by the "L" level is input to \overline{AC} pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 123₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|-------|----------|----------|---|------------|----|---|---|---|-------|---|---|---|---|---|----|----|------------|----|--|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | HP0 | 0 | If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^{10} 2^n NP_{n+m} \right)$ T: Period of display frequency 2007 settings are possible. m : offset value differ for the setting of the register EXCK0 and EXCK1. It shown below. <table border="1" style="margin: 10px auto;"> <tr> <td>EXCK1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>EXCK0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>m</td> <td>13</td> <td>13</td> <td>Do not set</td> <td>19</td> </tr> </table> | EXCK1 | 0 | 0 | 1 | 1 | EXCK0 | 0 | 1 | 0 | 1 | m | 13 | 13 | Do not set | 19 | Horizontal display start location is specified using the 11 bits from HP10 to HP0. HP10 to HP0 = (000000000002) and (000001001112) setting is forbidden. |
| | | EXCK1 | | 0 | 0 | 1 | 1 | | | | | | | | | | | | |
| EXCK0 | 0 | 1 | | 0 | 1 | | | | | | | | | | | | | | |
| m | 13 | 13 | | Do not set | 19 | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | HP1 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 2 | HP2 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 3 | HP3 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 4 | HP4 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 5 | HP5 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 6 | HP6 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 7 | HP7 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 8 | HP8 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 9 | HP9 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| A | HP10 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| B | TEST0 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| C | TEST1 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| D | TEST2 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |
| E | TEST3 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |



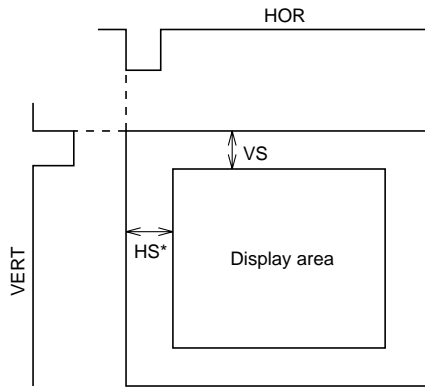
HS*(shown left) shows horizontal display start location this is register B/F (address 129₁₆) = "0" is set.

Note. The mark 0 around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124₁₆

| DA | Register | Contents | | Remarks |
|----|----------|----------|---|---|
| | | Status | Function | |
| 0 | VP0 | 0 | If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{10} 2^n VP_n$ | The vertical start location is specified using the 11 bits from VP10 to VP0. VP10 to VP0 = (00000000000 ₂) setting is forbidden. HS*(shown left) shows horizontal display start location this is register B/F (address 129 ₁₆) = "0" is set. |
| | | 1 | | |
| 1 | VP1 | 0 | T: Cycle with the horizontal synchronizing pulse 2047 settings are possible. | |
| | | 1 | | |
| 2 | VP2 | 0 | | |
| | | 1 | | |
| 3 | VP3 | 0 | | |
| | | 1 | | |
| 4 | VP4 | 0 | | |
| | | 1 | | |
| 5 | VP5 | 0 | | |
| | | 1 | | |
| 6 | VP6 | 0 | | |
| | | 1 | | |
| 7 | VP7 | 0 | | |
| | | 1 | | |
| 8 | VP8 | 0 | | |
| | | 1 | | |
| 9 | VP9 | 0 | | |
| | | 1 | | |
| A | VP10 | 0 | | |
| | | 1 | | |
| B | TEST18 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| C | TEST19 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | RBLK0 | 0 | Matrix-outline size. | Sets the blanking mode of RAM character. See DISPLAY FORM 2. |
| | | 1 | Character size. (Note 2) | |
| E | TEST20 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |



Note1. The mark 0 around the status value means the reset status by the "L" level is input to AC pin.
 Note2. The part of the appointed color by BB, BG and BB of the display RAM changes that the blanking is "OFF".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 125₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | | |
|----|----------|-----------------------|--|-----------------------------------|----------|----------|----------|---|---|-----------------------|----------------|---|---|-----------|--------|---|---|--------|----------------|---|---|----------------|-----------|----------------------------------|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | |
| 0 | DSP0 | 0 | The display modes of display screen inside n+1 line by DSPn (n=0~11) | Sets the display mode of line 1. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 1 | DSP1 | 0 | The display mode decided by the combination with registers BLK1 and BLK0 (address 129 ₁₆). Settings are given below. | Sets the display mode of line 2. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 2 | DSP2 | 0 | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>DSPn="0"</th> <th>DSPn="1"</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Matrix-outline border</td> <td>Matrix-outline</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character</td> <td>Border</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border</td> <td>Matrix-outline</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline</td> <td>Character</td> </tr> </tbody> </table> | BLK1 | BLK0 | DSPn="0" | DSPn="1" | 0 | 0 | Matrix-outline border | Matrix-outline | 0 | 1 | Character | Border | 1 | 0 | Border | Matrix-outline | 1 | 1 | Matrix-outline | Character | Sets the display mode of line 3. |
| | | BLK1 | | BLK0 | DSPn="0" | DSPn="1" | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Matrix-outline border | Matrix-outline | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Character | Border | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Border | Matrix-outline | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Matrix-outline | Character | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | DSP3 | 0 | (At register BCOL="0") | Sets the display mode of line 4. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 4 | DSP4 | 0 | For detail, see DISPLAY FORM 1 (1). | Sets the display mode of line 5. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 5 | DSP5 | 0 | | Sets the display mode of line 6. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 6 | DSP6 | 0 | | Sets the display mode of line 7. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 7 | DSP7 | 0 | | Sets the display mode of line 8. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 8 | DSP8 | 0 | | Sets the display mode of line 9. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 9 | DSP9 | 0 | | Sets the display mode of line 10. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| A | DSP10 | 0 | | Sets the display mode of line 11. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| B | DSP11 | 0 | | Sets the display mode of line 12. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| C | TEST21 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |
| D | TEST22 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |
| E | TEST23 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |

Note. The mark 0 around the status value means the reset status by the "L" level is input to \overline{AC} pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|------------------|----------------------------|----------------------------|--|--|-------------------------|-------------------------|----------|----------------------------|----------------------------|------------------|----------------------------|----------------------------|--|---|--------|---|---|--------|--|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | LIN2 | 0 | The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17). | Character size setting in the vertical direction for the 2nd line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 1 | LIN3 | 0 | Dot size can be selected between 2 types for each dot line. | Character size setting in the vertical direction for the 3rd line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 2 | LIN4 | 0 | For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another. | Character size setting in the vertical direction for the 4th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 3 | LIN5 | 0 | <table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th></th> <th>LINn = "0"</th> <th>LINn = "1"</th> </tr> </thead> <tbody> <tr> <td>1st line</td> <td>Refer to VSZ1L0 and VSZ1L1</td> <td>Refer to VSZ1H0 and VSZ1H1</td> </tr> <tr> <td>2nd to 12th line</td> <td>Refer to VSZ2L0 and VSZ2L1</td> <td>Refer to VSZ2H0 and VSZ2H1</td> </tr> </tbody> </table> | | LINn = "0" | LINn = "1" | 1st line | Refer to VSZ1L0 and VSZ1L1 | Refer to VSZ1H0 and VSZ1H1 | 2nd to 12th line | Refer to VSZ2L0 and VSZ2L1 | Refer to VSZ2H0 and VSZ2H1 | Character size setting in the vertical direction for the 5th line. | | | | | | |
| | | | | LINn = "0" | LINn = "1" | | | | | | | | | | | | | | |
| 1st line | Refer to VSZ1L0 and VSZ1L1 | Refer to VSZ1H0 and VSZ1H1 | | | | | | | | | | | | | | | | | |
| 2nd to 12th line | Refer to VSZ2L0 and VSZ2L1 | Refer to VSZ2H0 and VSZ2H1 | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| 4 | LIN6 | 0 | | Character size setting in the vertical direction for the 6th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 5 | LIN7 | 0 | | Character size setting in the vertical direction for the 7th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 6 | LIN8 | 0 | | Character size setting in the vertical direction for the 8th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 7 | LIN9 | 0 | | Character size setting in the vertical direction for the 9th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 8 | V1SZ0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction for the 1st line. (display monitor 1 to 12 line) | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 9 | V1SZ1 | 0 | <table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>V1SZ1</th> <th>V1SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | V1SZ1 | V1SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | V1SZ1 | | V1SZ0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| A | VSZ1L0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 to LIN17 (address 126 ₁₆ , 127 ₁₆). | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| B | VSZ1L1 | 0 | <table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1L1 | VSZ1L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ1L1 | | VSZ1L0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| C | VSZ1H0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 to LIN17 (address 126 ₁₆ , 127 ₁₆). | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| D | VSZ1H1 | 0 | <table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>VSZ1H1</th> <th>VSZ1H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ1H1 | VSZ1H0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ1H1 | | VSZ1H0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| E | TEST24 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |

Note. The mark ○ around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|------------------|----------------------------|----------------------------|--|--|-------------------------|-------------------------|----------|----------------------------|----------------------------|------------------|----------------------------|----------------------------|---|---|--------|---|---|--------|--|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | LIN10 | 0 | The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17). | Character size setting in the vertical direction for the 10th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 1 | LIN11 | 0 | Dot size can be selected between 2 types for each dot line. | Character size setting in the vertical direction for the 11th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 2 | LIN12 | 0 | For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another. | Character size setting in the vertical direction for the 12th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 3 | LIN13 | 0 | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>LINn = "0"</th> <th>LINn = "1"</th> </tr> </thead> <tbody> <tr> <td>1st line</td> <td>Refer to VSZ1L0 and VSZ1L1</td> <td>Refer to VSZ1H0 and VSZ1H1</td> </tr> <tr> <td>2nd to 12th line</td> <td>Refer to VSZ2L0 and VSZ2L1</td> <td>Refer to VSZ2H0 and VSZ2H1</td> </tr> </tbody> </table> | | LINn = "0" | LINn = "1" | 1st line | Refer to VSZ1L0 and VSZ1L1 | Refer to VSZ1H0 and VSZ1H1 | 2nd to 12th line | Refer to VSZ2L0 and VSZ2L1 | Refer to VSZ2H0 and VSZ2H1 | Character size setting in the vertical direction for the 13th line. | | | | | | |
| | | | | LINn = "0" | LINn = "1" | | | | | | | | | | | | | | |
| 1st line | Refer to VSZ1L0 and VSZ1L1 | Refer to VSZ1H0 and VSZ1H1 | | | | | | | | | | | | | | | | | |
| 2nd to 12th line | Refer to VSZ2L0 and VSZ2L1 | Refer to VSZ2H0 and VSZ2H1 | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| 4 | LIN14 | 0 | | Character size setting in the vertical direction for the 14th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 5 | LIN15 | 0 | | Character size setting in the vertical direction for the 15th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 6 | LIN16 | 0 | | Character size setting in the vertical direction for the 16th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 7 | LIN17 | 0 | | Character size setting in the vertical direction for the 17th line. | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 8 | V18SZ0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction for the 18th line. (display monitor 1 to 12 line) | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 9 | V18SZ1 | 0 | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | V18SZ1 | V18SZ0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | V18SZ1 | | V18SZ0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| A | VSZ2L0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor for 2 to 12 line) at "0" state in register LIN2 to LIN17 (address 126 ₁₆ , 127 ₁₆). | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| B | VSZ2L1 | 0 | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2L1 | VSZ2L0 | Vertical direction size | 0 | 0 | 1H/dot | 0 | 1 | 2H/dot | 1 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ2L1 | | VSZ2L0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| C | VSZ2H0 | 0 | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor for 2 to 12 line) at "1" state in register LIN2 to LIN17 (address 126 ₁₆ , 127 ₁₆). | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| D | VSZ2H1 | 0 | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>0</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table> | VSZ2H1 | VSZ2H0 | Vertical direction size | 0 | 0 | 1H/dot | 1 | 1 | 2H/dot | 0 | 0 | 3H/dot | 1 | 1 | 4H/dot | |
| | | VSZ2H1 | | VSZ2H0 | Vertical direction size | | | | | | | | | | | | | | |
| 0 | 0 | 1H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 2H/dot | | | | | | | | | | | | | | | | | |
| 0 | 0 | 3H/dot | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4H/dot | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| E | TEST25 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | | | Can not be used. | | | | | | | | | | | | | | |

Note. The mark ○ around the status value means the reset status by the "L" level is input to \overline{AC} pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128₁₆

| DA | Register | Contents | | | | Remarks | |
|----|----------|----------|--------------------------------------|-------|---------------------------|---|--|
| | | Status | Function | | | | |
| 0 | RR | ⓪ | | | | Sets the raster color of all blankings. | |
| | | 1 | RB | RG | RR | | Color |
| 1 | RG | ⓪ | 0 | 0 | 0 | | Black |
| | | 1 | 0 | 0 | 1 | | Red |
| 2 | RB | ⓪ | 0 | 1 | 0 | | Green |
| | | 1 | 0 | 1 | 1 | | Yellow |
| 3 | FR | ⓪ | 1 | 0 | 0 | | Blue |
| | | 1 | 1 | 0 | 1 | | Magenta |
| 4 | FG | ⓪ | 1 | 1 | 0 | | Cyan |
| | | 1 | 1 | 1 | 1 | | White |
| 5 | FB | ⓪ | | | | Set the blanking color of the Border size, or the shadow size. | |
| | | 1 | FB | FG | FR | | Color |
| 6 | TEST26 | ⓪ | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 7 | TEST27 | ⓪ | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 8 | TEST28 | ⓪ | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| 9 | BETA14 | ⓪ | Matrix-outline display (12 X 18 dot) | | | | |
| | | 1 | Matrix-outline display (14 X 18 dot) | | | | |
| A | HSZ10 | ⓪ | | | | Charcter size setting in the horizontal direction for the first line. T: Display frequency cycle | |
| | | 1 | HSZ11 | HSZ10 | Horizontal direction size | | |
| B | HSZ11 | ⓪ | 0 | 0 | 1T/dot | | |
| | | 1 | 0 | 1 | 2T/dot | | |
| C | HSZ20 | ⓪ | 1 | 0 | 3T/dot | | |
| | | 1 | 1 | 1 | 4T/dot | | |
| D | HSZ21 | ⓪ | | | | | Charcter size setting in the horizontal direction for the 2nd line to 12th line. T: Display frequency cycle |
| | | 1 | HSZ21 | HSZ20 | Horizontal direction size | | |
| E | TEST29 | ⓪ | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |

Note. The mark ⓪ around the status value means the reset status by the "L" level is input to \overline{AC} pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(10) Address 129₁₆

| DA | Register | Contents | | Remarks | | | | | | | | | | | | | | | |
|--------|--|---------------------|--|--|--------|---------------|---|---|---------------------|---|---|----------------|---|---|-------------|---|---|---------------------|---|
| | | Status | Function | | | | | | | | | | | | | | | | |
| 0 | BCOL | 0 | Blanking of BLK0, BLK1 | Sets all raster blanking | | | | | | | | | | | | | | | |
| | | 1 | All raster blanking | | | | | | | | | | | | | | | | |
| 1 | B \bar{F} | 0 | Synchronize with the leading edge of horizontal synchronization. | Synchronize with the front porch or back porch of the horizontal synchronization signal. | | | | | | | | | | | | | | | |
| | | 1 | Synchronize with the trailing edge of horizontal synchronization. | | | | | | | | | | | | | | | | |
| 2 | VMASK | 0 | Do not mask by VERT input signal | Set mask at phase comparison operating. | | | | | | | | | | | | | | | |
| | | 1 | Mask by VERT input signal | | | | | | | | | | | | | | | | |
| 3 | POLV | 0 | VERT pin is negative polarity | Set VERT pin polarity. | | | | | | | | | | | | | | | |
| | | 1 | VERT pin is positive polarity | | | | | | | | | | | | | | | | |
| 4 | POLH | 0 | HOR pin is negative polarity | Set HOR pin polarity. | | | | | | | | | | | | | | | |
| | | 1 | HOR pin is positive polarity | | | | | | | | | | | | | | | | |
| 5 | BLK0 | 0 | <table border="1"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>Blanking mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Matrix-outline size</td> </tr> </tbody> </table> | BLK1 | BLK0 | Blanking mode | 0 | 0 | Matrix-outline size | 0 | 1 | Character size | 1 | 0 | Border size | 1 | 1 | Matrix-outline size | Set blanking mode. See DISPLAY FORM 1 (1). |
| BLK1 | BLK0 | Blanking mode | | | | | | | | | | | | | | | | | |
| 0 | 0 | Matrix-outline size | | | | | | | | | | | | | | | | | |
| 0 | 1 | Character size | | | | | | | | | | | | | | | | | |
| 1 | 0 | Border size | | | | | | | | | | | | | | | | | |
| 1 | 1 | Matrix-outline size | | | | | | | | | | | | | | | | | |
| 1 | (When DSPn (address 125 ₁₆) = "0") | | | | | | | | | | | | | | | | | | |
| 6 | BLK1 | 0 | (When DSPn (address 125 ₁₆) = "0") | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| 7 | SYAD | 0 | Border display of character | See DISPLAY FORM 1 (2). | | | | | | | | | | | | | | | |
| | | 1 | Shadow display of character | | | | | | | | | | | | | | | | |
| 8 | RAMERS | 0 | RAM not erased | When register RAMERS is set to "1," do not stop the display clock. There is no need to reset because there is no register for this bit. Refer to REGISTER SUPPLEMENTARY DESCRIPTION. | | | | | | | | | | | | | | | |
| | | 1 | RAM erased | | | | | | | | | | | | | | | | |
| 9 | STOP | 0 | Oscillation of clock for display | | | | | | | | | | | | | | | | |
| | | 1 | Stop the oscillation of clock for display | | | | | | | | | | | | | | | | |
| A | DSPON | 0 | Display OFF | | | | | | | | | | | | | | | | |
| | | 1 | Display ON | | | | | | | | | | | | | | | | |
| B | BLINK0 | 0 | <table border="1"> <thead> <tr> <th>BLINK1</th> <th>BLINK0</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Blinking OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table> | BLINK1 | BLINK0 | Duty | 0 | 0 | Blinking OFF | 0 | 1 | 25% | 1 | 0 | 50% | 1 | 1 | 75% | Set blinking duty ratio. |
| BLINK1 | BLINK0 | Duty | | | | | | | | | | | | | | | | | |
| 0 | 0 | Blinking OFF | | | | | | | | | | | | | | | | | |
| 0 | 1 | 25% | | | | | | | | | | | | | | | | | |
| 1 | 0 | 50% | | | | | | | | | | | | | | | | | |
| 1 | 1 | 75% | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| C | BLINK1 | 0 | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | |
| D | BLINK2 | 0 | Divided into 64 of vertical synchronous signal | Set blinking frequency. | | | | | | | | | | | | | | | |
| | | 1 | Divided into 32 of vertical synchronous signal | | | | | | | | | | | | | | | | |
| E | TEST30 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | |

Note. The mark 0 around the status value means the reset status by the "L" level is input to \bar{AC} pin.

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode
 Setting external clock input and display frequency mode (by use of EXCK0, EXCK1 (121₁₆) and DIV10 to DIV0 (120₁₆), as explained here following.

(a) When (EXCK1, EXCK0) = (0, 0)External synchronous 1 (External clock display) ... Fosc = 20 to 70 MHz
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal. Never stop inputting the clock while displaying. Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (0, 1)Internal synchronous... Fosc = 20 to 100 MHz
 Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock. The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV10 to DIV0 (address 120₁₆). Also, set the display frequency range. (See the next page.) Display frequency is calculated using the below expression.

$$\text{Display frequency} = \text{Horizontal synchronous frequency} \times \text{Multiply value}$$

(c) When (EXCK1, EXCK0) = (1, 0) Setting disabled

(d) When (EXCK1, EXCK0) = (1, 1)External synchronous 2 (Internal oscillation clock display) ... Fosc = 20 to 100 MHz
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal. Never stop inputting the clock while displaying. An internal clock which is in sync with the external input clock is used as the display clock.

Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV10 to DIV0 (address 120₁₆) for make the display frequency is equal to the external clock frequency.

$$N1 = \text{external clock frequency} / \text{horizontal synchronous frequency}$$

$$N1 = \sum_{n=0}^{10} 2^n \text{DIV}_n$$

Also, set the display frequency range. (See the next page.)

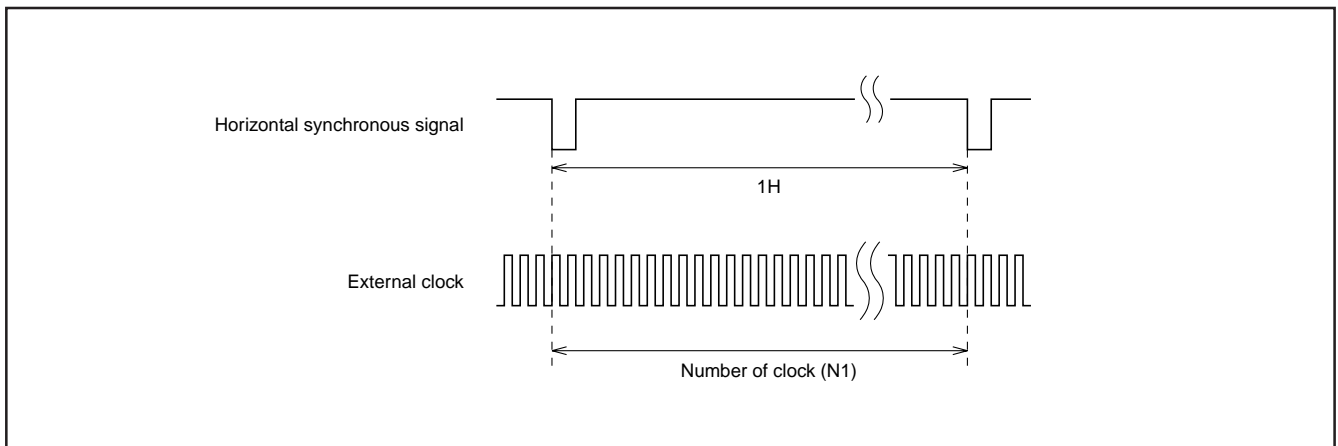


Fig. 12 Example of external clock input

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121₁₆). Frequency ranges are given here below.

| RSEL1 | RSEL0 | DIVS2 | DIVS1 | DIVS0 | Display frequency range MHz |
|-------|-------|-------|-------|-------|-----------------------------|
| 0 | 1 | 0 | 0 | 0 | 90.00 to 100.00 |
| 0 | 0 | 0 | 0 | 0 | 80.00 to 90.50 |
| 1 | 1 | 0 | 0 | 1 | 73.33 to 80.67 |
| 1 | 0 | 0 | 0 | 1 | 66.67 to 74.00 |
| 0 | 1 | 0 | 0 | 1 | 60.00 to 67.33 |
| 0 | 0 | 0 | 0 | 1 | 53.33 to 60.67 |
| 1 | 0 | 0 | 1 | 0 | 50.00 to 54.00 |
| 0 | 1 | 0 | 1 | 0 | 45.00 to 50.50 |
| 0 | 0 | 0 | 1 | 0 | 40.00 to 45.50 |
| 1 | 1 | 0 | 1 | 1 | 36.67 to 40.33 |
| 1 | 0 | 0 | 1 | 1 | 33.33 to 37.00 |
| 0 | 1 | 0 | 1 | 1 | 30.00 to 33.67 |
| 0 | 0 | 0 | 1 | 1 | 26.67 to 30.33 |
| 1 | 0 | 1 | 0 | 0 | 25.00 to 27.75 |
| 0 | 1 | 1 | 0 | 0 | 22.50 to 25.25 |
| 0 | 0 | 1 | 0 | 0 | 20.00 to 22.75 |

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

- (a) Turn the display OFF. ... DSPON (address 129₁₆) = "0"
- (b) Set the display frequency. ... Set from DIV10 to DIV0(address 120₁₆), DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121₁₆).
- (c) Wait 20 ms while the horizontal synchronization signal is being input.
- (d) Turn the display ON. ... DSPON (address 129₁₆) = "1"

To set EXCK1 = "1", EXCK0 = "1"

- (a) Turn the display OFF. ... DSPON (address 129₁₆) = "0"
- (b) Set the display frequency. ... Set from DIV10 to DIV0(address 120₁₆), DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 121₁₆).
- (c) Wait 20 ms while the horizontal synchronization signal and external clock are being input.
- (d) Turn the display ON. ... DSPON (address 129₁₆) = "1"

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DISPLAY FORM 1

M35047-XXXSP/FP has the following four display forms.

(1) ROM character blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

: Blanking the background 12 X 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0 (address 129₁₆), DSP0 to DSP11 (address 125₁₆).

| BCOL | BLK1 | BLK0 | Line of DSPn = "0" | | Line of DSPn = "1" | |
|------|------|------|-------------------------------|---------------------|------------------------|---------------------|
| | | | Display mode | Blanking mode | Display mode | Blanking mode |
| 0 | 0 | 0 | Matrix-outline border display | Matrix-outline size | Matrix-outline display | Matrix-outline size |
| | 0 | 1 | Character display | Character size | Border display | Border size |
| | 1 | 0 | Border display | Border size | Matrix-outline display | Matrix-outlinesize |
| | 1 | 1 | Matrix-outline display | Matrix-outline size | Character display | Character size |
| 1 | 0 | 0 | Matrix-outline border display | All blanking size | Matrix-outline display | All blanking size |
| | 0 | 1 | Character display | | Border display | |
| | 1 | 0 | Border display | | Matrix-outline display | |
| | 1 | 1 | Matrix-outline display | | Character display | |

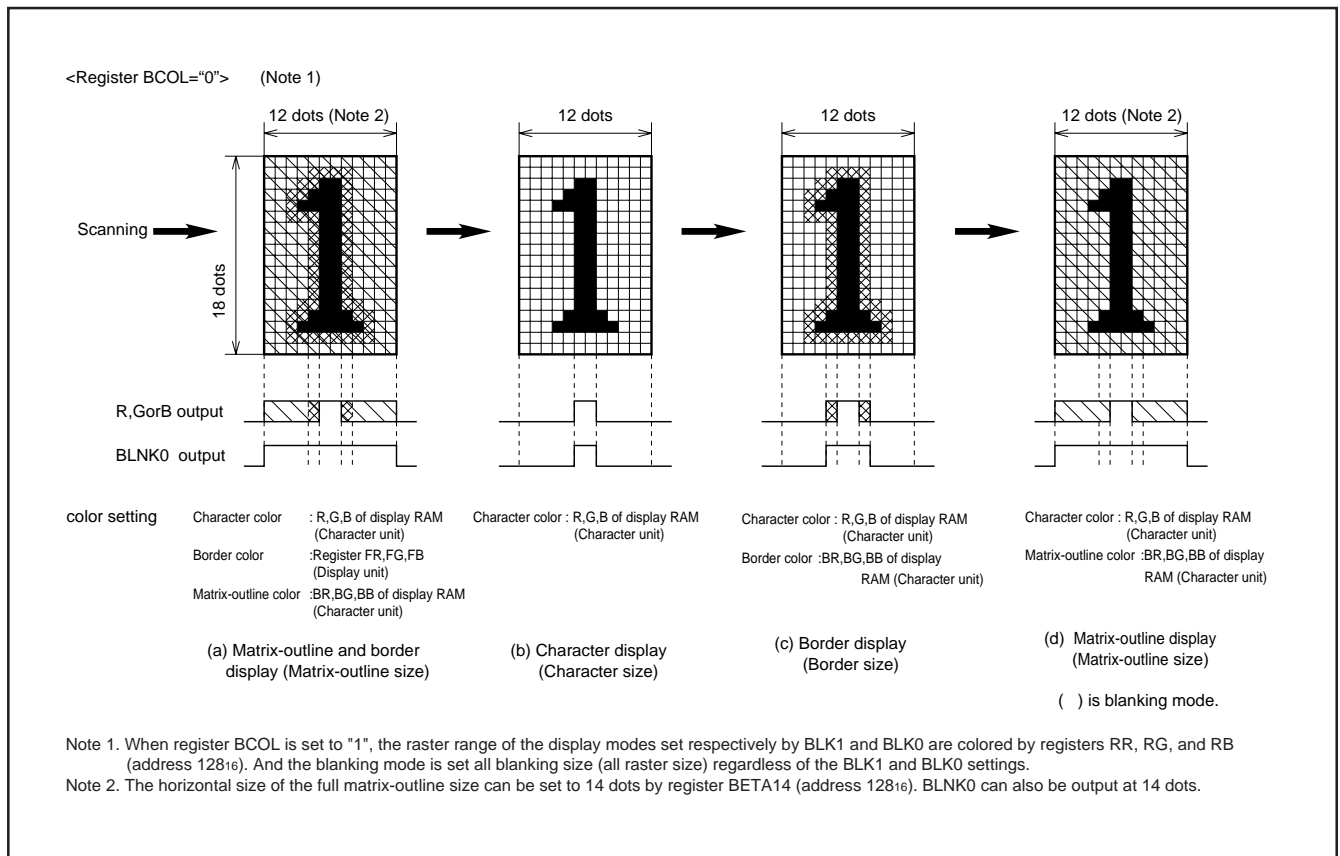


Fig. 13 Display form

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Shadow display

When border display mode, if set SYAD (address 12916) = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

Set shadow display color by BR, BG and BB of display RAM or by register FR, FG and FB.

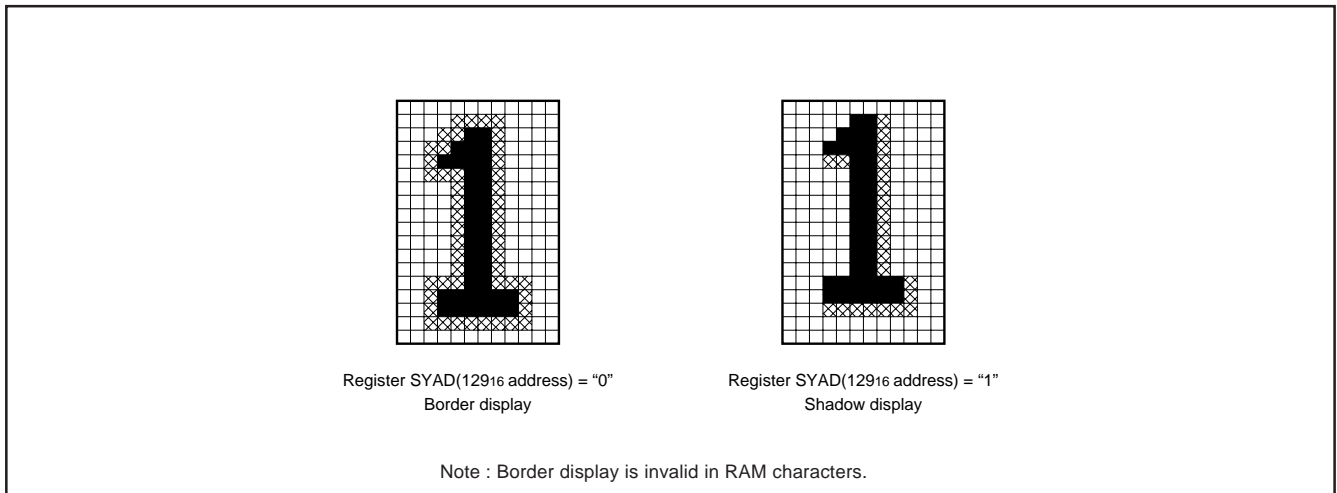


Fig.14 Border and shadow display

DISPLAY FORM 2

This IC can display both ROM character and RAM character at the same time. The display form is shown in Figure 15 and 16.

(1) RAM character blanking mode

| BCOL | RBLK0 | Display mode | Blanking mode |
|------|-------|---------------------------|------------------------|
| 0 | 0 | Matrix-outline display | Matrix-outline size |
| | 1 | Character display (Note1) | Character size (Note2) |
| 1 | 0 | Matrix-outline display | All blanking size |
| | 1 | Character display (Note1) | All blanking size |

Note1: The part of the appointed color by BR, BG and BB of the display RAM changes that is not coloring.

Note2: The part of the appointed color by BR, BG and BB of the display RAM changes that the blanking is "OFF"

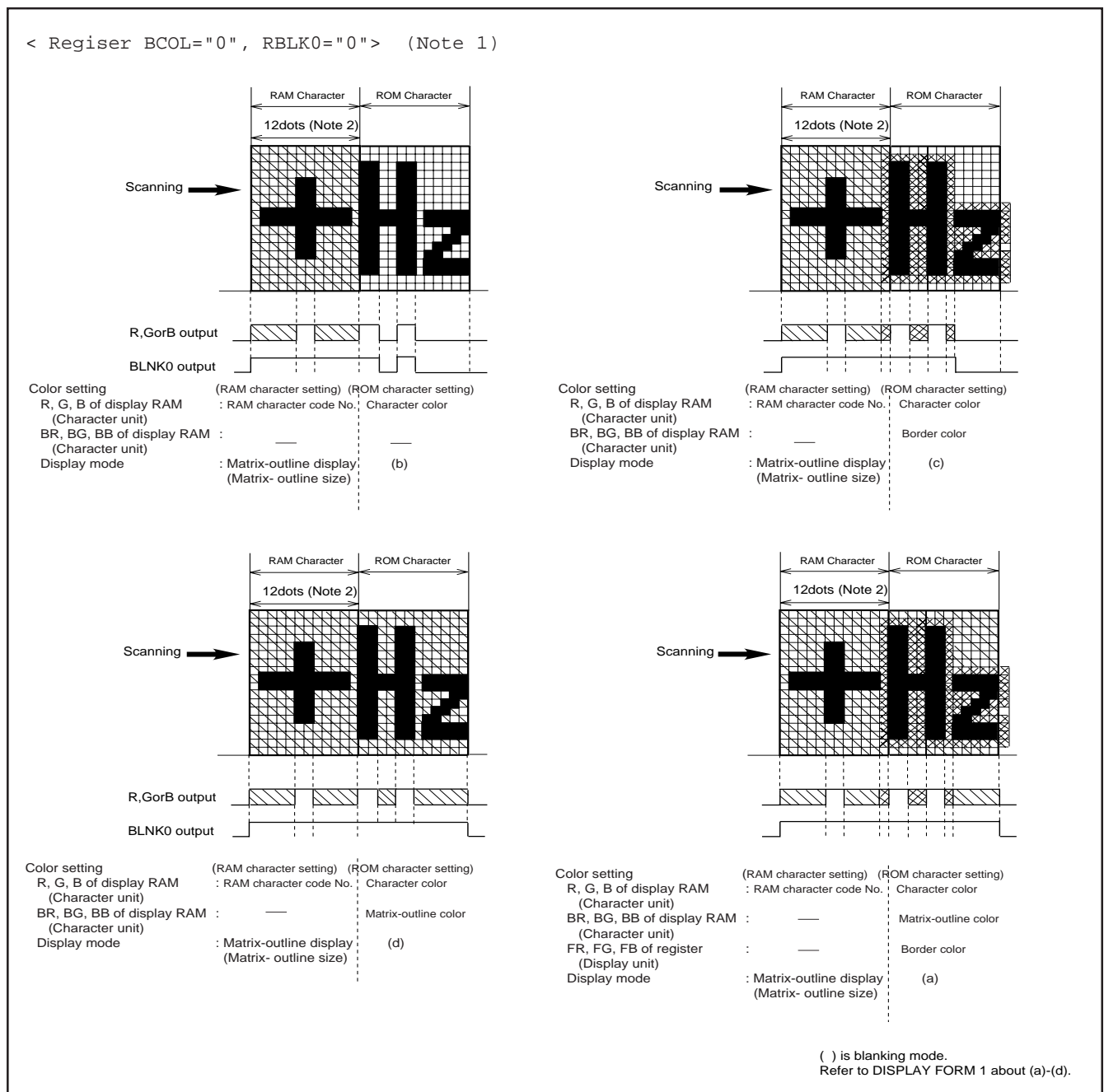
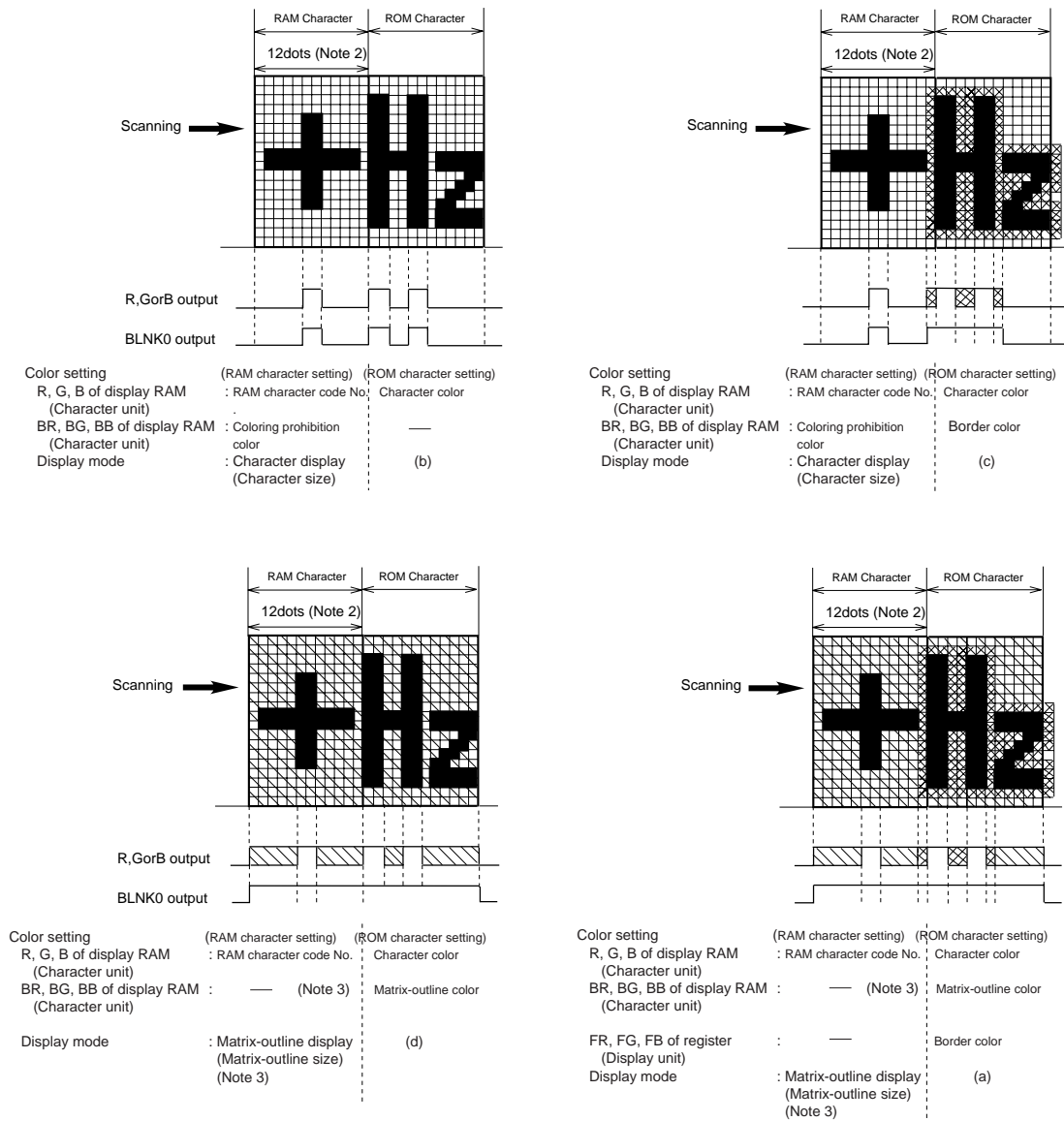


Fig.15 Display form1

Continue to Next

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

< Register BCOL="0", RBLK0="1" > (Note 1)



() is blanking mode.
Refer to DISPLAY FORM 1 about (a)-(d).

- Note 1 : When register BCOL = "1", the raster range of the display modes set respectively by RBLK0 is colored by register RR, RG and RB (address 128₁₆) . And the blanking mode is set all blanking size (all raster size) independent of the RBLK0 settings.
- Note 2 : The horizontal size of the full matrix-outline size can be set to 14 dots by register BETA14 (address 128₁₆). BLNK0 can also be output at 14 dots.
- Note 3 : When display mode (setting by register BLK1, BLK0, DSPn) is Matrix-outline display or Matrix-outline border display, register RBLK0= "1" setting (coloring prohibition color setting) is invalid.

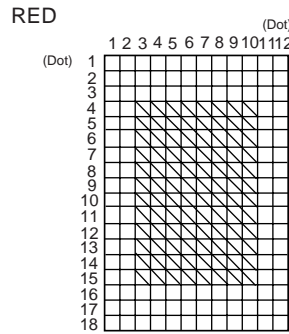
Fig. 16 Display form2

Example of setting RAM character data

For example : RAM character 0

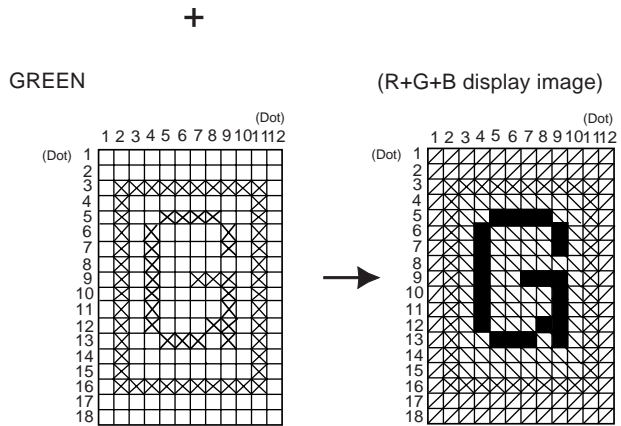
Example of setting the RED bit code data

| Address | DAF | DAE (BS) | DAD (GS) | DAC (RS) | DAB (1) | DAA (2) | DA9 (3) | DA8 (4) | DA7 (5) | DA6 (6) | DA5 (7) | DA4 (8) | DA3 (9) | DA2 (10) | DA1 (11) | DA0 (12) |
|-----------|--------------|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| (1)20016 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2)20116 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (3)20216 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (4)20316 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (5)20416 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (6)20516 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (7)20616 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (8)20716 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (9)20816 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (10)20916 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (11)20A16 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (12)20B16 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (13)20C16 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (14)20D16 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (15)20E16 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (16)20F16 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (17)21016 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (18)21116 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21216 | Can not used | | | | | | | | | | | | | | | |
| ... | | | | | | | | | | | | | | | | |
| 21F16 | Can not used | | | | | | | | | | | | | | | |



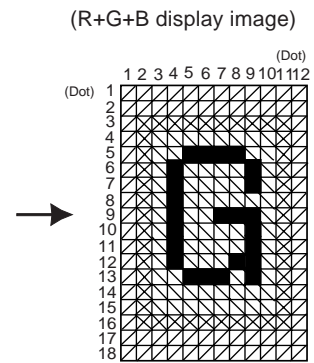
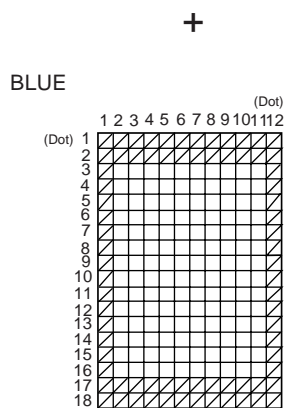
Example of setting the GREEN bit code data

| Address | DAF | DAE (BS) | DAD (GS) | DAC (RS) | DAB (1) | DAA (2) | DA9 (3) | DA8 (4) | DA7 (5) | DA6 (6) | DA5 (7) | DA4 (8) | DA3 (9) | DA2 (10) | DA1 (11) | DA0 (12) |
|-----------|--------------|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| (1)20016 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2)20116 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (3)20216 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (4)20316 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| (5)20416 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| (6)20516 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| (7)20616 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| (8)20716 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| (9)20816 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| (10)20916 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| (11)20A16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| (12)20B16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| (13)20C16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| (14)20D16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| (15)20E16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| (16)20F16 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| (17)21016 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (18)21116 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21216 | Can not used | | | | | | | | | | | | | | | |
| ... | | | | | | | | | | | | | | | | |
| 21F16 | Can not used | | | | | | | | | | | | | | | |



Example of setting the BLUE bit code data

| Address | DAF | DAE (BS) | DAD (GS) | DAC (RS) | DAB (1) | DAA (2) | DA9 (3) | DA8 (4) | DA7 (5) | DA6 (6) | DA5 (7) | DA4 (8) | DA3 (9) | DA2 (10) | DA1 (11) | DA0 (12) |
|-----------|--------------|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|
| (1)20016 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (2)20116 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (3)20216 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (4)20316 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (5)20416 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (6)20516 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (7)20616 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (8)20716 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (9)20816 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (10)20916 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (11)20A16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (12)20B16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (13)20C16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (14)20D16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (15)20E16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (16)20F16 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| (17)21016 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| (18)21116 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 21216 | Can not used | | | | | | | | | | | | | | | |
| ... | | | | | | | | | | | | | | | | |
| 21F16 | Can not used | | | | | | | | | | | | | | | |



- Note 1 : After clearing or setting all character RAM areas, and use the RAM characters.
- Note 2 : The RAM character's dots are set RED, GREEN and BLUE data, which are controlled by BS, GS and RS bit. (Can be set at same time)

Fig.17 Setting of the data of RAM character

CHARACTER FONT

Images are composed on a 12 X 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF16 is fixed as a blank without background. Therefore, cannot register a character font in this code.

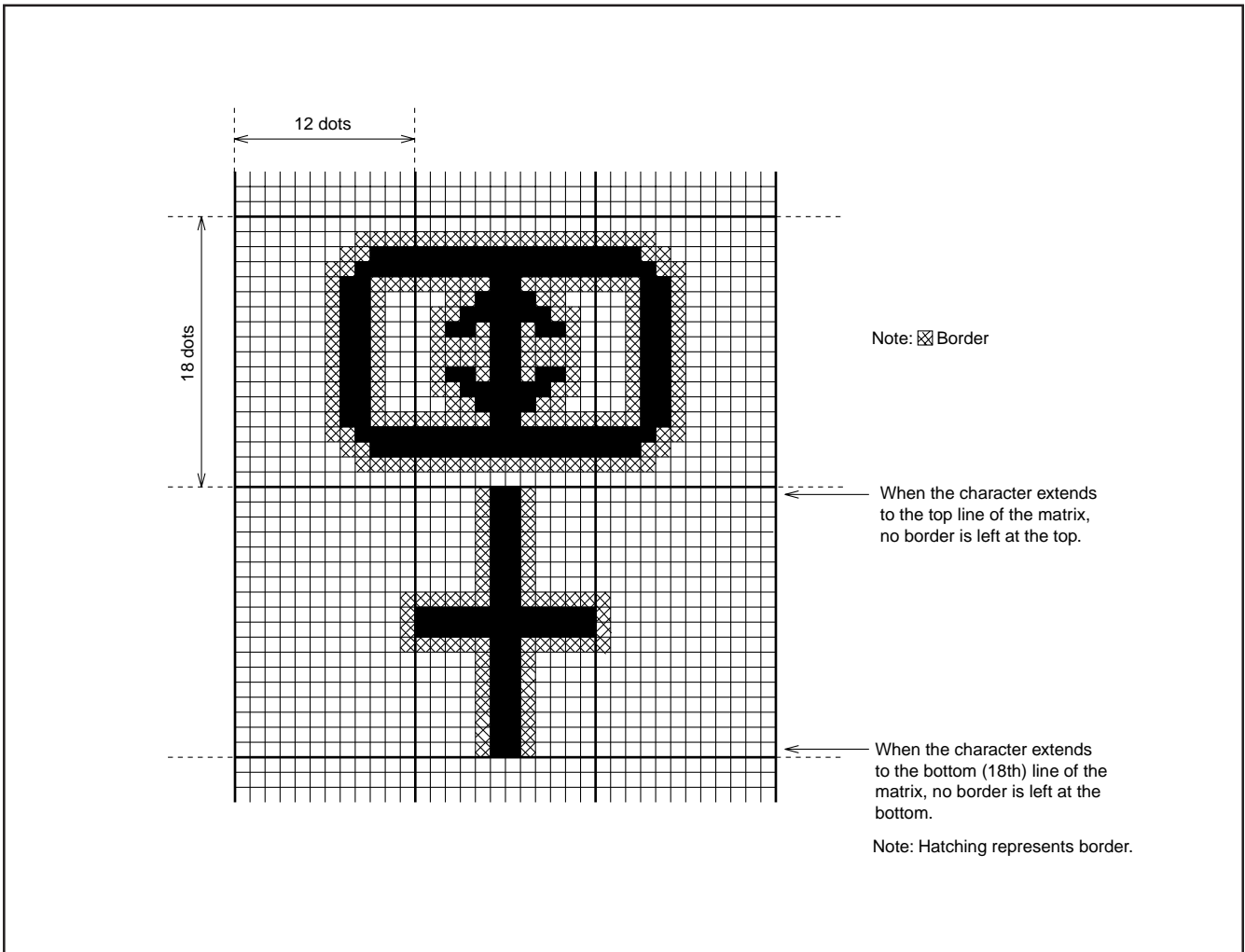


Fig.18 Example of border display

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the I²C-BUS serial input function. Example of data setting is shown in Figure 19 (at EXCK0 = "1", EXCK1 = "0" setting).

| Address/data | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Remarks |
|---------------------------|-----|---------------------|-----|----------------|-----------------|--------|----------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------------------------------------|
| 200 m sec hold | | | | | | | | | | | | | | | | | System set up (Note 3) |
| Address 120 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Address setting |
| Data 120 ₁₆ | 0 | 0 | 0 | 0 | 0 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 | Frequency value setting |
| Data 121 ₁₆ | 0 | 0 | 1 | RSEL1 | RSELO | DIVS2 | DIVS1 | DIVS0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Frequency range setting |
| Data 122 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Output setting |
| Data 123 ₁₆ | 0 | 0 | 0 | 0 | 0 | HP10 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display location setting |
| Data 124 ₁₆ | 0 | 0 | 0 | 0 | 0 | VP10 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display location setting |
| Data 125 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Display form setting |
| Data 126 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| Data 127 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| Data 128 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Color, character size setting |
| Data 129 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | POLH | POLV | 0 | 0 | 0 | Display OFF |
| 20 m sec hold | | | | | | | | | | | | | | | | | Be stable/Waiting time |
| Address 200 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Address setting |
| Data 200 ₁₆ | 0 | 0 | 0 | 1 | FR000B | FR000A | FR0009 | FR0008 | FR0007 | FR0006 | FR0005 | FR0004 | FR0003 | FR0002 | FR0001 | FR0000 | RED•bit code setting |
| ⋮ | ⋮ | Bit color | | Bit code/RED | | | | | | | | | | | | | |
| Data 2F ₁₆ | 0 | 0 | 0 | 1 | FR711B | FR711A | FR7119 | FR7118 | FR7117 | FR7116 | FR7115 | FR7114 | FR7113 | FR7112 | FR7111 | FR7110 | Address setting |
| Address 200 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Data 200 ₁₆ | 0 | 0 | 1 | 0 | FR000B | FR000A | FR0009 | FR0008 | FR0007 | FR0006 | FR0005 | FR0004 | FR0003 | FR0002 | FR0001 | FR0000 | GREEN•bit code setting |
| ⋮ | ⋮ | Bit color | | Bit code/GREEN | | | | | | | | | | | | | |
| Data 2F ₁₆ | 0 | 0 | 1 | 0 | FR711B | FR711A | FR7119 | FR7118 | FR7117 | FR7116 | FR7115 | FR7114 | FR7113 | FR7112 | FR7111 | FR7110 | Address setting |
| Address 200 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Data 200 ₁₆ | 0 | 1 | 0 | 0 | FR000B | FR000A | FR0009 | FR0008 | FR0007 | FR0006 | FR0005 | FR0004 | FR0003 | FR0002 | FR0001 | FR0000 | BLUE•bit code setting |
| ⋮ | ⋮ | Bit color | | Bit code/BLUE | | | | | | | | | | | | | |
| Data 2F ₁₆ | 0 | 1 | 0 | 0 | FR711B | FR711A | FR7119 | FR7118 | FR7117 | FR7116 | FR7115 | FR7114 | FR7113 | FR7112 | FR7111 | FR7110 | Address setting |
| Address 000 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Data 000 ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Character setting |
| ⋮ | ⋮ | Background coloring | | Blink-ing | Character color | | Character code | | | | | | | | | | |
| Data 11F ₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Address setting |
| Address 129 ₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | |
| Data 129 ₁₆ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display ON (Note 2) |

Notes 1: Input a continuous clock of constant period from the TCK pin. Also, input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
 2: Matrix-outline display in this data.
 3: Secure the waiting time of 200ms after releasing \overline{AC} , and set data from setting the display frequency (setting of the register).

Fig. 19 Example of data setting

M35047-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

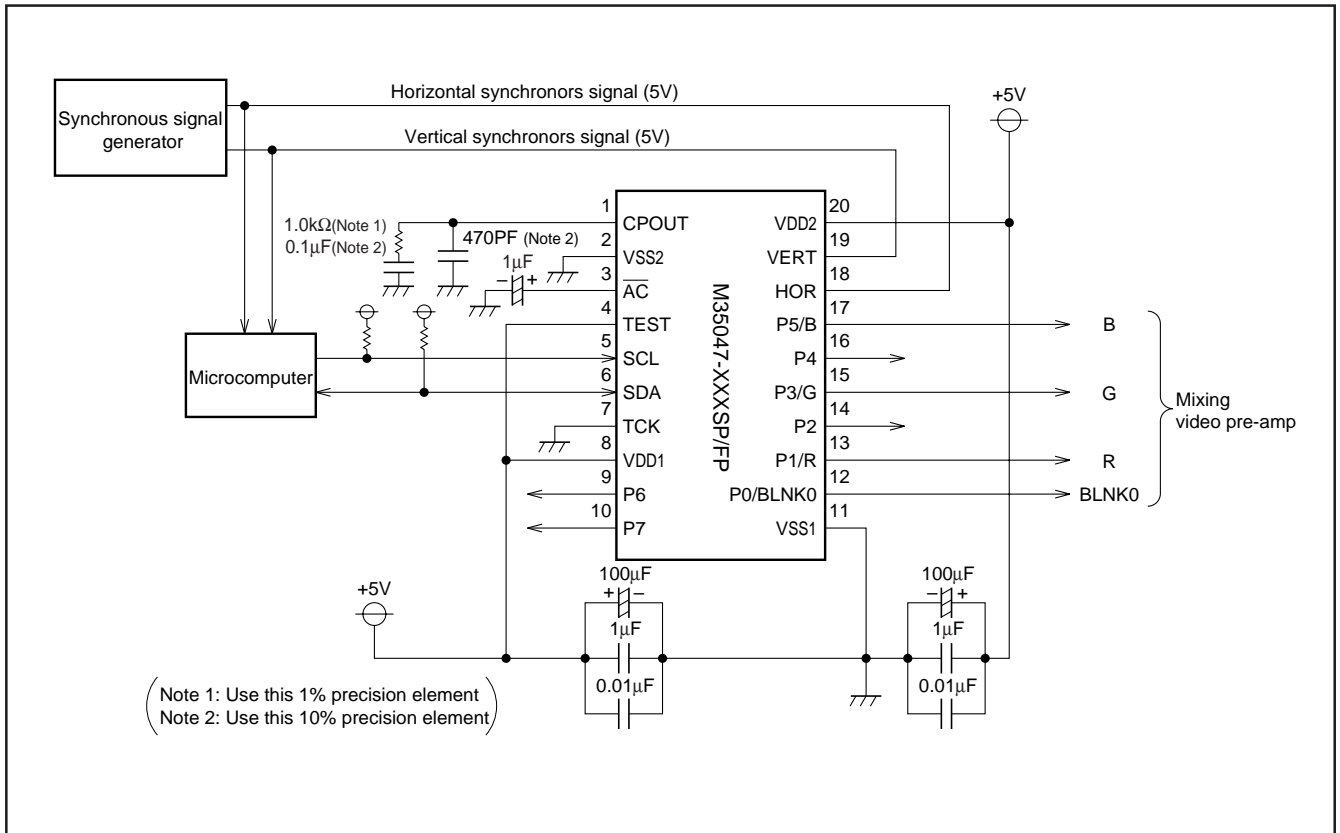
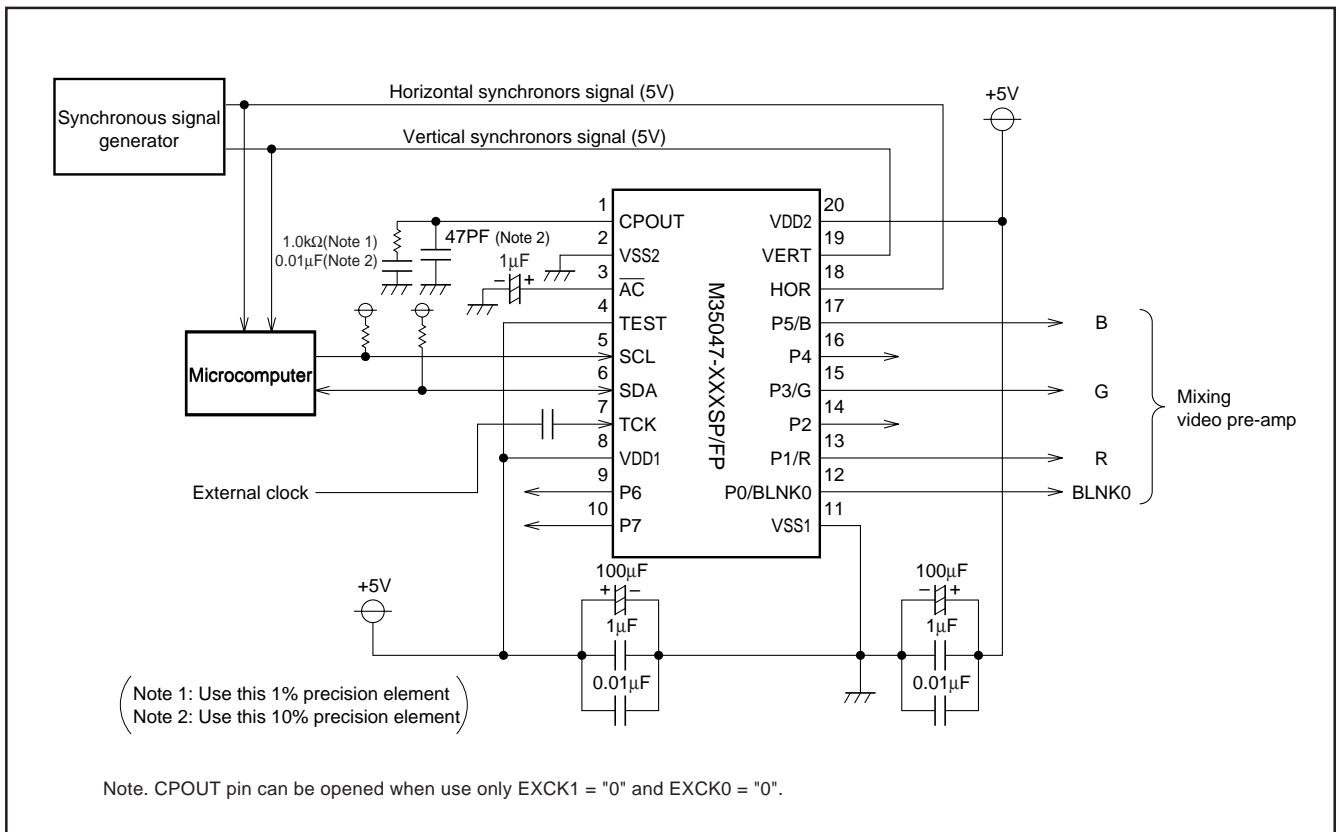


Fig.20 Example of the M35047-XXXSP/FP peripheral circuit (Internal synchronous. At EXCK1 = "0", EXCK0 = "1")



Note. CPOUT pin can be opened when use only EXCK1 = "0" and EXCK0 = "0".

Fig.21 Example of the M35047-XXXSP/FP peripheral circuit (External synchronous. At EXCK1 = "1", EXCK0 = "1")

DATA INPUT

(1) I²C-Bus communication function

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA).

Communications are controlled from the start/stop states. Also, always in put the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

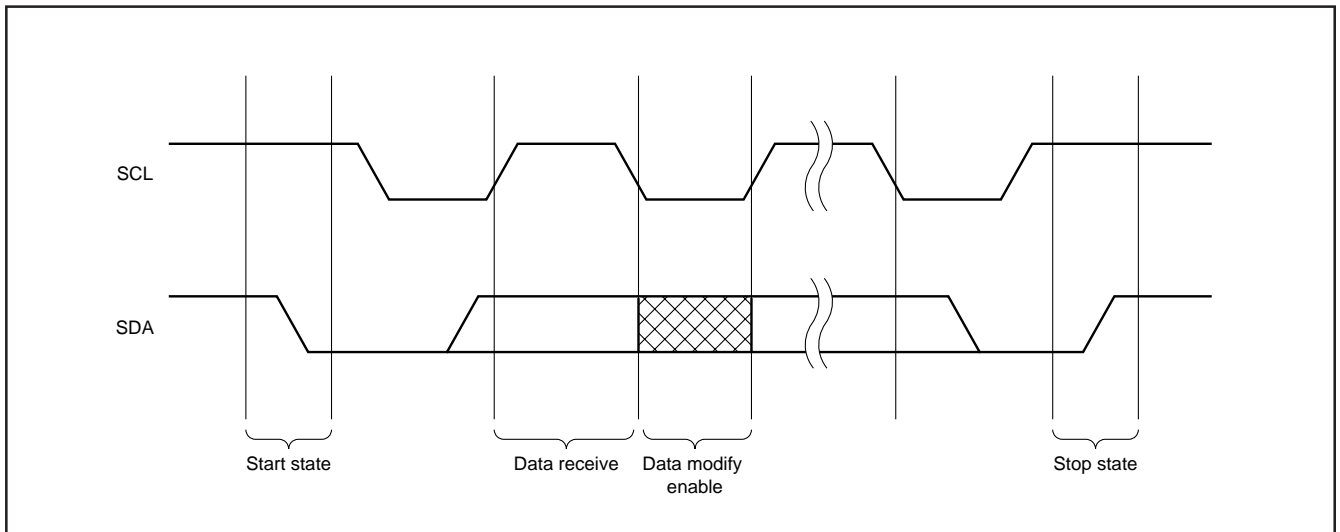


Fig.22 Start state / Stop state

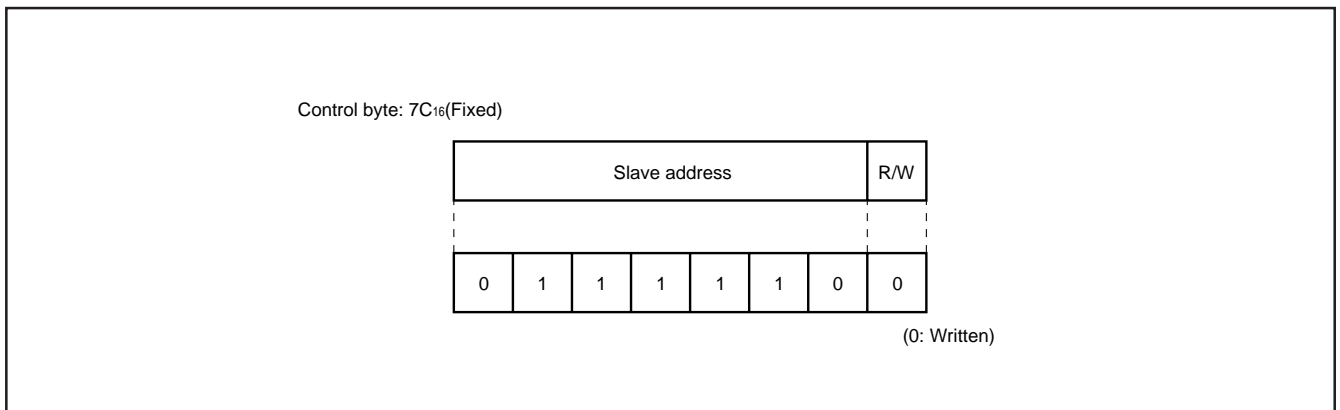


Fig.23 Control byte configuration

(2) Data input (Sequence)

- (a) Addresses are consists of 16 bits.
- (b) Data is consists of 16 bits.
- (c) Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.
- (d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 16 bits (2 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note: During external synchronous, do not stop the external clock input from the TCK pin while inputting data.

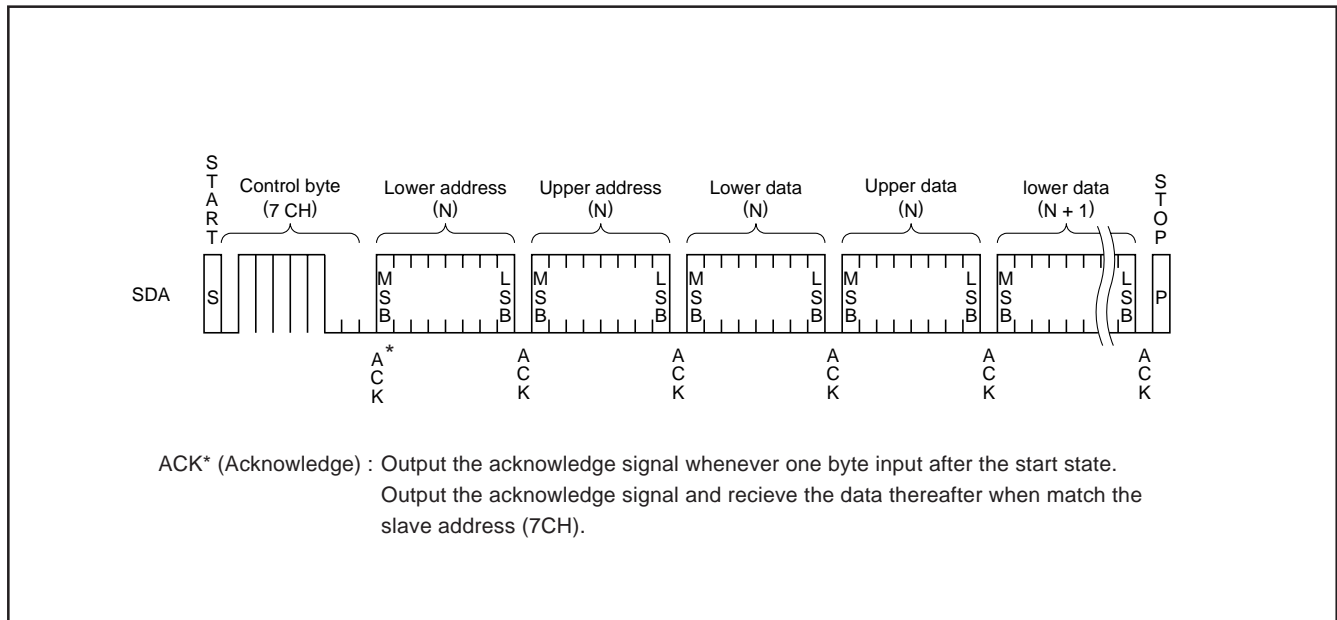


Fig.24 Data input sequence

TIMING REQUIREMENTS

Data input

| Symbol | Parameter | Limits | | | | Unit | Remarks |
|-----------|---|-----------|------|--------------------|------|------|--|
| | | Typ. mode | | High-speed mode | | | |
| | | Min. | Max. | Min. | Max. | | |
| fCLK | Clock frequency | 0 | 100 | 0 | 400 | KHz | |
| tHIGH | HIGH period of Clock | 4000 | – | 600 | – | ns | |
| tLOW | LOW period of Clock | 4700 | – | 1300 | – | ns | |
| tR | SDA & SCL rise time | – | 1000 | 20+(Note) 0.1CB | 300 | ns | |
| tF | SDA & SCL fall time | – | 300 | 20+(Note) 0.1CB | 300 | ns | |
| tHD : STA | Hold time at START status | 4000 | – | 600 | – | ns | |
| tsu : STA | Set up time at START status | 4700 | – | 600 | – | ns | Only at START state repeating generation |
| tHD : DAT | Data input hold time | 0 | – | 0 | – | ns | |
| tsu : DAT | Data input setup time | 250 | – | 100 | – | ns | |
| tsu : STO | Set up time at STOP state | 4000 | – | 600 | – | ns | |
| tBUF | Bus release time | 4700 | – | 1300 | – | ns | Time must be released bus before next transmission |
| tSP | Input filter / spike suppress (SDA & SCL pin) | N/A | N/A | 0 | 50 | ns | |

Note. CB = total capacitance of 1 bus line.

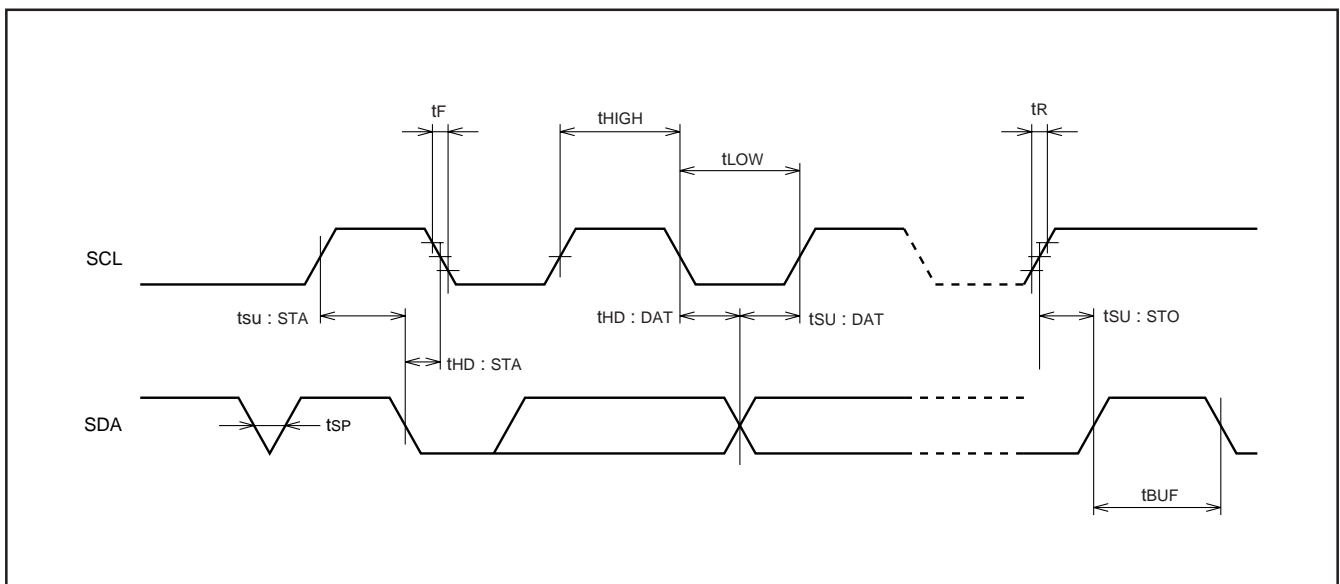


Fig.25 Data input timing

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|--------|-----------------------|----------------------|---|-------------|
| VDD | Supply voltage | With respect to VSS. | -0.3 to +6.0 | V |
| Vi | Input voltage | | $V_{SS} - 0.3 \leq V_i \leq V_{DD} + 0.3$ | V |
| Vo | Output voltage | | $V_{SS} \leq V_o \leq V_{DD}$ | V |
| Pd | Power dissipation | $T_a = +25^{\circ}C$ | +300 | mW |
| Topr | Operating temperature | | -20 to +85 | $^{\circ}C$ |
| Tstg | Storage temperature | | -40 to +125 | $^{\circ}C$ |

RECOMMENDED OPERATING CONDITIONS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | |
|--------|---|---------------------------|--------|-------|--------|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply voltage | 4.75 | 5.0 | 5.25 | V | |
| VIH | "H" level input voltage | \overline{AC} HOR, VERT | 0.8VDD | VDD | VDD | V |
| | | SCL, SDA | 0.7VDD | VDD | VDD | V |
| VIL | "L" level input voltage | \overline{AC} HOR, VERT | 0 | 0 | 0.2VDD | V |
| | | SCL, SDA | 0 | 0 | 0.3VDD | V |
| FOSC | Oscillating frequency for display | 20.0 | — | 100.0 | MHz | |
| H.sync | Horizontal synchronous signal input frequency | 15.0 | — | 130.0 | kHz | |

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.00V$, $T_a = 25^{\circ}C$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|--------|------------------------------------|--------------------------------|--------|------|--------|------------|---------------------------------------|
| | | | Min. | Typ. | Max. | | |
| VDD | Supply voltage | $T_a = -20$ to $+85^{\circ}C$ | 4.75 | 5.0 | 5.25 | V | |
| IDD | Supply current | $V_{DD} = 5.00V$ | — | 40 | 60 | mA | |
| VOH | "H" level output voltage | P0 to P7 (Note1) | 3.5 | — | — | V | |
| | | CPOUT | | | | | $V_{DD} = 4.75V$, $I_{OH} = -0.05mA$ |
| VOL | "L" level output voltage | P0 to P7 (Note2) | — | — | 0.4 | V | |
| | | CPOUT | | | | | $V_{DD} = 4.75V$, $I_{OL} = 0.05mA$ |
| | | SDA | | | | | $V_{DD} = 4.75V$, $I_{OL} = 3.0mA$ |
| Ri | Pull-up resistance \overline{AC} | $V_{DD} = 5.00V$ | 10 | 30 | 100 | k Ω | |
| VTCK | External clock input width | $4.75V \leq V_{DD} \leq 5.25V$ | 0.6VDD | — | 0.9VDD | V | |

Notes 1. The current from the IC must not exceed -0.4 mA/port at any of the port pins (P0 to P7).
 2. The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1)Timing of power supplying to AC pin

The internal circuit of M35047-XXXSP/FP is reset when the level of the auto clear input pin \overline{AC} is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of \overline{AC} pin is shown in Figure 26.

After supplying the power (V_{DD} and V_{SS}) to M35047-XXXSP/FP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the \overline{AC} pin for more than 1ms.

Start inputting from microcomputer after \overline{AC} pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

(2)Timing of power supplying to V_{DD1} and V_{DD2} .

Supply power to V_{DD1} and V_{DD2} at the same time.

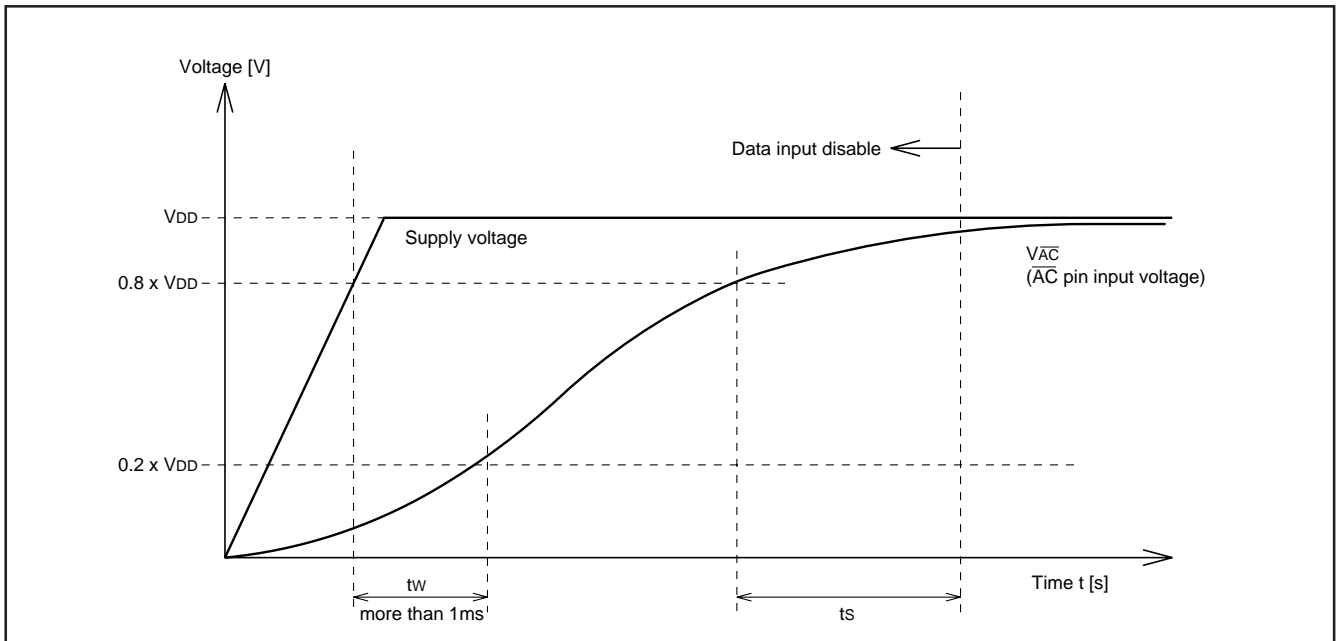


Fig.26 Timing of power supplying to AC pin

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/F register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/F register.

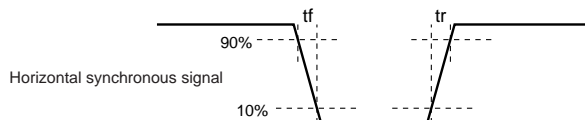
DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35047-XXXSP/FP mask ROM order confirmation form
- (2) 20P4B mark specification form
- (3) 20P2Q-A mark specification form
- (4) ROM data : EPROMs or floppy disks

*In the case of EPROMs, thres sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.



STANDARD ROM TYPE : M35047-002SP/FP

M35047-002SP/FP is a standard ROM type of M35047-XXXSP/FP.
The character patterns are fixed to the contents of Figure 27 to 30.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

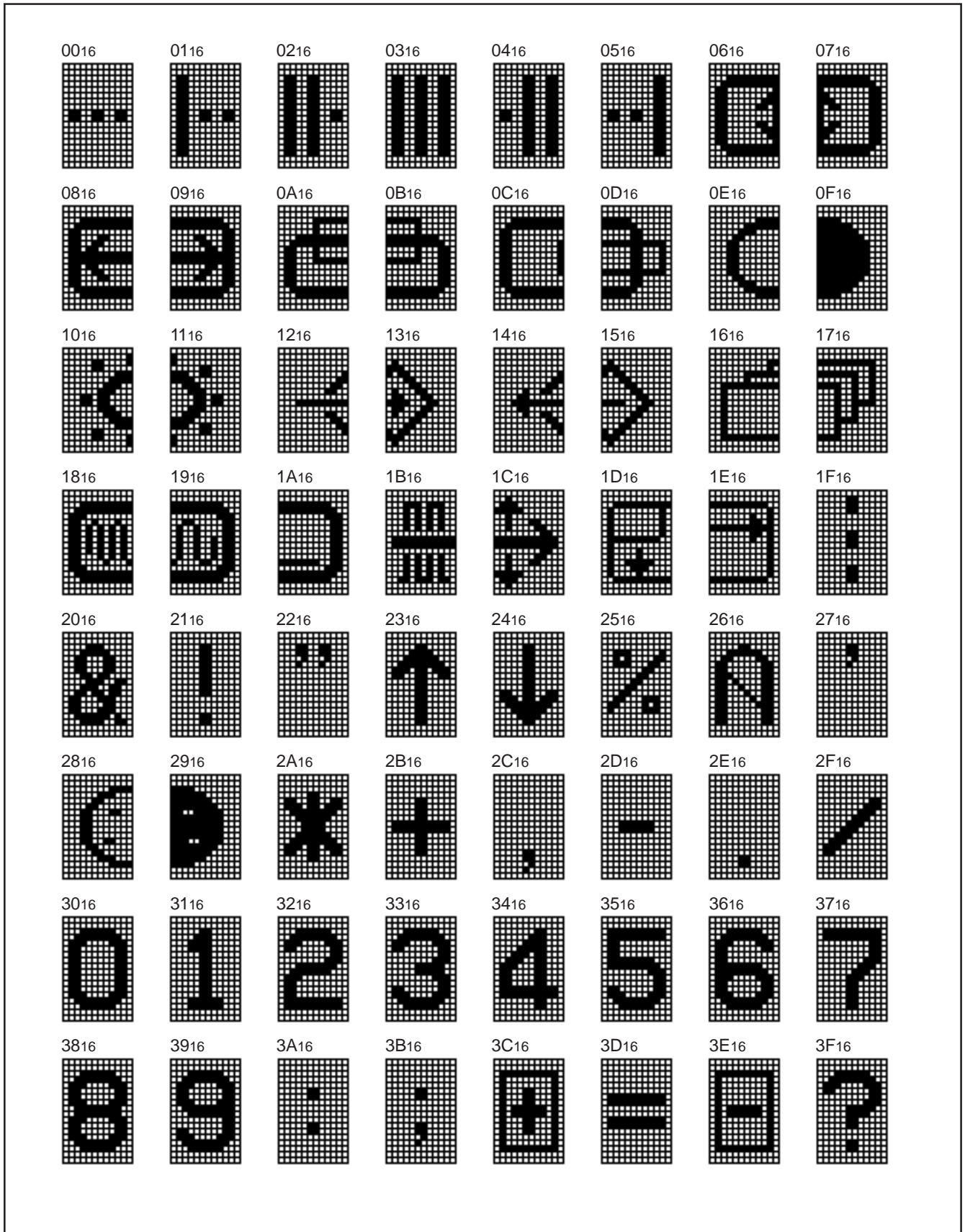


Fig.27 M35047-002SP/FP character patterns (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



Fig.28 M35047-002SP/FP character patterns (2)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

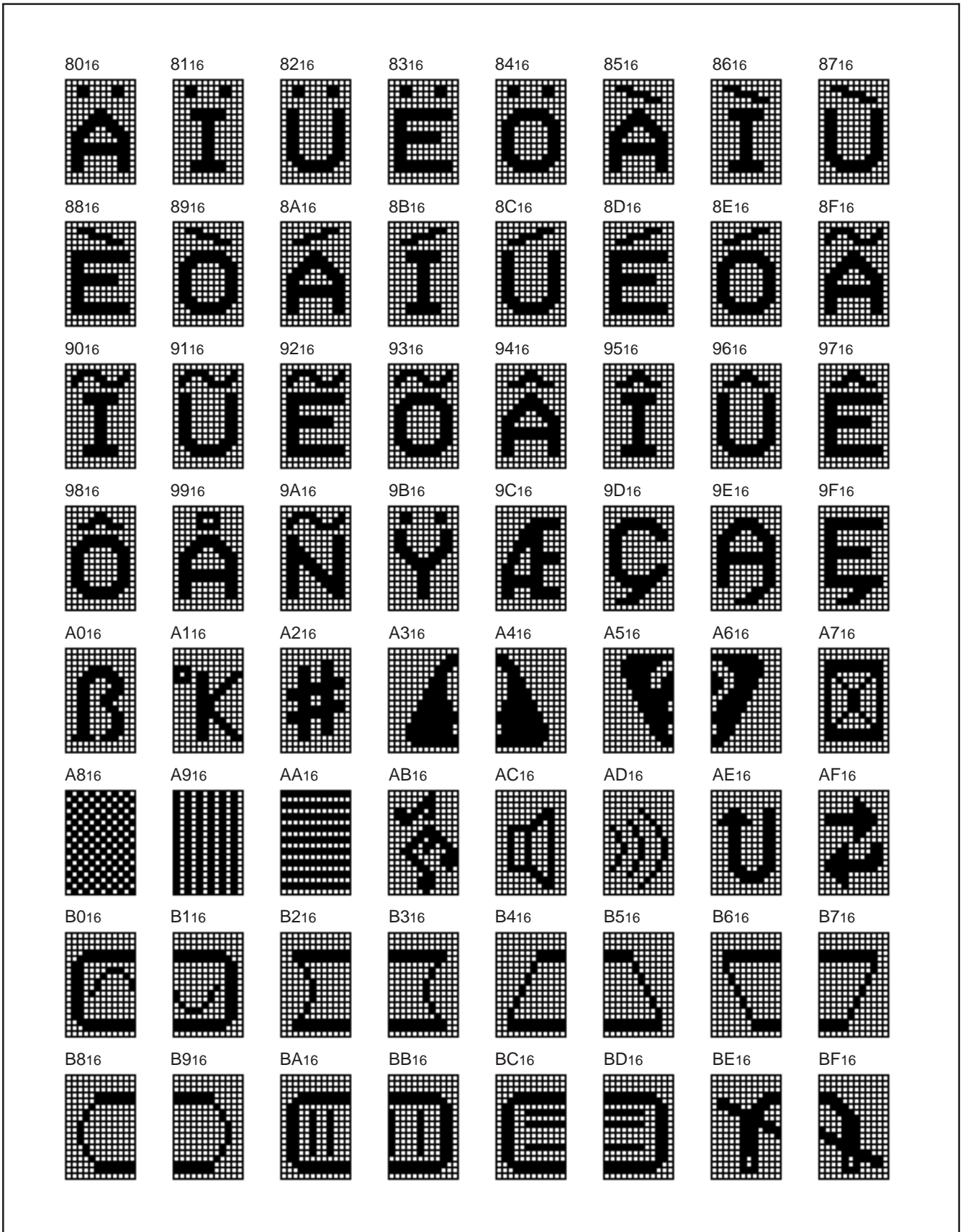


Fig.29 M35047-002SP/FP character patterns (3)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



Fig.30 M35047-002SP/FP character patterns (4)

M35047-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

GZZ-SH56-34B<92A0>

| | |
|-----------------|--|
| Mask ROM number | |
|-----------------|--|

**MASK ROM CONFIRMATION FORM
SCREEN DISPLAY IC M35047-XXXSP/FP
MITSUBISHI ELECTRIC**

| | | |
|---------|------------------------|----------------------|
| Receipt | Data : | |
| | Section head signature | Supervisor signature |
| | | |

Note : Please fill in all items marked *, □.

| | | | | | |
|------------|--------------|--------|--------------------|--------------|------------|
| * Customer | Company name | TEL | Issuance signature | Submitted by | Supervisor |
| | Data issued | Date : | | () | |

* 1. Confirmation

Confirm the Character Font Preparation Program in Mitsubishi Sales Sites.
Three EPROMs are required for each pattern if this order is performed by EPROMs.
One floppy disk is required for each pattern if this order is performed by a floppy disk.

□ Ordering by EPROMs

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs (27512 type used).

- (1) The font data prepared by the Character Font Preparation Program is saved as a binary type object file (addresses 0000h to FFFFh) and a hex type object file . Three sets of these EPROMs are required.
- (2) Attach the erase protect seals on three EPROMs. Each seal bears the type name (M35047), and ROM No. (-...SP/FP).

Checksum code for entire EPROM

| | | | |
|--|--|--|--|
| | | | |
|--|--|--|--|

 (hexadecimal notation)

Save file name

| | | | | | | | |
|---|---|---|---|---|--|--|--|
| M | 0 | 4 | 7 | R | | | |
|---|---|---|---|---|--|--|--|

 .

| | | | |
|---|--|--|--|
| V | | | |
|---|--|--|--|

 (equal or less than eight characters)

□ Ordering by floppy disk

We will produce masks based on the mask files generated by the mask file generating utility. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this mask file. Thus, extreme care must be taken to verify the mask file in the submitted floppy disk.

The mask files forms hex-file made by the character font preparation program in the mask file generation utility. Submit the mask file after be saved in the floppy disk.

The submitted floppy disk must be 3.5-inch 2HD type and DOS/V format. And the number of the mask files must be one in one floppy disk.

File code

| | | | | | | | |
|--|--|--|--|--|--|--|--|
| | | | | | | | |
|--|--|--|--|--|--|--|--|

 (hexadecimal notation)

Mask file name

| | | | | | | | |
|--|--|--|--|--|--|--|--|
| | | | | | | | |
|--|--|--|--|--|--|--|--|

 .MSK (equal or less than eight characters)

* 2. Select the marking type (Check ✓ in the appropriate box).

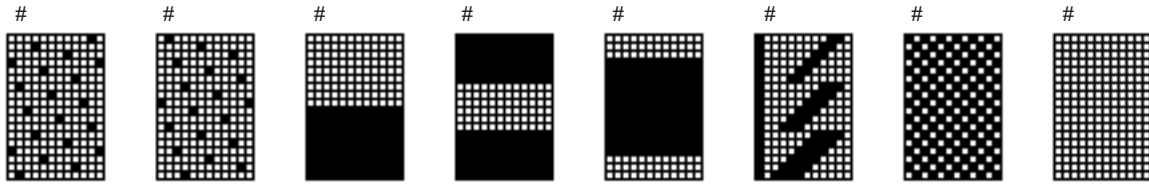
- Special Mark Fill in the Mark Specification Form (20P4B for M35047-XXXSP, 20P2Q-A for M35047-XXXFP) and attach to the Mask ROM Confirmation Form.
- Standard Mark No writing is required.

* 3. Select the package type (Check ✓ in the appropriate box).

- SDIP (M35047-XXXSP)
- SSOP (M35047-XXXFP)

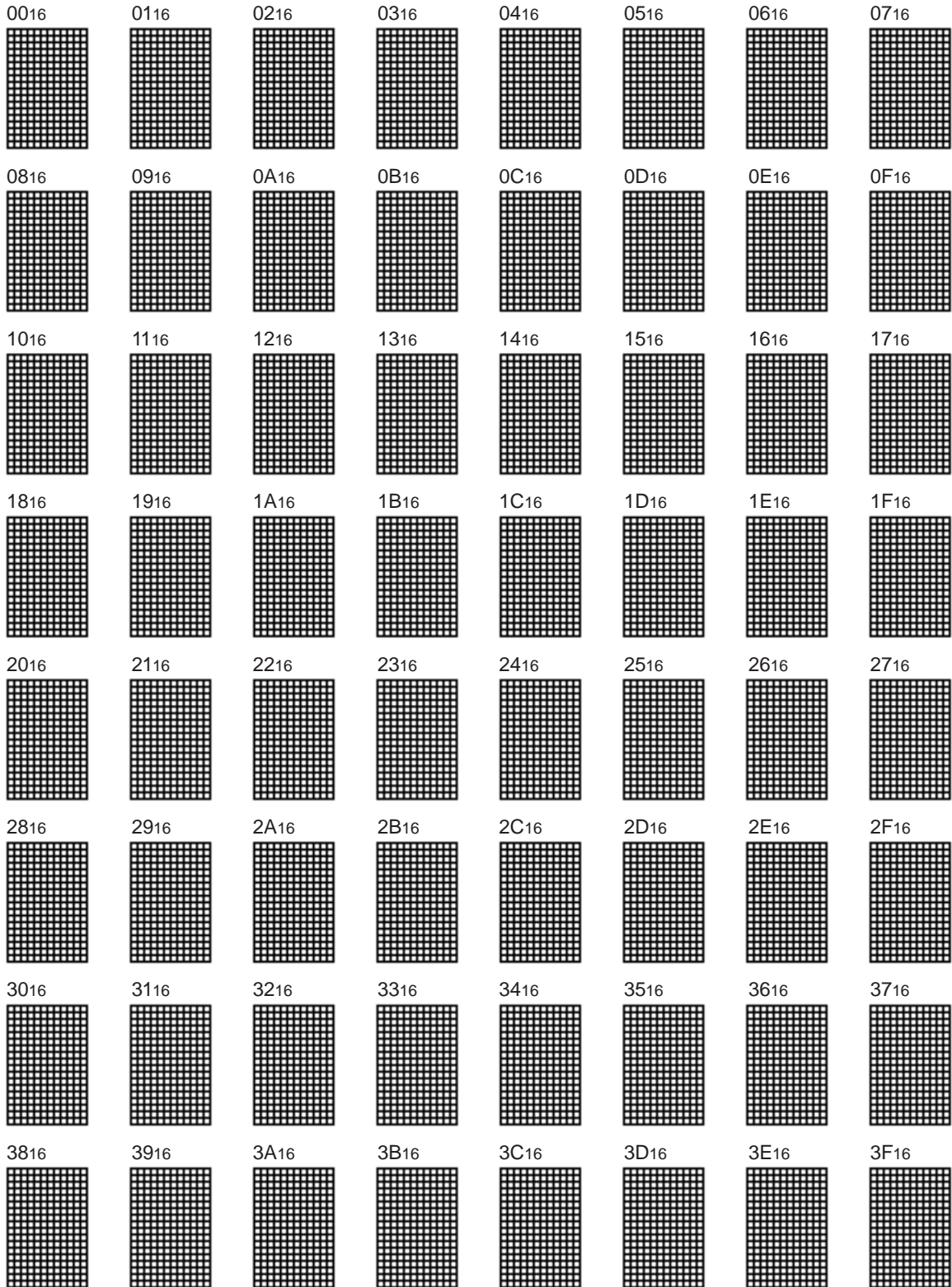
* 4. Comments

* 5. Test patterns

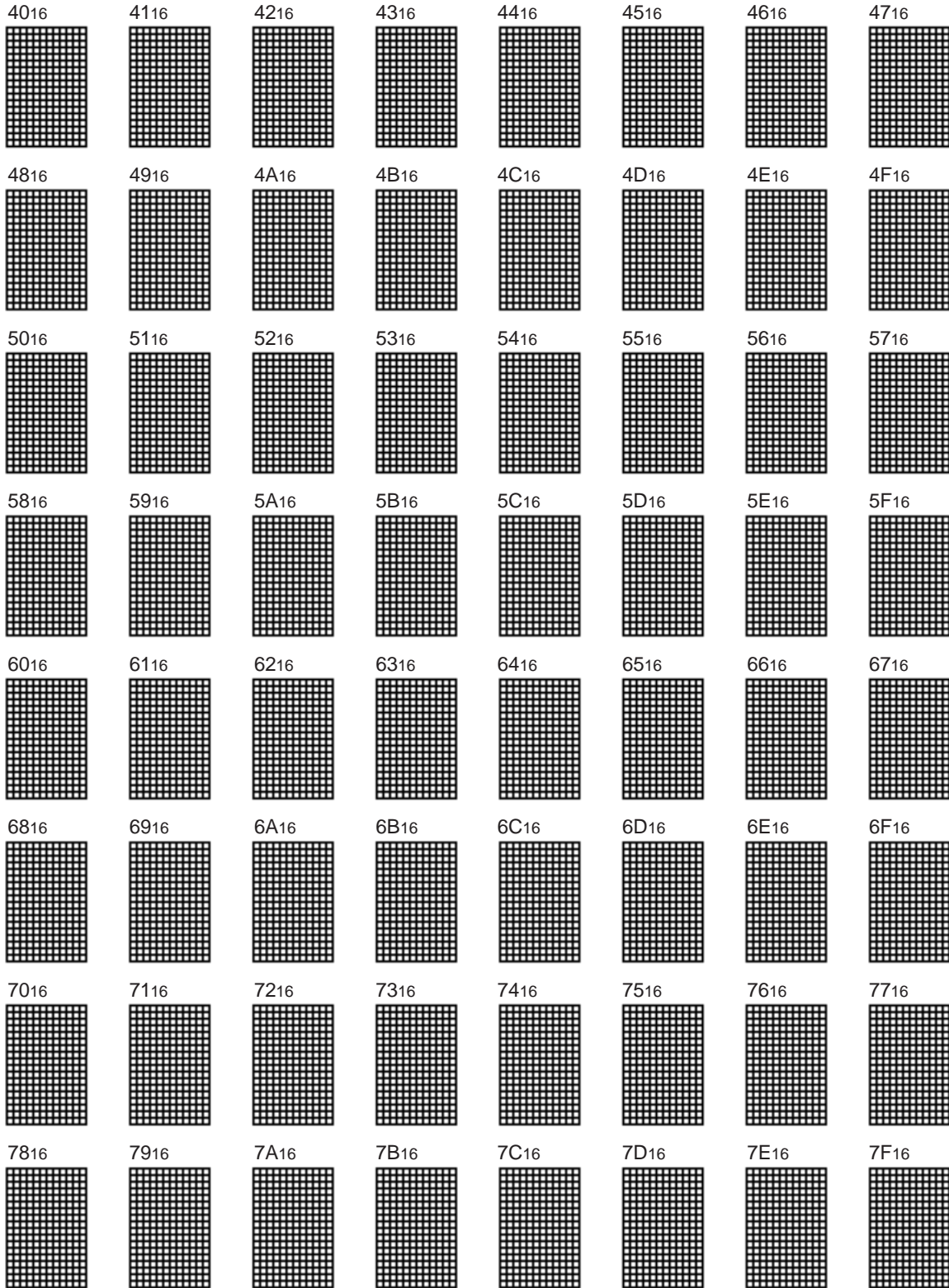


* 6. Character patterns
(See the next page)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

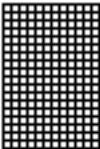
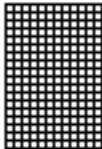
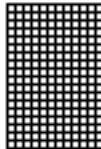
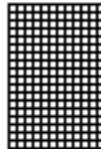
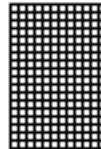
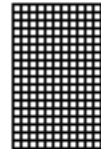
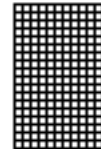
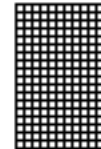
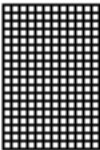
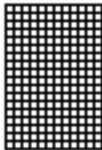
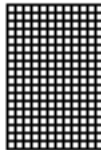
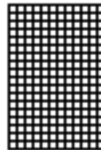
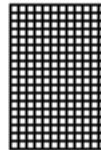
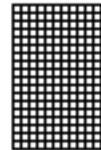
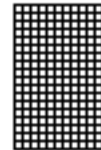
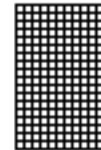
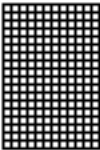
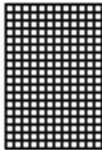
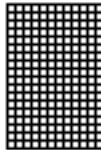
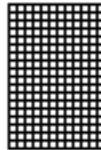
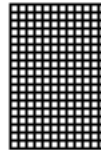
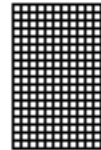
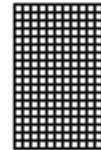
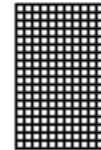
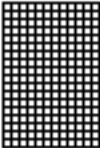
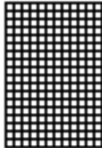
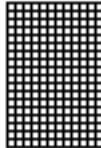
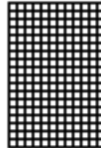
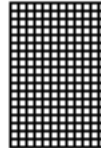
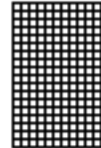
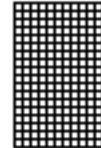
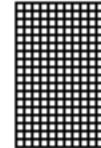
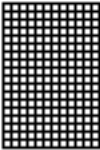
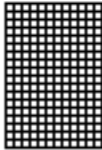
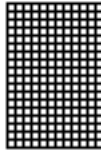
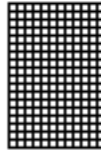
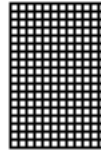
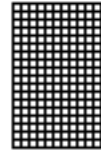
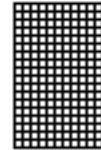
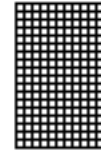
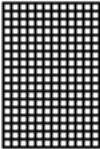
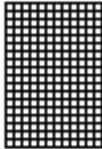
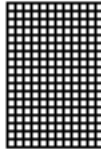
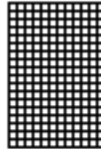
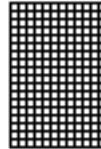
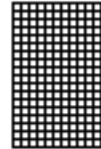
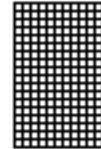
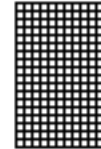
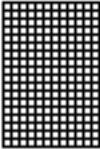
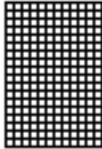
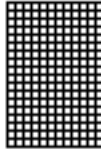
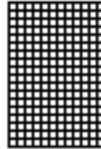
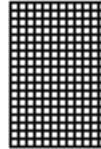
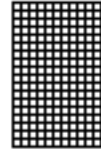
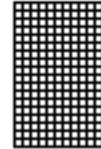
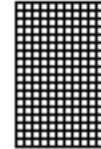
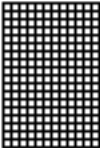
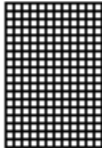
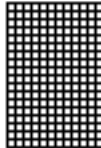
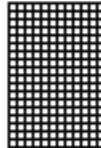
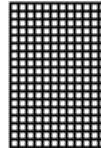
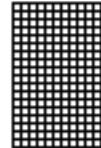
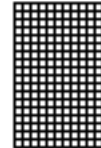
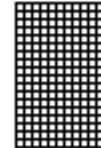


SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



M35047-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

| | | | | | | | |
|---|---|---|---|---|--|---|---|
| 8016  | 8116  | 8216  | 8316  | 8416  | 8516  | 8616  | 8716  |
| 8816  | 8916  | 8A16  | 8B16  | 8C16  | 8D16  | 8E16  | 8F16  |
| 9016  | 9116  | 9216  | 9316  | 9416  | 9516  | 9616  | 9716  |
| 9816  | 9916  | 9A16  | 9B16  | 9C16  | 9D16  | 9E16  | 9F16  |
| A016  | A116  | A216  | A316  | A416  | A516  | A616  | A716  |
| A816  | A916  | AA16  | AB16  | AC16  | AD16  | AE16  | AF16  |
| B016  | B116  | B216  | B316  | B416  | B516  | B616  | B716  |
| B816  | B916  | BA16  | BB16  | BC16  | BD16  | BE16  | BF16  |

M35047-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

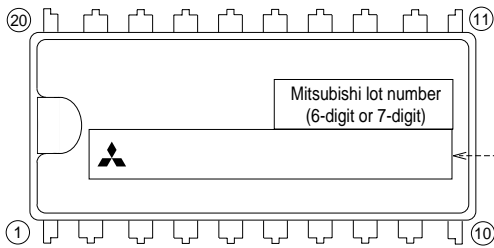
| | | | | | | | |
|------|------|------|------|------|------|------|-----------|
| C016 | C116 | C216 | C316 | C416 | C516 | C616 | C716 |
| C816 | C916 | CA16 | CB16 | CC16 | CD16 | CE16 | CF16 |
| D016 | D116 | D216 | D316 | D416 | D516 | D616 | D716 |
| D816 | D916 | DA16 | DB16 | DC16 | DD16 | DE16 | DF16 |
| E016 | E116 | E216 | E316 | E416 | E516 | E616 | E716 |
| E816 | E916 | EA16 | EB16 | EC16 | ED16 | EE16 | EF16 |
| F016 | F116 | F216 | F316 | F416 | F516 | F616 | F716 |
| F816 | F916 | FA16 | FB16 | FC16 | FD16 | FE16 | FF16blank |

20P4B (20-PIN SDIP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

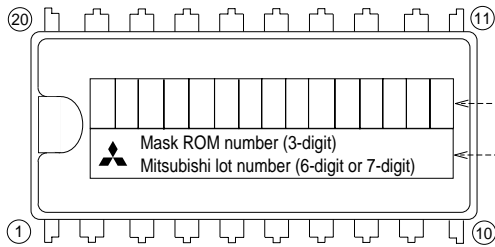
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number

Note: The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name and Mitsubishi lot number

Notes 1 : The mark field should be written right aligned.

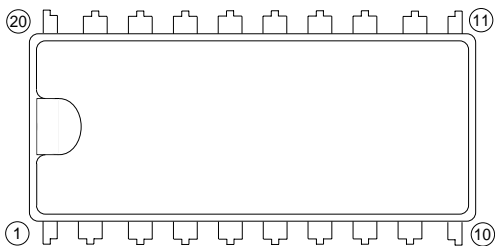
2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's Parts Number can be up to 13 characters: Only 0 to 9, A to Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note 1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.

Mitsubishi lot number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.

Please submit a clean original of the logo.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

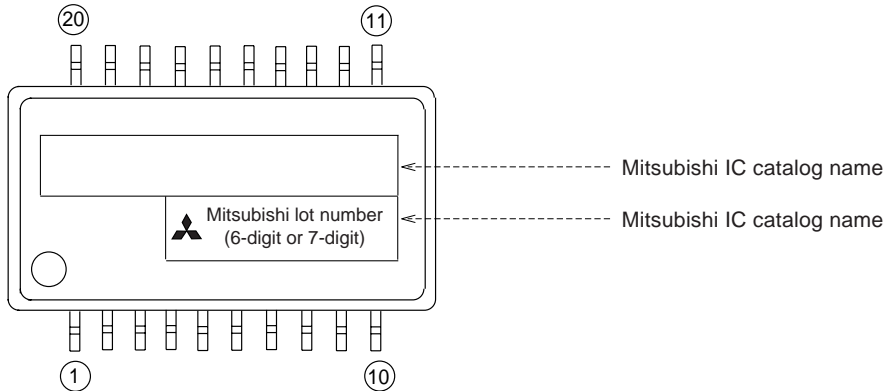
Special logo required

20P2Q-A (20-PIN SSOP) MARK SPECIFICATION FORM

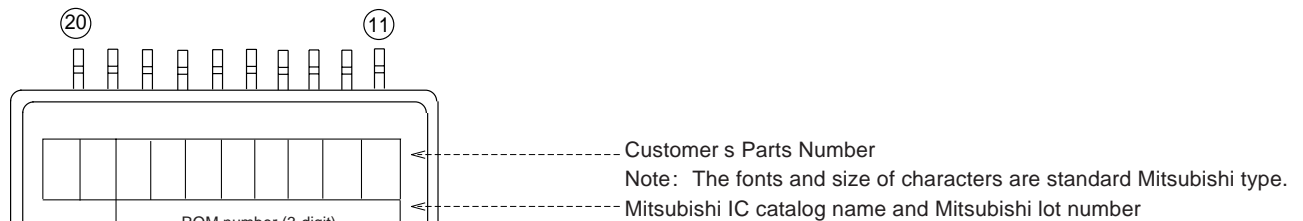
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



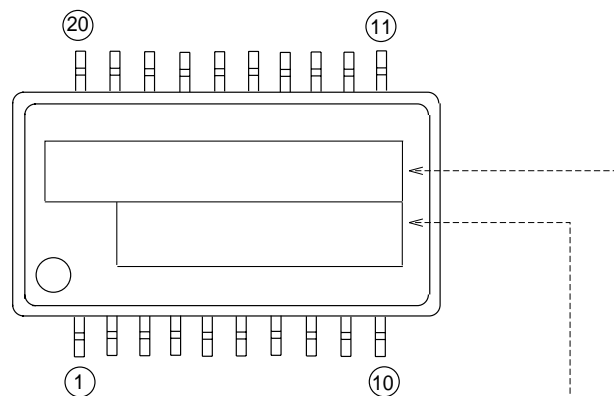
B. Customer's Parts Number + Mitsubishi IC Catalog Name



- Notes 1 : The mark field should be written right aligned.
 2 : The fonts and size of characters are standard Mitsubishi type.
 3 : Customer's Parts Number can be up to 10 characters: Only 0 to 9, A to Z, +, -, /, (,), &, ', . (period), and , (comma) are usable.
 4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



- Note 1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
 Mitsubishi lot number (4-digit) and Mask ROM number (3-digit) are always marked.
 2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
 Please submit a clean original of the logo.
 For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special logo required

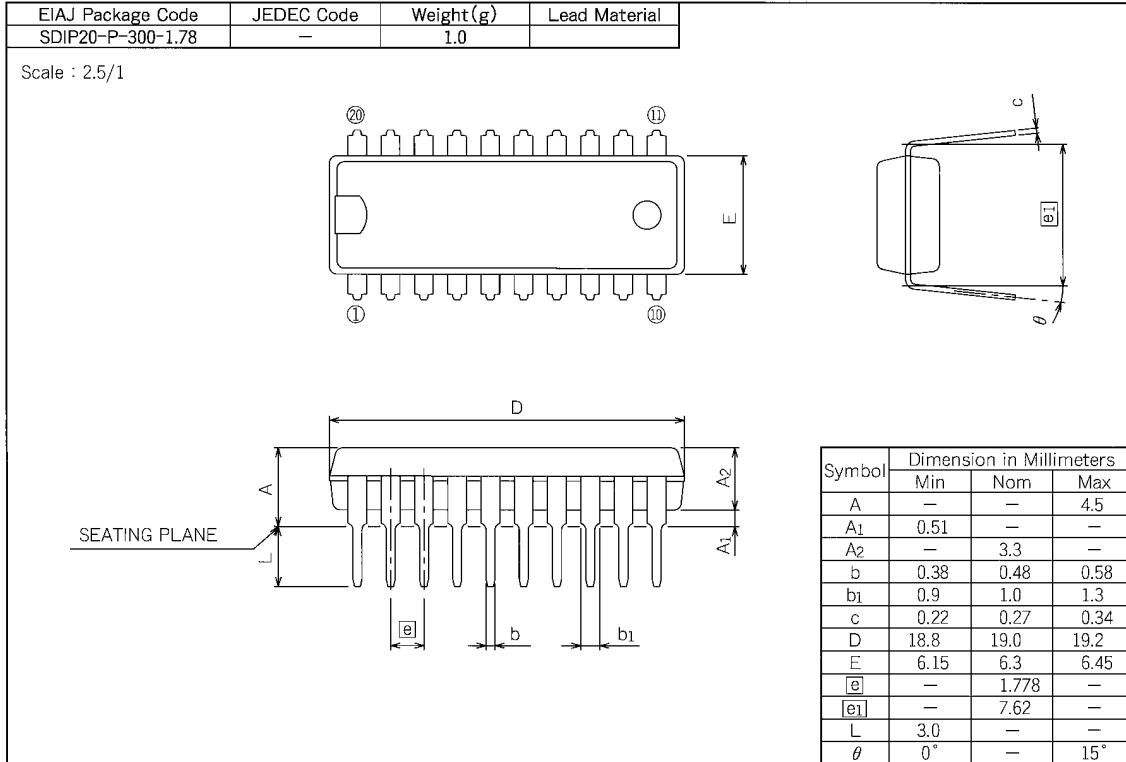
Special Mark (Customer's Trade Mark)

Mitsubishi IC catalog name

PACKAGE OUTLINE

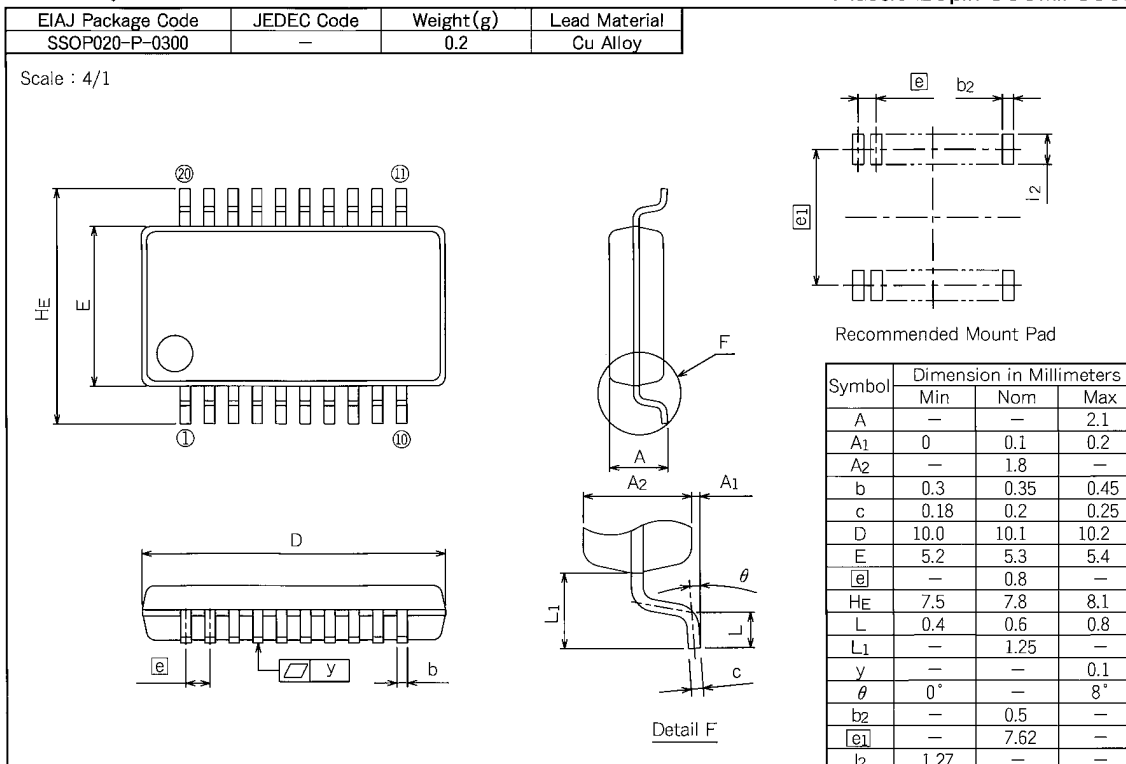
20P4B

Plastic 20pin 300mil SDIP



20P2Q-A

Plastic 20pin 300mil SSOP





Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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REVISION DESCRIPTION LIST

M35047-XXXSP/FP DATA SHEET

| Rev. No. | Revision Description | Rev. date |
|----------|--|-----------|
| 1.0 | First Edition | 980402 |
| 1.1 | P47 20P2Q-A (20-PIN SSOP) MARK SPECIFICATION FORM B: Note 4 added | 000707 |
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