

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

# MITSUBISHI MICROCOMPUTERS M37736EHLXXXHP

PROM VERSION OF M37736MHLXXXHP

## DESCRIPTION

The M37736EHLXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the PROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage, and the small package.

In the M37736MHLXXXHP, as the multiplex method of the external bus, either of 2 types can be selected.

The M37736EHLXXXHP has the same function as the M37736MHLXXXHP except that the built-in ROM is PROM. (Refer to the basic function blocks description.)

## FEATURES

- Number of basic instructions ..... 103
- Memory size      PROM ..... 124 Kbytes  
                       RAM ..... 3968 bytes

## ● Instruction execution time

The fastest instruction at 12 MHz frequency ..... 333 ns

● Single power supply ..... 2.7–5.5 V

● Low power dissipation (At 3 V supply voltage, 12 MHz frequency)  
 ..... 9 mW (Typ.)

● Interrupts ..... 19 types, 7 levels

● Multiple-function 16-bit timer ..... 5 + 3

● Serial I/O (UART or clock synchronous) ..... 3

● 10-bit A-D converter ..... 8-channel inputs

● 12-bit watchdog timer

● Programmable input/output, output  
 (ports P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10) ..... 84

● Clock generating circuit ..... 2 circuits built-in

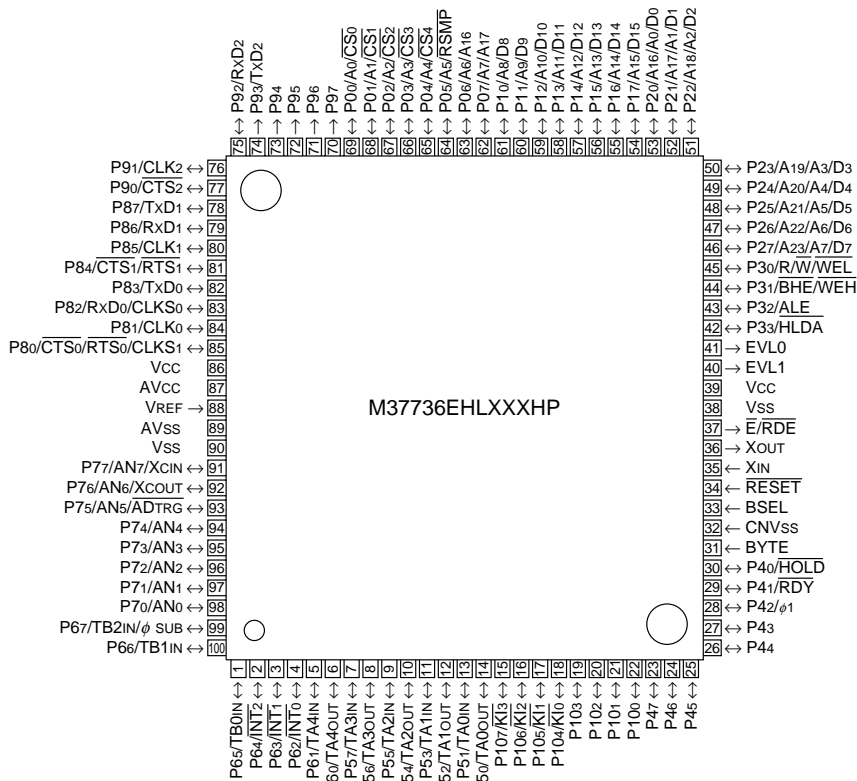
● Small package ..... 100-pin plastic molded fine-pitch QFP  
 (100P6Q-A; 0.5 mm lead pitch)

## APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and others.

Control devices for general industrial equipment such as communication equipment, and others.

## PIN CONFIGURATION (TOP VIEW)

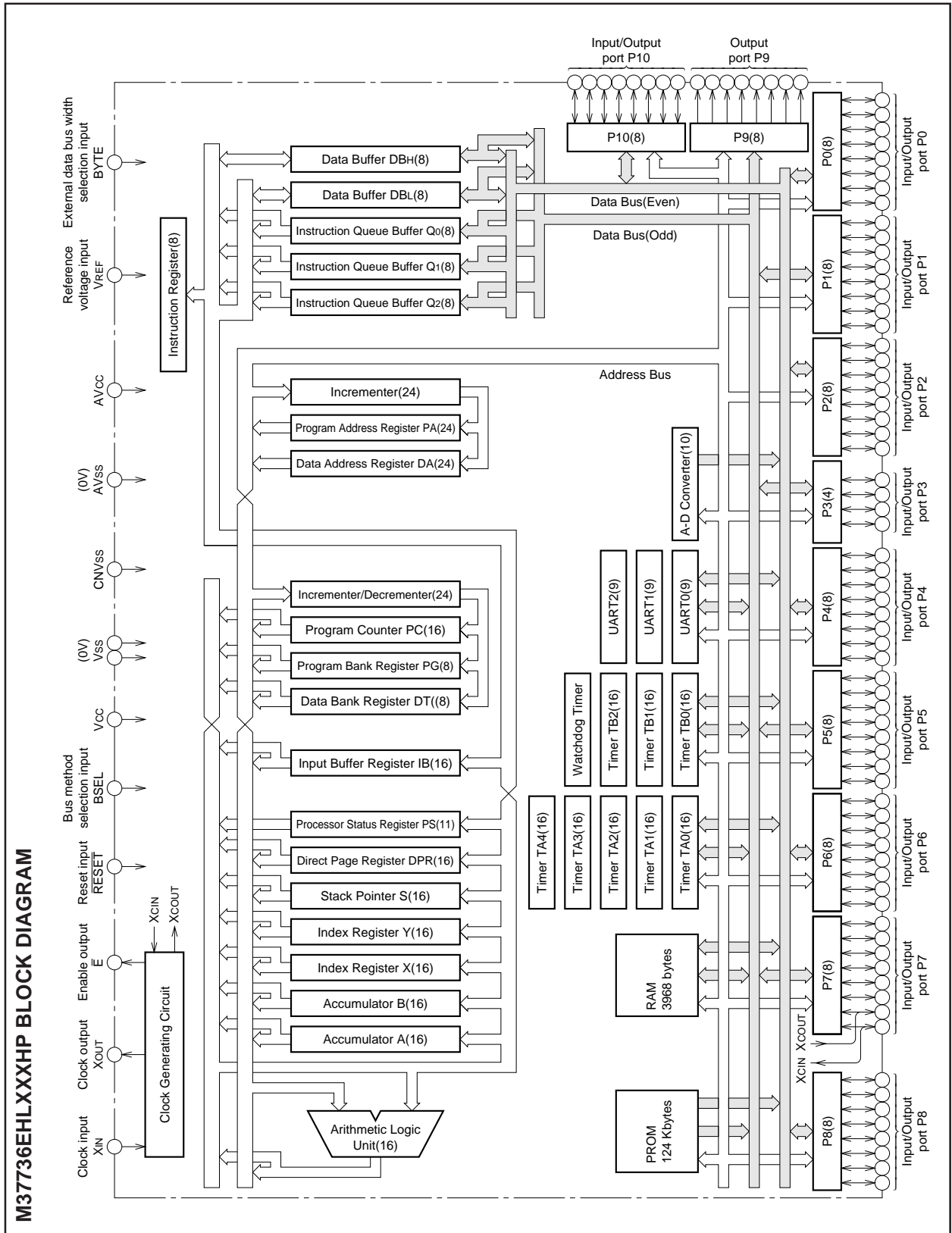


Outline 100P6Q-A

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**FUNCTIONS OF M37736EHLXXXHP**

| Parameter                    |                         | Functions  |
|------------------------------|-------------------------|--|
| Number of basic instructions |                         | 103  |
| Instruction execution time   |                         | 333 ns (the fastest instruction at external clock 12 MHz frequency)                              |
| Memory size                  | PROM                    | 124 Kbytes   |
|                              | RAM                     | 3968 bytes   |
| Input/Output ports           | P0 – P2, P4 – P8, P10   | 8-bit X 9  |
|                              | P3                      | 4-bit X 1  |
| Output port                  | P9                      | 8-bit X 1  |
| Multi-function timers        | TA0, TA1, TA2, TA3, TA4 | 16-bit X 5   |
|                              | TB0, TB1, TB2           | 16-bit X 3   |
| Serial I/O                   |                         | (UART or clock synchronous serial I/O) X 3   |
| A-D converter                |                         | 10-bit X 1 (8 channels)  |
| Watchdog timer               |                         | 12-bit X 1   |
| Interrupts                   |                         | 3 external types, 16 internal types<br>Each interrupt can be set to the priority level (0 – 7.)  |
| Clock generating circuit     |                         | 2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator) |
| Supply voltage               |                         | 2.7 – 5.5 V  |
| Power dissipation            |                         | 9 mW (at 3 V supply voltage, external clock 12 MHz frequency)                                    |
|                              |                         | 22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)                                 |
| Input/Output characteristic  | Input/Output voltage    | 5 V  |
|                              | Output current          | 5 mA   |
| Memory expansion             |                         | External bus mode A; maximum 16 Mbytes,<br>External bus mode B; maximum 1 Mbytes                 |
| Operating temperature range  |                         | –40 to 85 °C   |
| Device structure             |                         | CMOS high-performance silicon gate process   |
| Package                      |                         | 100-pin plastic molded fine-pitch QFP (100P6Q-A;0.5 mm lead pitch)                               |

**PIN DESCRIPTION**

| Pin                                 | Name                                    | Input/Output | Functions   |
|-------------------------------------|---|--------------|---|
| Vcc, Vss                            | Power source                            |              | Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.  |
| CNVss                               | CNVss input                             | Input        | This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.  |
| RESET                               | Reset input                             | Input        | When "L" level is applied to this pin, the microcomputer enters the reset state.  |
| XIN                                 | Clock input                             | Input        | These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.  |
| XOUT                                | Clock output                            | Output       |   |
| E                                   | Enable output                           | Output       | This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the external bus mode B and the memory expansion mode or the microprocessor mode, this pin output signal RDE.  |
| BYTE                                | External data bus width selection input | Input        | In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.  |
| BSEL                                | Bus method select input                 | Input        | In the memory expansion mode or the microprocessor mode, this pin determines the external bus mode. The bus mode becomes the external bus mode A when "H" signal is input, and the external bus mode B when "L" signal is input.  |
| AVcc, AVss                          | Analog power source input               |              | Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.   |
| VREF                                | Reference voltage input                 | Input        | This is reference voltage input pin for the A-D converter.  |
| P0 <sub>0</sub> – P0 <sub>7</sub>   | I/O port P0                             | I/O          | In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset.<br><br>In the memory expansion mode or the microprocessor mode, these pins output address (A <sub>0</sub> – A <sub>7</sub> ) at the external bus mode A, and these pins output signals CS <sub>0</sub> – CS <sub>4</sub> and RSM <sub>P</sub> , and addresses (A <sub>16</sub> , A <sub>17</sub> ) at the external bus mode B. |
| P1 <sub>0</sub> – P1 <sub>7</sub>   | I/O port P1                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D <sub>8</sub> – D <sub>15</sub> ) is input/output or an address (A <sub>8</sub> – A <sub>15</sub> ) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A <sub>8</sub> – A <sub>15</sub> ) is output.  |
| P2 <sub>0</sub> – P2 <sub>7</sub>   | I/O port P2                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D <sub>0</sub> – D <sub>7</sub> ) is input/output or an address is output. When using the external bus mode A, the address is A <sub>16</sub> – A <sub>23</sub> . When using the external bus mode B, the address is A <sub>0</sub> – A <sub>7</sub> .   |
| P3 <sub>0</sub> – P3 <sub>3</sub>   | I/O port P3                             | I/O          | In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output at the external bus mode A, and WEL, WEH, ALE, and HLDA signals are output at the external bus mode B.   |
| P4 <sub>0</sub> – P4 <sub>7</sub>   | I/O port P4                             | I/O          | In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P4 <sub>0</sub> , P4 <sub>1</sub> , and P4 <sub>2</sub> become HOLD and RDY input pins, and a clock φ <sub>1</sub> output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P4 <sub>2</sub> can be selected as an I/O port.   |
| P5 <sub>0</sub> – P5 <sub>7</sub>   | I/O port P5                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3.  |
| P6 <sub>0</sub> – P6 <sub>7</sub>   | I/O port P6                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT <sub>0</sub> – INT <sub>2</sub> ) and input pins for timers B0 to B2. P6 <sub>7</sub> also functions as sub-clock φ <sub>SUB</sub> output pin.   |
| P7 <sub>0</sub> – P7 <sub>7</sub>   | I/O port P7                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. Additionally, P7 <sub>6</sub> and P7 <sub>7</sub> have the function as the output pin (XCOUT) and the input pin (XCIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P7 <sub>6</sub> and P7 <sub>7</sub> are used as the XCOUT and XCIN pins, connect a resonator or an oscillator between the both.  |
| P8 <sub>0</sub> – P8 <sub>7</sub>   | I/O port P8                             | I/O          | In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.  |
| P9 <sub>0</sub> – P9 <sub>7</sub>   | Output port P9                          | Output       | Port P9 is an 8-bit I/O port. These ports are floating when reset. When writing to the port latch, these ports become the output mode. P9 <sub>0</sub> – P9 <sub>3</sub> also function as I/O port for UART 2.  |
| P10 <sub>0</sub> – P10 <sub>7</sub> | I/O port P10                            | I/O          | In addition to having the same functions as port P0 in the single-chip mode. P10 <sub>4</sub> – P10 <sub>7</sub> also function as input pins for key input interrupt input (KI <sub>0</sub> – KI <sub>3</sub> ).  |
| EVL0, EVL1                          | ————                                    | Output       | These pins should be left open.   |

## BASIC FUNCTION BLOCKS

The M37736EHLXXXHP has the same functions as the M37736MHBXXXGP except for the following :

- (1) The built-in ROM is PROM.
- (2) The package is different.
- (3) The reset circuit is different.

Refer to the section on the M37736MHBXXXGP.

## RESET CIRCUIT

The microcomputer is released from the reset state when the  $\overline{\text{RESET}}$  pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A<sub>23</sub> – A<sub>16</sub> to 00<sub>16</sub>, A<sub>15</sub> – A<sub>8</sub> to the contents of address FFFF<sub>16</sub>, and A<sub>7</sub> – A<sub>0</sub> to the contents of address FFFE<sub>16</sub>. Figure 1 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

The status of the internal registers during reset is the same as the M37736MHBXXXGP's.

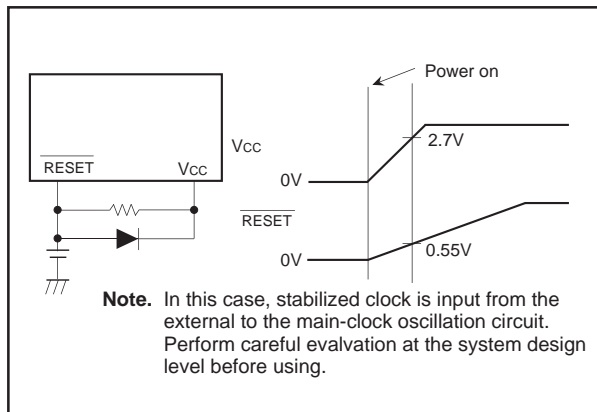


Fig. 1 Example of a reset circuit

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**PIN DESCRIPTION (EPROM MODE)**

| Pin         | Name                     | Input/Output | Functions  |
|-------------|--------------------------|--------------|--|
| VCC, VSS    | Power supply             |              | Supply 5V±10% to Vcc and 0V to Vss.  |
| CNVSS       | VPP input                | Input        | Connect to VPP when programming or verifying.  |
| BYTE        | VPP input                | Input        | Connect to VPP when programming or verifying.  |
| RESET       | Reset input              | Input        | Connect to Vss.  |
| XIN         | Clock input              | Input        | Connect a ceramic resonator between XIN and XOUT.  |
| XOUT        | Clock output             | Output       |  |
| E           | Enable output            | Output       | Keep open.   |
| AVCC, AVSS  | Analog supply input      |              | Connect AVCC to Vcc and AVSS to Vss.   |
| VREF        | Reference voltage input  | Input        | Connect to Vss.  |
| P00 – P07   | Address input (A0 – A7)  | Input        | Port P0 functions as the lower 8 bits address input (A0 – A7).   |
| P10 – P17   | Address input (A8 – A15) | Input        | Port P1 functions as the higher 8 bits address input (A8 – A15).   |
| P20 – P27   | Data I/O (D0 – D7)       | I/O          | Port P2 functions as the 8 bits data bus(D0 – D7).   |
| P30         | Address input (A16)      | Input        | P30 functions as the most significant bit address input (A16).   |
| P31 – P33   | Input port P3            | Input        | Connect to Vss.  |
| P40 – P47   | Input port P4            | Input        | Connect to Vss.  |
| P50 – P57   | Control signal input     | Input        | P50, P51 and P52 function as PGM, OE and CE input pins respectively. Connect P53, P54, P55 and P56 to Vcc. Connect P57 to Vss. |
| P60 – P67   | Input port P6            | Input        | Connect to Vss.  |
| P70 – P77   | Input port P7            | Input        | Connect to Vss.  |
| P80 – P87   | Input port P8            | Input        | Connect to Vss.  |
| P90 – P97   | Input port P9            | Input        | Connect to Vss.  |
| P100 – P107 | Input port P10           | Input        | Connect to Vss.  |
| BSEL        | —                        | Input        | Connect to Vcc.  |
| EVL0,EVL1   | —                        | Output       | Keep open.   |

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**EPROM MODE**

The M37736EHLXXXHP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 2 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss and BYTE are used for the EPROM (equivalent to the

M5M27C101K). When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 01000<sub>16</sub> – 1FFFF<sub>16</sub>.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

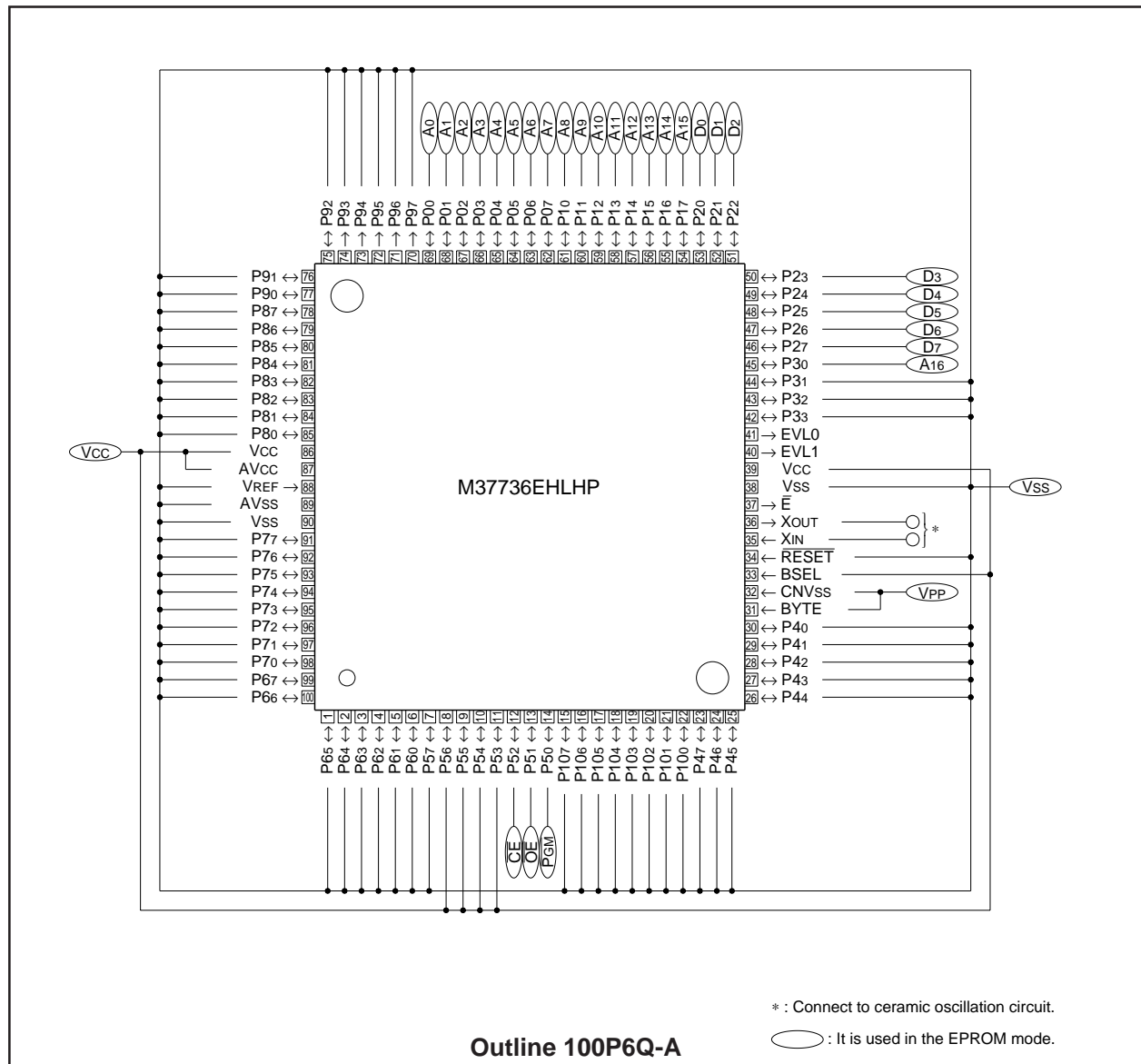


Fig. 2 Pin connection in EPROM mode

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Table 1 Pin function in EPROM mode

|                        | M37736EHLXXXHP                | M5M27C101K                       |
|------------------------|-------------------------------|----------------------------------|
| V <sub>CC</sub>        | V <sub>CC</sub>               | V <sub>CC</sub>                  |
| V <sub>PP</sub>        | CNV <sub>SS</sub> , BYTE      | V <sub>PP</sub>                  |
| V <sub>SS</sub>        | V <sub>SS</sub>               | V <sub>SS</sub>                  |
| Address input          | Ports P0, P1, P3 <sub>0</sub> | A <sub>0</sub> – A <sub>16</sub> |
| Data I/O               | Port P2                       | D <sub>0</sub> – D <sub>7</sub>  |
| $\overline{\text{CE}}$ | P5 <sub>2</sub>               | $\overline{\text{CE}}$           |
| $\overline{\text{OE}}$ | P5 <sub>1</sub>               | $\overline{\text{OE}}$           |
| PGM                    | P5 <sub>0</sub>               | PGM                              |



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**FUNCTION IN EPROM MODE**  
**1M mode (equivalent to the M5M27C101K)**

**Reading**

To read the EPROM, set the  $\overline{CE}$  and  $\overline{OE}$  pins to a "L" level. Input the address of the data (A0 – A16) to be read, and the data will be output to the I/O pins D0 – D7. The data I/O pins will be floating when either the  $\overline{CE}$  or  $\overline{OE}$  pins are in the "H" state.

**Programming**

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the  $\overline{CE}$  pin to a "L" level and the  $\overline{OE}$  pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the VPP pin. The address to be programmed to is selected with pins A0 – A16, and the data to be programmed is input to pins D0 – D7. Set the  $\overline{PGM}$  pin to a "L" level to being programming.

**Programming operation**

To program the M37736EHLXXXHP, first set VCC = 6 V, VPP = 12.5 V, and set the address to 0100016. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 X X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with VCC = VPP = 5 V (or VCC = VPP = 5.5 V).

Table 2. I/O signal in each mode

| Mode               | Pin             |                 |                  |        |     |          |
|--------------------|-----------------|-----------------|------------------|--------|-----|----------|
|                    | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | VPP    | VCC | Data I/O |
| Read-out           | VIL             | VIL             | X                | 5 V    | 5 V | Output   |
| Output             | VIL             | VIH             | X                | 5 V    | 5 V | Floating |
| Disable            | VIH             | X               | X                | 5 V    | 5 V | Floating |
| Programming        | VIL             | VIH             | VIL              | 12.5 V | 6 V | Input    |
| Programming Verify | VIL             | VIL             | VIH              | 12.5 V | 6 V | Output   |
| Program Disable    | VIH             | VIH             | VIH              | 12.5 V | 6 V | Floating |

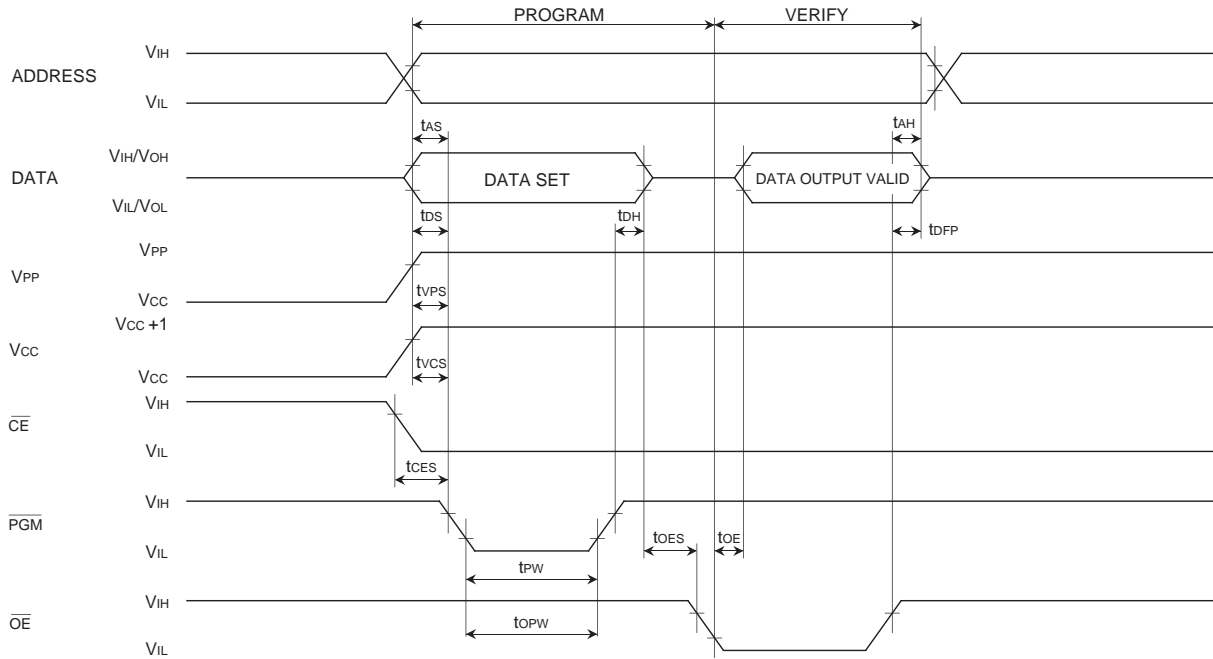
**Note 1** : An X indicates either VIL or VIH.

**Programming operation (equivalent to the M5M27C101K)**

AC ELECTRICAL CHARACTERISTICS (Ta = 25 ± 5 °C, VCC = 6 V ± 0.25 V, VPP = 12.5 ± 0.3 V, unless otherwise noted)

| Symbol | Parameter                                 | Test conditions | Limits |      |      | Unit |
|--------|---|-----------------|--------|------|------|------|
|        |   |                 | Min.   | Typ. | Max. |      |
| tAS    | Address setup time                        |                 | 2      |      |      | μs   |
| toES   | $\overline{OE}$ setup time                |                 | 2      |      |      | μs   |
| tDS    | Data setup time                           |                 | 2      |      |      | μs   |
| tAH    | Address hold time                         |                 | 0      |      |      | μs   |
| tDH    | Data hold time                            |                 | 2      |      |      | μs   |
| tDFP   | Output enable to output float delay       |                 | 0      |      | 130  | ns   |
| tvCS   | VCC setup time                            |                 | 2      |      |      | μs   |
| tvPS   | VPP setup time                            |                 | 2      |      |      | μs   |
| tpW    | $\overline{PGM}$ pulse width              |                 | 0.19   | 0.2  | 0.21 | ms   |
| topW   | $\overline{PGM}$ over program pulse width |                 | 0.19   |      | 5.25 | ms   |
| tCES   | $\overline{CE}$ setup time                |                 | 2      |      |      | μs   |
| toE    | Data valid from $\overline{OE}$           |                 |        |      | 150  | ns   |

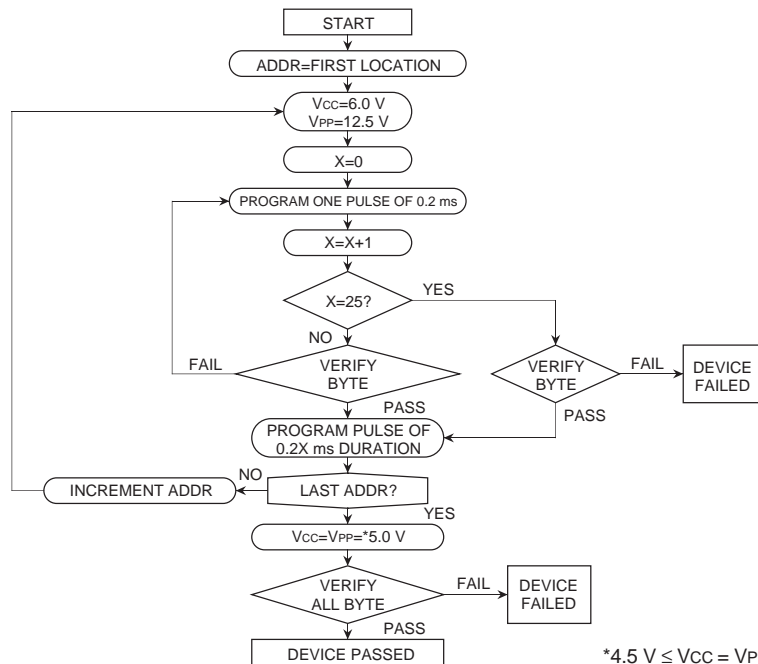
**AC waveforms**



Test conditions for A.C. characteristics

Input voltage :  $V_{IL} = 0.45 \text{ V}$ ,  $V_{IH} = 2.4 \text{ V}$   
 Input rise and fall times (10% – 90%) :  $\leq 20 \text{ ns}$   
 Reference voltage at timing measurement : Input, Output  
 "L" = 0.8 V, "H" = 2 V

**Programming algorithm flow chart**

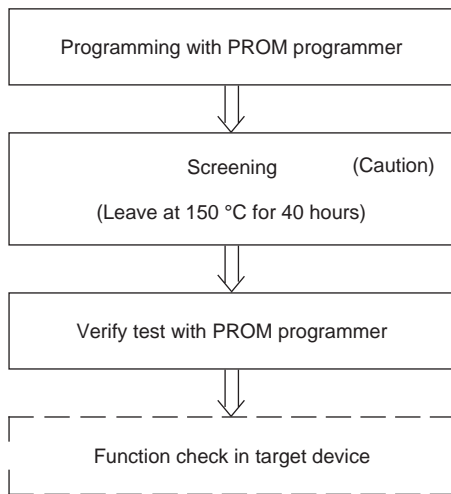


\*4.5 V ≤ VCC = VPP ≤ 5.5 V

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**SAFETY INSTRUCTIONS**

- (1) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (2) The programmable M37736EHLHP that is shipped in blank is also provided. For the M37736EHLHP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

**ADDRESSING MODES**

The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

**MACHINE INSTRUCTION LIST**

The M37736EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

**DATA REQUIRED FOR PROM ORDERING**

Please send the following data for writing to PROM.

- (1) M37736EHLXXXHP writing to PROM order confirmation form
- (2) 100P6Q mark specification form (100P6D mark specification form is substituted.)
- (3) ROM data (EPROM 3 sets)

**ABSOLUTE MAXIMUM RATINGS**

| Symbol           | Parameter  | Conditions             | Ratings                       | Unit |
|------------------|--|------------------------|-------------------------------|------|
| V <sub>cc</sub>  | Power source voltage   |                        | -0.3 to +7                    | V    |
| AV <sub>cc</sub> | Analog power source voltage  |                        | -0.3 to +7                    | V    |
| V <sub>i</sub>   | Input voltage RESET, CNV <sub>ss</sub> , BYTE  |                        | -0.3 to +12(Note)             | V    |
| V <sub>i</sub>   | Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, V <sub>REF</sub> , X <sub>IN</sub> , BSEL |                        | -0.3 to V <sub>cc</sub> + 0.3 | V    |
| V <sub>o</sub>   | Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107, X <sub>OUT</sub> , E                     |                        | -0.3 to V <sub>cc</sub> + 0.3 | V    |
| P <sub>d</sub>   | Power dissipation  | T <sub>a</sub> = 25 °C | 200                           | mW   |
| T <sub>opr</sub> | Operating temperature  |                        | -40 to +85                    | °C   |
| T <sub>stg</sub> | Storage temperature  |                        | -65 to +150                   | °C   |

**Note.** When the EPROM is programmed, input voltage of pins CNV<sub>ss</sub> and BYTE is 13 V respectively.

**RECOMMENDED OPERATING CONDITIONS** (V<sub>cc</sub> = 2.7 – 5.5 V, T<sub>a</sub> = -40 to +85 °C, unless otherwise noted)

| Symbol                | Parameter  |  | Limits              |                 |                     | Unit |
|-----------------------|--|--|---------------------|-----------------|---------------------|------|
|                       |  |  | Min.                | Typ.            | Max.                |      |
| V <sub>cc</sub>       | Power source voltage   | f(X <sub>IN</sub> ) : Operating                                  | 2.7                 |                 | 5.5                 | V    |
|                       |  | f(X <sub>IN</sub> ) : Stopped, f(X <sub>CIN</sub> ) = 32.768 kHz | 2.7                 |                 | 5.5                 |      |
| AV <sub>cc</sub>      | Analog power source voltage  |  |                     | V <sub>cc</sub> |                     | V    |
| V <sub>ss</sub>       | Power source voltage   |  |                     | 0               |                     | V    |
| AV <sub>ss</sub>      | Analog power source voltage  |  |                     | 0               |                     | V    |
| V <sub>IH</sub>       | High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, BSEL, X <sub>CIN</sub> (Note 3) |  | 0.8 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IH</sub>       | High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)  |  | 0.8 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IH</sub>       | High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)   |  | 0.5 V <sub>cc</sub> |                 | V <sub>cc</sub>     | V    |
| V <sub>IL</sub>       | Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, BSEL, X <sub>CIN</sub> (Note 3)  |  | 0                   |                 | 0.2V <sub>cc</sub>  | V    |
| V <sub>IL</sub>       | Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)   |  | 0                   |                 | 0.2V <sub>cc</sub>  | V    |
| V <sub>IL</sub>       | Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)  |  | 0                   |                 | 0.16V <sub>cc</sub> | V    |
| I <sub>OH(peak)</sub> | High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107   |  |                     |                 | -10                 | mA   |
| I <sub>OH(avg)</sub>  | High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107  |  |                     |                 | -5                  | mA   |
| I <sub>OL(peak)</sub> | Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107  |  |                     |                 | 10                  | mA   |
| I <sub>OL(peak)</sub> | Low-level peak output current P44 – P47, P100 – P103   |  |                     |                 | 16                  | mA   |
| I <sub>OL(avg)</sub>  | Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107   |  |                     |                 | 5                   | mA   |
| I <sub>OL(avg)</sub>  | Low-level average output current P44 – P47, P100 – P103  |  |                     |                 | 12                  | mA   |
| f(X <sub>IN</sub> )   | Main-clock oscillation frequency (Note 4)  |  |                     |                 | 12                  | MHz  |
| f(X <sub>CIN</sub> )  | Sub-clock oscillation frequency  |  |                     | 32.768          | 50                  | kHz  |

- Notes**
1. Average output current is the average value of a 100 ms interval.
  2. The sum of I<sub>OL(peak)</sub> for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I<sub>OH(peak)</sub> for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I<sub>OL(peak)</sub> for ports P4, P5, P6, P7, and P10 must be 100 mA or less, and the sum of I<sub>OH(peak)</sub> for ports P4, P5, P6, P7, and P10 must be 80 mA or less.
  3. Limits V<sub>IH</sub> and V<sub>IL</sub> for X<sub>CIN</sub> are applied when the sub clock external input selection bit = "1".
  4. The maximum value of f(X<sub>IN</sub>) = 6 MHz when the main clock division selection bit = "1".

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**MITSUBISHI MICROCOMPUTERS**  
**M37736EHLXXXHP**

PROM VERSION OF M37736MHLXXXHP

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40$  to  $+85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 12\text{ MHz}$ , unless otherwise noted)

| Symbol                            | Parameter   | Test conditions  | Limits                |       |       | Unit    |         |
|-----------------------------------|---|--|-----------------------|-------|-------|---------|---------|
|                                   |   |  | Min.                  | Typ.  | Max.  |         |         |
| V <sub>OH</sub>                   | High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33,<br>P40 – P47, P50 – P57, P60 – P67, P70 – P77,<br>P80 – P87, P90 – P97, P100 – P107   | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –10 mA          | 3                     |       |       | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OH</sub> = –1 mA           | 2.5                   |       |       |         |         |
| V <sub>OH</sub>                   | High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33  | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –400 $\mu$ A    | 4.7                   |       |       | V       |         |
| V <sub>OH</sub>                   | High-level output voltage P30 – P32   | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –10 mA          | 3.1                   |       |       | V       |         |
|                                   |   | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –400 $\mu$ A    | 4.8                   |       |       |         |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OH</sub> = –1 mA           | 2.6                   |       |       |         |         |
| V <sub>OH</sub>                   | High-level output voltage $\bar{E}$   | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –10 mA          | 3.4                   |       |       | V       |         |
|                                   |   | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –400 $\mu$ A    | 4.8                   |       |       |         |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OH</sub> = –1 mA           | 2.6                   |       |       |         |         |
| V <sub>OL</sub>                   | Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33,<br>P40 – P43, P50 – P57, P60 – P67, P70 – P77,<br>P80 – P87, P90 – P97, P104 – P107  | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 10 mA           |                       |       | 2     | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 1 mA            |                       |       | 0.5   |         |         |
| V <sub>OL</sub>                   | Low-level output voltage P44 – P47, P100 – P103   | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 16 mA           |                       |       | 1.8   | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 10 mA           |                       |       | 1.5   |         |         |
| V <sub>OL</sub>                   | Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33   | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 2 mA            |                       |       | 0.45  | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 10 mA           |                       |       | 1.9   |         |         |
| V <sub>OL</sub>                   | Low-level output voltage P30 – P32  | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 10 mA           |                       |       | 0.43  | V       |         |
|                                   |   | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 2 mA            |                       |       | 0.4   |         |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 1 mA            |                       |       | 1.6   |         |         |
| V <sub>OL</sub>                   | Low-level output voltage $\bar{E}$  | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 10 mA           |                       |       | 0.4   | V       |         |
|                                   |   | V <sub>CC</sub> = 5 V, I <sub>OL</sub> = 2 mA            |                       |       | 0.4   |         |         |
|                                   |   | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 1 mA            |                       |       | 0.4   |         |         |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis HOLD, RDY, TA0IN – TA4IN, TB0IN – TB2IN,<br>INT0 – INT2, ADTRG, CTS0, CTS1, CTS2, CLK0,<br>CLK1, CLK2, K10 – K13   | V <sub>CC</sub> = 5 V                                    | 0.4                   |       | 1     | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V                                    | 0.1                   |       | 0.7   |         |         |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis $\bar{\text{RESET}}$   | V <sub>CC</sub> = 5 V                                    | 0.2                   |       | 0.5   | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V                                    | 0.1                   |       | 0.4   |         |         |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis X <sub>IN</sub>  | V <sub>CC</sub> = 5 V                                    | 0.1                   |       | 0.4   | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V                                    | 0.06                  |       | 0.26  |         |         |
| V <sub>T+</sub> – V <sub>T–</sub> | Hysteresis X <sub>CIN</sub> (When external clock is input)  | V <sub>CC</sub> = 5 V                                    | 0.1                   |       | 0.4   | V       |         |
|                                   |   | V <sub>CC</sub> = 3 V                                    | 0.06                  |       | 0.26  |         |         |
| I <sub>IH</sub>                   | High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33,<br>P40 – P47, P50 – P57, P60 – P67, P70 – P77,<br>P80 – P87, P90 – P92, P100 – P107, X <sub>IN</sub> , $\bar{\text{RESET}}$ ,<br>CNV <sub>SS</sub> , BYTE, BSEL          | V <sub>CC</sub> = 5 V, V <sub>I</sub> = 5 V              |                       |       | 5     | $\mu$ A |         |
|                                   |   | V <sub>CC</sub> = 3 V, V <sub>I</sub> = 3 V              |                       |       | 4     |         |         |
| I <sub>IL</sub>                   | Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33,<br>P40 – P47, P50 – P53, P60, P61, P65 – P67,<br>P70 – P77, P80 – P87, P90 – P92, P100 – P103,<br>X <sub>IN</sub> , $\bar{\text{RESET}}$ , CNV <sub>SS</sub> , BYTE, BSEL | V <sub>CC</sub> = 5 V, V <sub>I</sub> = 0 V              |                       |       | –5    | $\mu$ A |         |
|                                   |   | V <sub>CC</sub> = 3 V, V <sub>I</sub> = 0 V              |                       |       | –4    |         |         |
| I <sub>IL</sub>                   | Low-level input current P62 – P64, P104 – P107  | V <sub>I</sub> = 0 V,<br>without a pull-up<br>transistor | V <sub>CC</sub> = 5 V |       |       | –5      | $\mu$ A |
|                                   |   |  | V <sub>CC</sub> = 3 V |       |       | –4      |         |
|                                   |   | V <sub>I</sub> = 0 V,<br>with a pull-up<br>transistor    | V <sub>CC</sub> = 5 V | –0.25 | –0.5  | –1.0    | mA      |
|                                   |   |  | V <sub>CC</sub> = 3 V | –0.08 | –0.18 | –0.35   |         |
| V <sub>RAM</sub>                  | RAM hold voltage  | When clock is stopped.                                   | 2                     |       |       | V       |         |

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$ , unless otherwise noted)

| Symbol          | Parameter            | Test conditions   | Limits  |      |      | Unit |    |    |
|-----------------|----------------------|---|---|------|------|------|----|----|
|                 |                      |   | Min.  | Typ. | Max. |      |    |    |
| I <sub>CC</sub> | Power source current | When single-chip mode, output pins are open, and other pins are V <sub>SS</sub> . | V <sub>CC</sub> = 5 V,<br>f(X <sub>IN</sub> ) = 12 MHz (square waveform),<br>f(f <sub>2</sub> ) = 6 MHz,<br>f(X <sub>CIN</sub> ) = 32.768 kHz,<br>in operating (Note 1) |      | 4.5  | 9    | mA |    |
|                 |                      |   | V <sub>CC</sub> = 3 V,<br>f(X <sub>IN</sub> ) = 12 MHz (square waveform),<br>f(f <sub>2</sub> ) = 6 MHz,<br>f(X <sub>CIN</sub> ) = 32.768 kHz,<br>in operating (Note 1) |      | 3    | 6    | mA |    |
|                 |                      |   | V <sub>CC</sub> = 3 V,<br>f(X <sub>IN</sub> ) = 12 MHz (square waveform),<br>f(f <sub>2</sub> ) = 0.75 MHz,<br>f(X <sub>CIN</sub> ) : Stopped,<br>in operating          |      | 0.4  | 0.8  | mA |    |
|                 |                      |   | V <sub>CC</sub> = 3 V,<br>f(X <sub>IN</sub> ) = 12 MHz (square waveform),<br>f(X <sub>CIN</sub> ) = 32.768 kHz,<br>when a WIT instruction is executed (Note 2)          |      | 6    | 12   | μA |    |
|                 |                      |   | V <sub>CC</sub> = 3 V,<br>f(X <sub>IN</sub> ) : Stopped,<br>f(X <sub>CIN</sub> ) = 32.768 kHz,<br>in operating (Note 3)   |      | 30   | 60   | μA |    |
|                 |                      |   | V <sub>CC</sub> = 3 V,<br>f(X <sub>IN</sub> ) : Stopped,<br>f(X <sub>CIN</sub> ) = 32.768 kHz,<br>when a WIT instruction is executed (Note 4)                           |      | 3    | 6    | μA |    |
|                 |                      |   | T <sub>a</sub> = 25 °C,<br>when clock is stopped  |      |      |      | 1  | μA |
|                 |                      |   | T <sub>a</sub> = 85 °C,<br>when clock is stopped  |      |      |      | 20 | μA |

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
  2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
  3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
  4. This applies when the X<sub>COUT</sub> drivability selection bit = "0" and the system clock stop bit at wait state = "1".

**A-D CONVERTER CHARACTERISTICS**

( $V_{CC} = AV_{CC} = 5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 12\text{ MHz}$ , unless otherwise noted (Note))

| Symbol            | Parameter            | Test conditions                    | Limits |      |                  | Unit |
|-------------------|----------------------|------------------------------------|--------|------|------------------|------|
|                   |                      |                                    | Min.   | Typ. | Max.             |      |
| —                 | Resolution           | V <sub>REF</sub> = V <sub>CC</sub> |        |      | 10               | Bits |
| —                 | Absolute accuracy    | V <sub>REF</sub> = V <sub>CC</sub> |        |      | ± 3              | LSB  |
| RLADDER           | Ladder resistance    | V <sub>REF</sub> = V <sub>CC</sub> | 10     |      | 25               | kΩ   |
| t <sub>CONV</sub> | Conversion time      |                                    | 19.6   |      |                  | μs   |
| V <sub>REF</sub>  | Reference voltage    |                                    | 2.7    |      | V <sub>CC</sub>  | V    |
| V <sub>IA</sub>   | Analog input voltage |                                    | 0      |      | V <sub>REF</sub> | V    |

**Note.** This applies when the main clock division selection bit = "0" and f(f<sub>2</sub>) = 6 MHz.

**TIMING REQUIREMENTS** ( $V_{CC} = 2.7 - 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 12 \text{ MHz}$ , unless otherwise noted (Note 1))

**Notes 1.** This applies when the main clock division selection bit = "0" and  $f(f_2) = 6 \text{ MHz}$ .

**2.** Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

**External clock input**

| Symbol     | Parameter  | Limits |      | Unit |
|------------|--|--------|------|------|
|            |  | Min.   | Max. |      |
| $t_c$      | External clock input cycle time (Note 3)             | 83     |      | ns   |
| $t_{w(H)}$ | External clock input high-level pulse width (Note 4) | 33     |      | ns   |
| $t_{w(L)}$ | External clock input low-level pulse width (Note 4)  | 33     |      | ns   |
| $t_r$      | External clock rise time                             |        | 15   | ns   |
| $t_f$      | External clock fall time                             |        | 15   | ns   |

**Notes 3.** When the main clock division selection bit = "1", the minimum value of  $t_c = 166 \text{ ns}$ .

**4.** When the main clock division selection bit = "1", values of  $t_{w(H)} / t_c$  and  $t_{w(L)} / t_c$  must be set to values from 0.45 through 0.55.

**Single-chip mode**

| Symbol           | Parameter                 | Limits |      | Unit |
|------------------|---------------------------|--------|------|------|
|                  |                           | Min.   | Max. |      |
| $t_{su(P0D-E)}$  | Port P0 input setup time  | 200    |      | ns   |
| $t_{su(P1D-E)}$  | Port P1 input setup time  | 200    |      | ns   |
| $t_{su(P2D-E)}$  | Port P2 input setup time  | 200    |      | ns   |
| $t_{su(P3D-E)}$  | Port P3 input setup time  | 200    |      | ns   |
| $t_{su(P4D-E)}$  | Port P4 input setup time  | 200    |      | ns   |
| $t_{su(P5D-E)}$  | Port P5 input setup time  | 200    |      | ns   |
| $t_{su(P6D-E)}$  | Port P6 input setup time  | 200    |      | ns   |
| $t_{su(P7D-E)}$  | Port P7 input setup time  | 200    |      | ns   |
| $t_{su(P8D-E)}$  | Port P8 input setup time  | 200    |      | ns   |
| $t_{su(P10D-E)}$ | Port P10 input setup time | 200    |      | ns   |
| $t_{h(E-P0D)}$   | Port P0 input hold time   | 0      |      | ns   |
| $t_{h(E-P1D)}$   | Port P1 input hold time   | 0      |      | ns   |
| $t_{h(E-P2D)}$   | Port P2 input hold time   | 0      |      | ns   |
| $t_{h(E-P3D)}$   | Port P3 input hold time   | 0      |      | ns   |
| $t_{h(E-P4D)}$   | Port P4 input hold time   | 0      |      | ns   |
| $t_{h(E-P5D)}$   | Port P5 input hold time   | 0      |      | ns   |
| $t_{h(E-P6D)}$   | Port P6 input hold time   | 0      |      | ns   |
| $t_{h(E-P7D)}$   | Port P7 input hold time   | 0      |      | ns   |
| $t_{h(E-P8D)}$   | Port P8 input hold time   | 0      |      | ns   |
| $t_{h(E-P10D)}$  | Port P10 input hold time  | 0      |      | ns   |

**Memory expansion mode and microprocessor mode**

| Symbol                | Parameter                                   | Limits |      | Unit |
|-----------------------|---|--------|------|------|
|                       |   | Min.   | Max. |      |
| $t_{su(D-E)}$         | Data input setup time (external bus mode A) | 50     |      | ns   |
| $t_{su(D-RDE)}$       | Data input setup time (external bus mode B) | 50     |      | ns   |
| $t_{su(RDY-\phi_1)}$  | RDY input setup time                        | 80     |      | ns   |
| $t_{su(HOLD-\phi_1)}$ | HOLD input setup time                       | 80     |      | ns   |
| $t_{h(E-D)}$          | Data input hold time (external bus mode A)  | 0      |      | ns   |
| $t_{h(RDE-D)}$        | Data input hold time (external bus mode B)  | 0      |      | ns   |
| $t_{h(\phi_1-RDY)}$   | RDY input hold time                         | 0      |      | ns   |
| $t_{h(\phi_1-HOLD)}$  | HOLD input hold time                        | 0      |      | ns   |

**Timer A input** (Count input in event counter mode)

| Symbol               | Parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time             | 250    |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 125    |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 125    |      | ns   |

**Timer A input** (Gating input in timer mode)

| Symbol               | Parameter                                 | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time (Note)             | 666    |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width (Note) | 333    |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width (Note)  | 333    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS".

**Timer A input** (External trigger input in one-shot pulse mode)

| Symbol               | Parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIN input cycle time (Note)      | 666    |      | ns   |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 166    |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 166    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS".

**Timer A input** (External trigger input in pulse width modulation mode)

| Symbol               | Parameter                          | Limits |      | Unit |
|----------------------|------------------------------------|--------|------|------|
|                      |                                    | Min.   | Max. |      |
| t <sub>w</sub> (TAH) | TAiIN input high-level pulse width | 166    |      | ns   |
| t <sub>w</sub> (TAL) | TAiIN input low-level pulse width  | 166    |      | ns   |

**Timer A input** (Up-down input in event counter mode)

| Symbol                                | Parameter                           | Limits |      | Unit |
|---------------------------------------|-------------------------------------|--------|------|------|
|                                       |                                     | Min.   | Max. |      |
| t <sub>c</sub> (UP)                   | TAiOUT input cycle time             | 3333   |      | ns   |
| t <sub>w</sub> (UPH)                  | TAiOUT input high-level pulse width | 1666   |      | ns   |
| t <sub>w</sub> (UPL)                  | TAiOUT input low-level pulse width  | 1666   |      | ns   |
| t <sub>su</sub> (UP-T <sub>IN</sub> ) | TAiOUT input setup time             | 666    |      | ns   |
| t <sub>h</sub> (T <sub>IN</sub> -UP)  | TAiOUT input hold time              | 666    |      | ns   |

**Timer A input** (Two-phase pulse input in event counter mode)

| Symbol                         | Parameter               | Limits |      | Unit |
|--------------------------------|-------------------------|--------|------|------|
|                                |                         | Min.   | Max. |      |
| t <sub>c</sub> (TA)            | TAjIN input cycle time  | 2000   |      | ns   |
| t <sub>su</sub> (TAjIN-TAjOUT) | TAjIN input setup time  | 500    |      | ns   |
| t <sub>su</sub> (TAjOUT-TAjIN) | TAjOUT input setup time | 500    |      | ns   |



**Timer B input** (Count input in event counter mode)

| Symbol               | Parameter  | Limits |      | Unit |
|----------------------|--|--------|------|------|
|                      |  | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TBiN input cycle time (one edge count)               | 250    |      | ns   |
| t <sub>w</sub> (TBH) | TBiN input high-level pulse width (one edge count)   | 125    |      | ns   |
| t <sub>w</sub> (TBL) | TBiN input low-level pulse width (one edge count)    | 125    |      | ns   |
| t <sub>c</sub> (TB)  | TBiN input cycle time (both edges count)             | 500    |      | ns   |
| t <sub>w</sub> (TBH) | TBiN input high-level pulse width (both edges count) | 250    |      | ns   |
| t <sub>w</sub> (TBL) | TBiN input low-level pulse width (both edges count)  | 250    |      | ns   |

**Timer B input** (Pulse period measurement mode)

| Symbol               | Parameter                                | Limits |      | Unit |
|----------------------|--|--------|------|------|
|                      |  | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TBiN input cycle time (Note)             | 666    |      | ns   |
| t <sub>w</sub> (TBH) | TBiN input high-level pulse width (Note) | 333    |      | ns   |
| t <sub>w</sub> (TBL) | TBiN input low-level pulse width (Note)  | 333    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS".

**Timer B input** (Pulse width measurement mode)

| Symbol               | Parameter                                | Limits |      | Unit |
|----------------------|--|--------|------|------|
|                      |  | Min.   | Max. |      |
| t <sub>c</sub> (TB)  | TBiN input cycle time (Note)             | 666    |      | ns   |
| t <sub>w</sub> (TBH) | TBiN input high-level pulse width (Note) | 333    |      | ns   |
| t <sub>w</sub> (TBL) | TBiN input low-level pulse width (Note)  | 333    |      | ns   |

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS".

**A-D trigger input**

| Symbol               | Parameter  | Limits |      | Unit |
|----------------------|--|--------|------|------|
|                      |  | Min.   | Max. |      |
| t <sub>c</sub> (AD)  | AD <sub>TRG</sub> input cycle time (minimum allowable trigger) | 1333   |      | ns   |
| t <sub>w</sub> (ADL) | AD <sub>TRG</sub> input low-level pulse width                  | 166    |      | ns   |

**Serial I/O**

| Symbol                | Parameter                                     | Limits |      | Unit |
|-----------------------|---|--------|------|------|
|                       |   | Min.   | Max. |      |
| t <sub>c</sub> (CK)   | CLK <sub>i</sub> input cycle time             | 333    |      | ns   |
| t <sub>w</sub> (CKH)  | CLK <sub>i</sub> input high-level pulse width | 166    |      | ns   |
| t <sub>w</sub> (CKL)  | CLK <sub>i</sub> input low-level pulse width  | 166    |      | ns   |
| t <sub>d</sub> (C-Q)  | TxD <sub>i</sub> output delay time            |        | 100  | ns   |
| t <sub>h</sub> (C-Q)  | TxD <sub>i</sub> hold time                    | 0      |      | ns   |
| t <sub>su</sub> (D-C) | RxD <sub>i</sub> input setup time             | 65     |      | ns   |
| t <sub>h</sub> (C-D)  | RxD <sub>i</sub> input hold time              | 75     |      | ns   |

**External interrupt INT<sub>i</sub> input, key input interrupt K<sub>i</sub> input**

| Symbol               | Parameter                                     | Limits |      | Unit |
|----------------------|---|--------|------|------|
|                      |   | Min.   | Max. |      |
| t <sub>w</sub> (INH) | INT <sub>i</sub> input high-level pulse width | 250    |      | ns   |
| t <sub>w</sub> (INL) | INT <sub>i</sub> input low-level pulse width  | 250    |      | ns   |
| t <sub>w</sub> (KIL) | K <sub>i</sub> input low-level pulse width    | 250    |      | ns   |

**DATA FORMULAS**

**Timer A input** (Gating input in timer mode)

| Symbol               | Parameter                          | Limits                                 |      | Unit |
|----------------------|------------------------------------|--|------|------|
|                      |                                    | Min.                                   | Max. |      |
| t <sub>c</sub> (TA)  | TAiIn input cycle time             | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w</sub> (TAH) | TAiIn input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w</sub> (TAL) | TAiIn input low-level pulse width  | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Timer A input** (External trigger input in one-shot pulse mode)

| Symbol              | Parameter              | Limits                                 |      | Unit |
|---------------------|------------------------|--|------|------|
|                     |                        | Min.                                   | Max. |      |
| t <sub>c</sub> (TA) | TAiIn input cycle time | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Timer B input** (In pulse period measurement mode or pulse width measurement mode)

| Symbol               | Parameter                          | Limits                                 |      | Unit |
|----------------------|------------------------------------|--|------|------|
|                      |                                    | Min.                                   | Max. |      |
| t <sub>c</sub> (TB)  | TBiIn input cycle time             | $\frac{8 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w</sub> (TBH) | TBiIn input high-level pulse width | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |
| t <sub>w</sub> (TBL) | TBiIn input low-level pulse width  | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ |      | ns   |

**Note.** f(f<sub>2</sub>) represents the clock f<sub>2</sub> frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

**SWITCHING CHARACTERISTICS**

(V<sub>CC</sub> = 2.7 – 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = –40 to +85°C, f(X<sub>IN</sub>) = 12 MHz, unless otherwise noted (Note))

**Single-chip mode**

| Symbol     | Parameter                       | Test conditions | Limits |      | Unit |
|------------|---------------------------------|-----------------|--------|------|------|
|            |                                 |                 | Min.   | Max. |      |
| td(E–P0Q)  | Port P0 data output delay time  | Fig. 3          |        | 300  | ns   |
| td(E–P1Q)  | Port P1 data output delay time  |                 |        | 300  | ns   |
| td(E–P2Q)  | Port P2 data output delay time  |                 |        | 300  | ns   |
| td(E–P3Q)  | Port P3 data output delay time  |                 |        | 300  | ns   |
| td(E–P4Q)  | Port P4 data output delay time  |                 |        | 300  | ns   |
| td(E–P5Q)  | Port P5 data output delay time  |                 |        | 300  | ns   |
| td(E–P6Q)  | Port P6 data output delay time  |                 |        | 300  | ns   |
| td(E–P7Q)  | Port P7 data output delay time  |                 |        | 300  | ns   |
| td(E–P8Q)  | Port P8 data output delay time  |                 |        | 300  | ns   |
| td(E–P9Q)  | Port P9 data output delay time  |                 |        | 300  | ns   |
| td(E–P10Q) | Port P10 data output delay time |                 |        | 300  | ns   |

**Note.** This applies when the main clock division selection bit = “0” and f(f<sub>2</sub>) = 6 MHz.

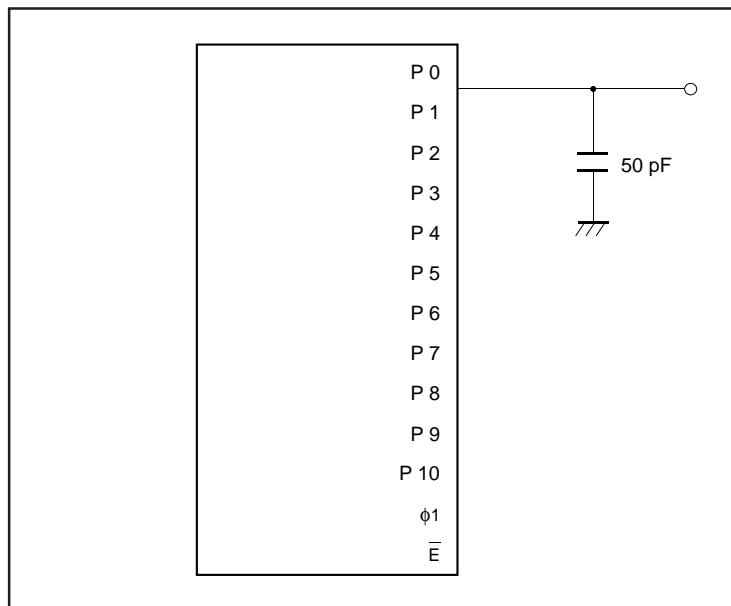


Fig. 3 Measuring circuit for ports P0 – P10 and phi1

**[External bus mode A]  
 Memory expansion mode and microprocessor mode**

(VCC = 2.7 – 5.5 V, VSS = 0 V, Ta = –40 to +85°C, f(XIN) = 12 MHz (Note 1), unless otherwise noted)

| Symbol      | Parameter                   | (Note 2)<br>Wait mode | Test conditions | Limits |      | Unit |
|-------------|-----------------------------|-----------------------|-----------------|--------|------|------|
|             |                             |                       |                 | Min.   | Max. |      |
| td(An–E)    | Address output delay time   | No wait               | Fig. 3          | 20     |      | ns   |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                |                 | 182    |      | ns   |
| td(A–E)     | Address output delay time   | No wait               |                 | 20     |      | ns   |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                |                 | 162    |      | ns   |
| th(E–An)    | Address hold time           |                       |                 | 40     |      | ns   |
| tw(ALE)     | ALE pulse width             | No wait               |                 | 40     |      | ns   |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                |                 | 123    |      | ns   |
| tsu(A–ALE)  | Address output setup time   | No wait               |                 | 10     |      | ns   |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                |                 | 93     |      | ns   |
| th(ALE–A)   | Address hold time           | No wait               |                 | 9      |      | ns   |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                | 40              |        | ns   |      |
| td(ALE–E)   | ALE output delay time       | No wait               | 4               |        | ns   |      |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                | 40              |        | ns   |      |
| td(E–DQ)    | Data output delay time      |                       |                 | 90     | ns   |      |
| th(E–DQ)    | Data hold time              |                       | 40              |        | ns   |      |
| tw(EL)      | E pulse width               | No wait               | 131             |        | ns   |      |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                | 298             |        | ns   |      |
| tpxz(E–DZ)  | Floating start delay time   |                       |                 | 10     | ns   |      |
| tpzx(E–DZ)  | Floating release delay time |                       | 53              |        | ns   |      |
| td(BHE–E)   | BHE output delay time       | No wait               | 20              |        | ns   |      |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                | 182             |        | ns   |      |
| td(R/W–E)   | R/W output delay time       | No wait               | 20              |        | ns   |      |
|             |                             | Wait 1                |                 |        |      |      |
|             |                             | Wait 0                | 182             |        | ns   |      |
| th(E–BHE)   | BHE hold time               |                       | 33              |        | ns   |      |
| th(E–R/W)   | R/W hold time               |                       | 33              |        | ns   |      |
| td(E–φ1)    | φ1 output delay time        |                       | 0               | 30     | ns   |      |
| td(φ1–HLDA) | HLDA output delay time      |                       |                 | 120    | ns   |      |

**Notes 1.** This applies when the main clock division selection bit = "0" and f(fz) = 6 MHz.

**2.** No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

**[External bus mode A]  
 Memory expansion mode and microprocessor mode**

**Bus timing data formulas** ( $V_{CC} = 2.7 - 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$ ,  $f(XIN) = 12 \text{ MHz}$  (Max., Note), unless otherwise noted)

| Symbol     | Parameter                                 | Wait mode | Limits                                      |      | Unit |
|------------|---|-----------|---|------|------|
|            |   |           | Min.  | Max. |      |
| td(An-E)   | Address output delay time                 | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 63 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ - 68 |      | ns   |
| td(A-E)    | Address output delay time                 | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 63 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ - 88 |      | ns   |
| th(E-An)   | Address hold time                         |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
| tw(ALE)    | ALE pulse width                           | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
| tsu(A-ALE) | Address output setup time                 | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 73 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ - 73 |      | ns   |
| th(ALE-A)  | Address hold time                         | No wait   | 9   |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
| td(ALE-E)  | ALE output delay time                     | No wait   | 4   |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
| td(E-DQ)   | Data output delay time                    |           |   | 90   | ns   |
| th(E-DQ)   | Data hold time                            |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 43 |      | ns   |
| tw(EL)     | $\bar{E}$ pulse width                     | No wait   | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ - 35 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ - 35 |      | ns   |
| tpxz(E-DZ) | Floating start delay time                 |           |   | 10   | ns   |
| tpzx(E-DZ) | Floating release delay time               |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 30 |      | ns   |
| td(BHE-E)  | $\overline{\text{BHE}}$ output delay time | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 63 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ - 68 |      | ns   |
| td(R/W-E)  | $\overline{\text{R/W}}$ output delay time | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 63 |      | ns   |
|            |   | Wait 1    |   |      |      |
|            |   | Wait 0    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ - 68 |      | ns   |
| th(E-BHE)  | $\overline{\text{BHE}}$ hold time         |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 50 |      | ns   |
| th(E-R/W)  | $\overline{\text{R/W}}$ hold time         |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ - 50 |      | ns   |
| td(E-φ1)   | φ1 output delay time                      |           | 0   | 30   | ns   |

**Notes 1.** This applies when the main-clock division selection bit = "0".

**2.**  $f(f_2)$  represents the clock  $f_2$  frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

**[External bus mode B]  
 Memory expansion mode and microprocessor mode**

(VCC = 2.7 – 5.5 V, VSS = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz, unless otherwise noted (Note 1))

| Symbol                                  | Parameter   | (Note 2)<br>Wait mode | Test conditions | Limits |      | Unit |
|---|---|-----------------------|-----------------|--------|------|------|
|   |   |                       |                 | Min.   | Max. |      |
| td(CS–WE)<br>td(CS–RDE)                 | Chip-select output delay time                             | No wait               | Fig.3           | 20     |      | ns   |
|   |   | Wait 1                |                 | 182    |      | ns   |
|   |   | Wait 0                |                 |        |      |      |
| th(WE–CS)<br>th(RDE–CS)                 | Chip-select hold time                                     |                       |                 | 4      |      | ns   |
|   |   |                       |                 |        |      |      |
|   |   |                       |                 |        |      |      |
| td(An–WE)<br>td(An–RDE)                 | Address output delay time                                 | No wait               |                 | 20     |      | ns   |
|   |   | Wait 1                |                 | 182    |      | ns   |
|   |   | Wait 0                |                 |        |      |      |
| td(A–WE)<br>td(A–RDE)                   | Address output delay time                                 | No wait               |                 | 20     |      | ns   |
|   |   | Wait 1                |                 | 162    |      | ns   |
|   |   | Wait 0                |                 |        |      |      |
| th(WE–An)<br>th(RDE–An)                 | Address hold time   |                       |                 | 40     |      | ns   |
|   |   |                       |                 |        |      |      |
|   |   |                       |                 |        |      |      |
| tw(ALE)                                 | ALE pulse width   | No wait               |                 | 40     |      | ns   |
|   |   | Wait 1                | 123             |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| tsu(A–ALE)                              | Address output setup time                                 | No wait               | 10              |        | ns   |      |
|   |   | Wait 1                | 93              |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| th(ALE–A)                               | Address hold time   | No wait               | 9               |        | ns   |      |
|   |   | Wait 1                | 40              |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| td(ALE–WE)<br>td(ALE–RDE)               | ALE output delay time                                     | No wait               | 4               |        | ns   |      |
|   |   | Wait 1                | 40              |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| td(WE–DQ)                               | Data output delay time                                    |                       |                 | 90     | ns   |      |
| th(WE–DQ)                               | Data hold time  |                       |                 | 40     | ns   |      |
| tw(WE)                                  | $\overline{\text{WEL}}/\overline{\text{WEH}}$ pulse width | No wait               | 131             |        | ns   |      |
|   |   | Wait 1                | 298             |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| tpxz(RDE–DZ)                            | Floating start delay time                                 |                       |                 | 10     | ns   |      |
| tpzx(RDE–DZ)                            | Floating release delay time                               |                       |                 | 53     | ns   |      |
| tw(RDE)                                 | $\overline{\text{RDE}}$ pulse width                       | No wait               | 128             |        | ns   |      |
|   |   | Wait 1                | 295             |        | ns   |      |
|   |   | Wait 0                |                 |        |      |      |
| td(RSMP–WE)<br>td(RSMP–RDE)             | RSMP output delay time                                    |                       | 25              |        | ns   |      |
|   |   |                       |                 |        |      |      |
|   |   |                       |                 |        |      |      |
| th( $\phi_1$ –RSMP)                     | RSMP hold time  |                       | 0               |        | ns   |      |
| td(WE– $\phi_1$ )<br>td(RDE– $\phi_1$ ) | $\phi_1$ output delay time                                |                       | 0               | 30     | ns   |      |
|   |   |                       |                 |        |      |      |
| td( $\phi_1$ –HLDA)                     | HLDA output delay time                                    |                       |                 | 120    | ns   |      |

**Notes 1.** This applies when the main clock division selection bit = "0" and f(f2) = 6 MHz.

**2.** No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

**[External bus mode B]**

**Bus timing data formulas** ( $V_{CC} = 2.7 - 5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$ ,  $f(X_{IN}) = 12$  MHz (Max.), unless otherwise noted (Note1))

| Symbol                                    | Parameter                                   | Wait mode | Limits                                 |      | Unit |
|---|---|-----------|--|------|------|
|   |   |           | Min.                                   | Max. |      |
| $t_{d(CS-WE)}$<br>$t_{d(CS-RDE)}$         | Chip-select output delay time               | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 63 | ns   |
|   |   | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ | - 68 |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 68 | ns   |
| $t_{h(WE-CS)}$<br>$t_{h(RDE-CS)}$         | Chip-select hold time                       |           | 4                                      |      | ns   |
| $t_{d(A_n-WE)}$<br>$t_{d(A_n-RDE)}$       | Address output delay time                   | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 63 | ns   |
|   |   | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ | - 68 |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 68 | ns   |
| $t_{d(A-WE)}$<br>$t_{d(A-RDE)}$           | Address output delay time                   | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 63 | ns   |
|   |   | Wait 1    | $\frac{3 \times 10^9}{2 \cdot f(f_2)}$ | - 88 |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 88 | ns   |
| $t_{h(WE-A_n)}$<br>$t_{h(RDE-A_n)}$       | Address hold time                           |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
| $t_w(ALE)$                                | ALE pulse width                             | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
|   |   | Wait 1    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 43 |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
| $t_{su(A-ALE)}$                           | Address output setup time                   | No wait   | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 73 | ns   |
|   |   | Wait 1    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 73 |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 73 | ns   |
| $t_{h(ALE-A)}$                            | Address hold time                           | No wait   | 9                                      |      | ns   |
|   |   | Wait 1    | 9                                      |      |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
| $t_{d(ALE-WE)}$<br>$t_{d(ALE-RDE)}$       | ALE output delay time                       | No wait   | 4                                      |      | ns   |
|   |   | Wait 1    | 4                                      |      |      |
|   |   | Wait 0    | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
| $t_{d(WE-DQ)}$                            | Data output delay time                      |           |  | 90   | ns   |
| $t_{h(WE-DQ)}$                            | Data hold time                              |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 43 | ns   |
| $t_w(WE)$                                 | $\overline{WEL}/\overline{WEH}$ pulse width | No wait   | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 35 | ns   |
|   |   | Wait 1    | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | - 35 |      |
|   |   | Wait 0    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 35 | ns   |
| $t_{pxz(RDE-DZ)}$                         | Floating start delay time                   |           |  | 10   | ns   |
| $t_{pzx(RDE-DZ)}$                         | Floating release delay time                 |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 30 | ns   |
| $t_w(RDE)$                                | $\overline{RDE}$ pulse width                | No wait   | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 38 | ns   |
|   |   | Wait 1    | $\frac{4 \times 10^9}{2 \cdot f(f_2)}$ | - 38 |      |
|   |   | Wait 0    | $\frac{2 \times 10^9}{2 \cdot f(f_2)}$ | - 38 | ns   |
| $t_{d(RSMP-WE)}$<br>$t_{d(RSMP-RDE)}$     | RSMP output delay time                      |           | $\frac{1 \times 10^9}{2 \cdot f(f_2)}$ | - 58 | ns   |
| $t_{h(\phi_1-RSMP)}$                      | RSMP hold time                              |           | 0                                      |      | ns   |
| $t_{d(WE-\phi_1)}$<br>$t_{d(RDE-\phi_1)}$ | $\phi_1$ output delay time                  |           | 0                                      | 30   | ns   |

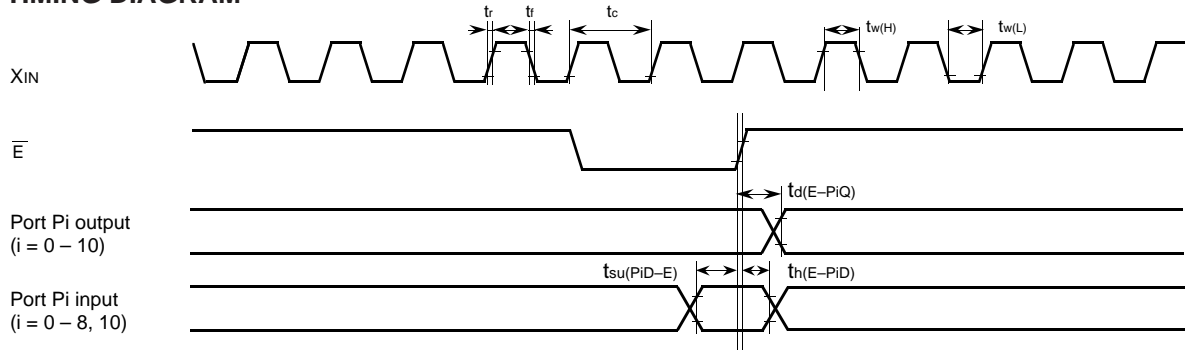
**Notes 1.** This applies when the main clock division selection bit = "0".

**2.**  $f(f_2)$  represents the clock  $f_2$  frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

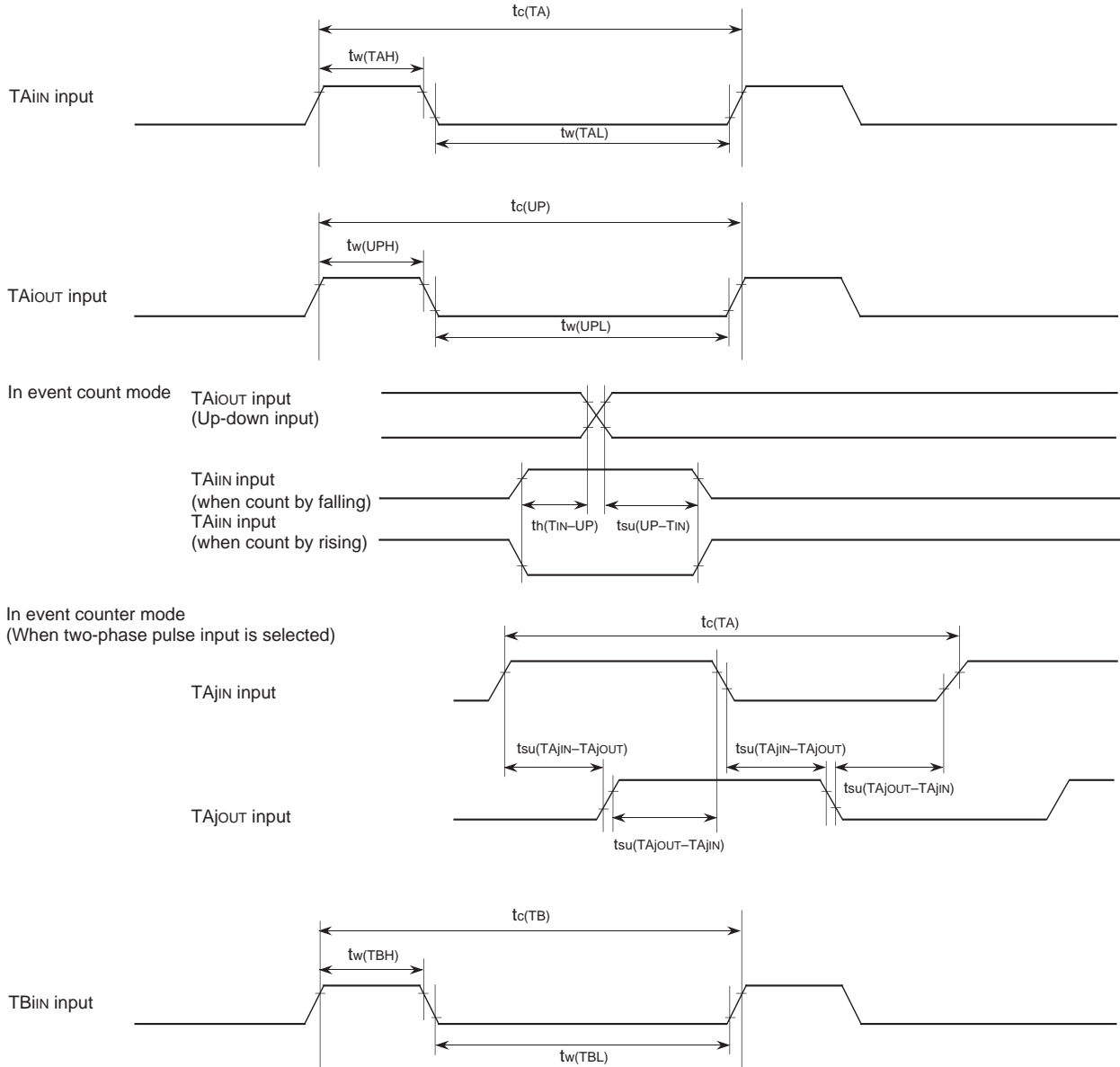
**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

**TIMING DIAGRAM**





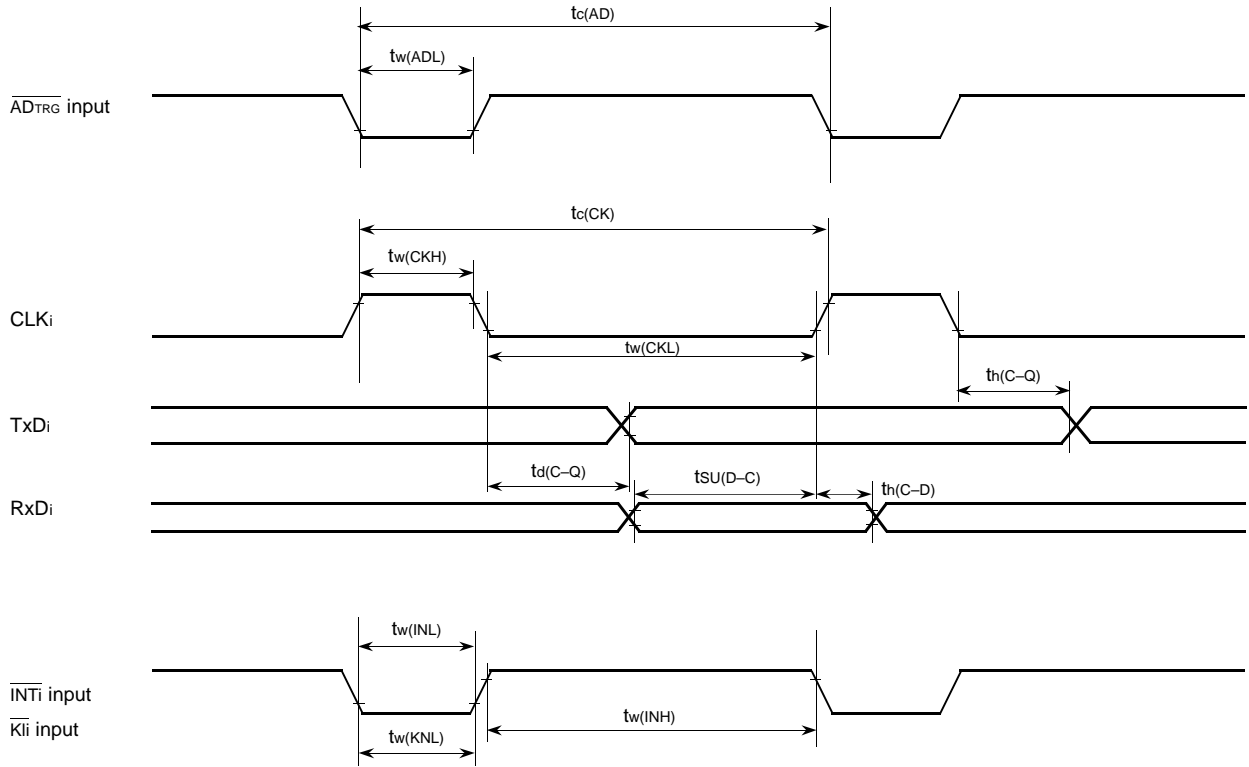
**PRELIMINARY**  
 Notice: This is not a final specification.  
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**PRELIMINARY**  
 Notice: This is not a final specification.  
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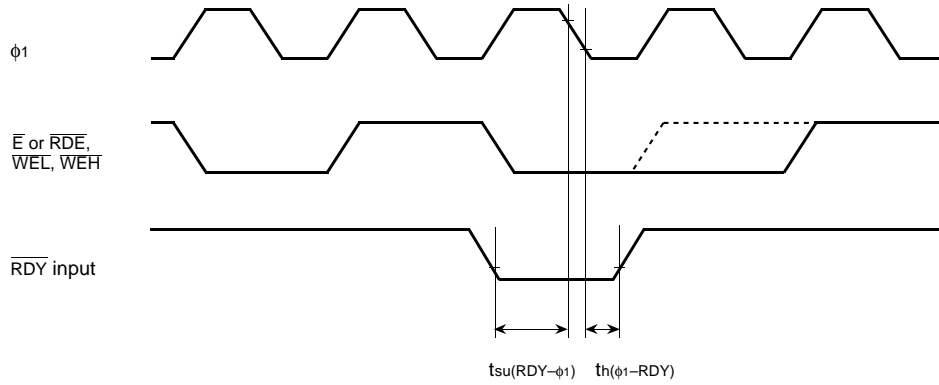
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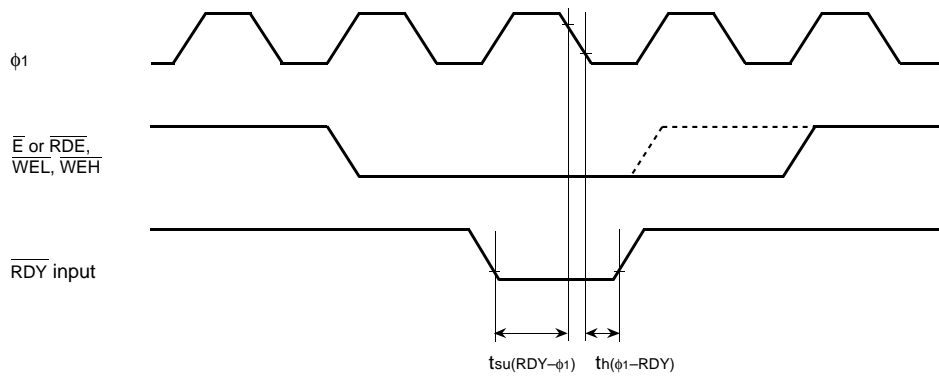


**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

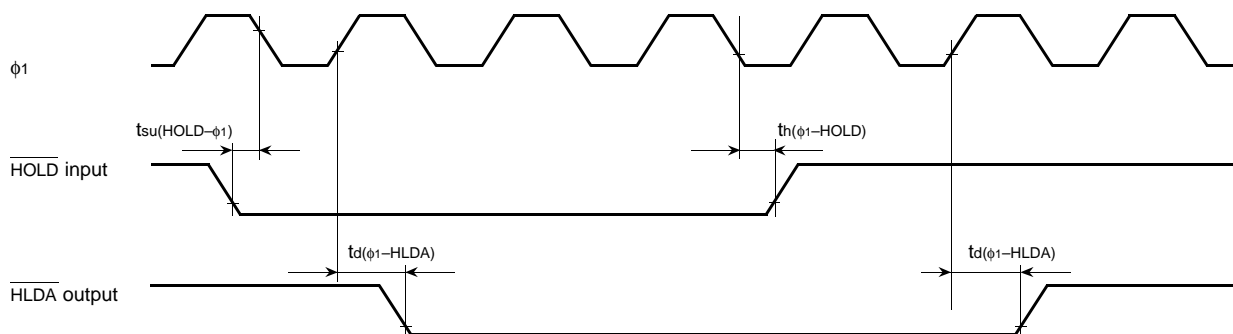
Memory expansion mode and microprocessor mode  
 (When wait bit = "1")



(When wait bit = "0")



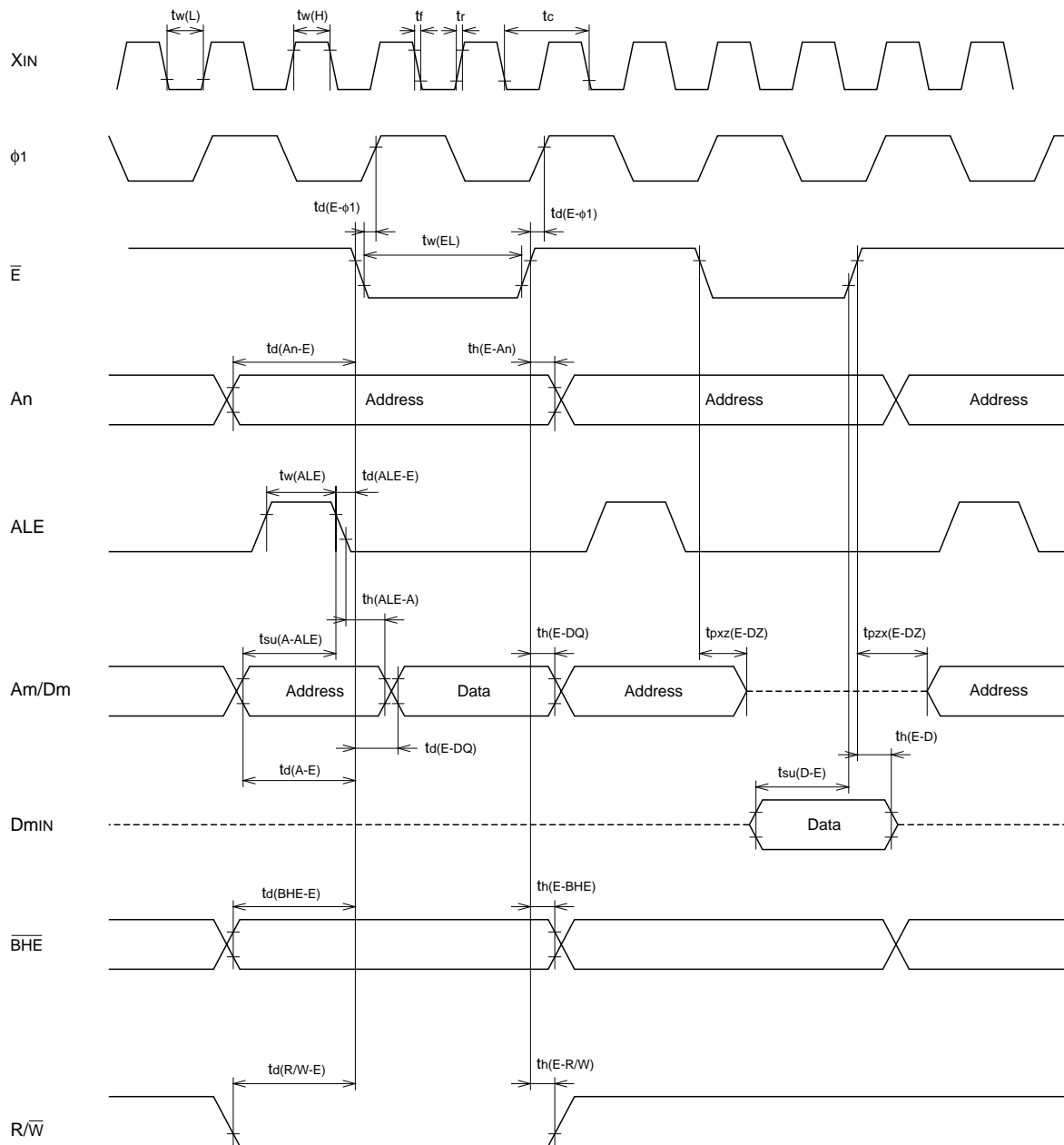
(When wait bit = "1" or "0" in common)



- Test conditions
- $V_{CC} = 2.7 - 5.5$  V
  - Input timing voltage :  $V_{IL} = 0.2 V_{CC}$ ,  $V_{IH} = 0.8 V_{CC}$
  - Output timing voltage :  $V_{OL} = 0.8$  V,  $V_{OH} = 2.0$  V

**[External bus mode A]**

Memory expansion mode and microprocessor mode  
 (No wait : When wait bit = "1")



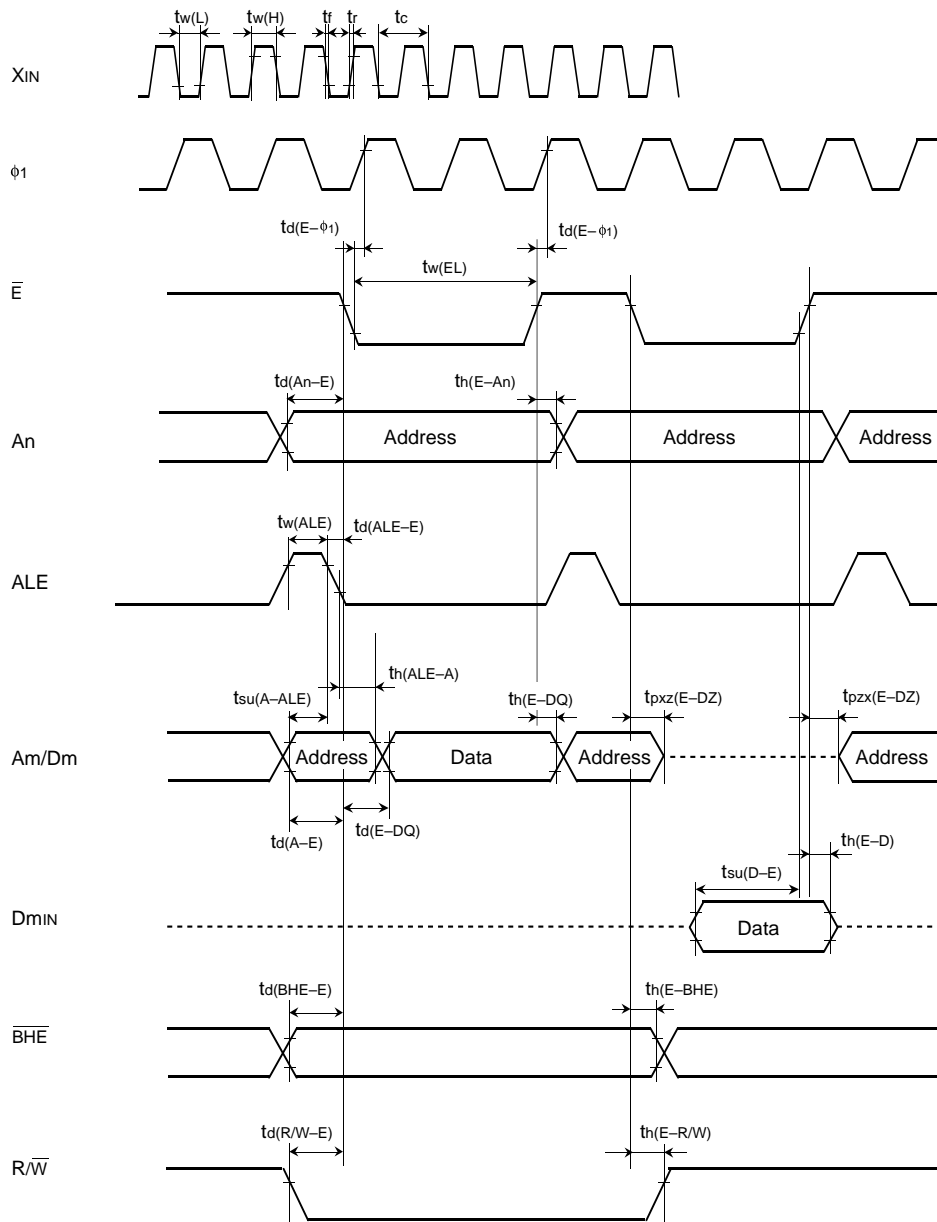
Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

**[External bus mode A]**

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



Test conditions

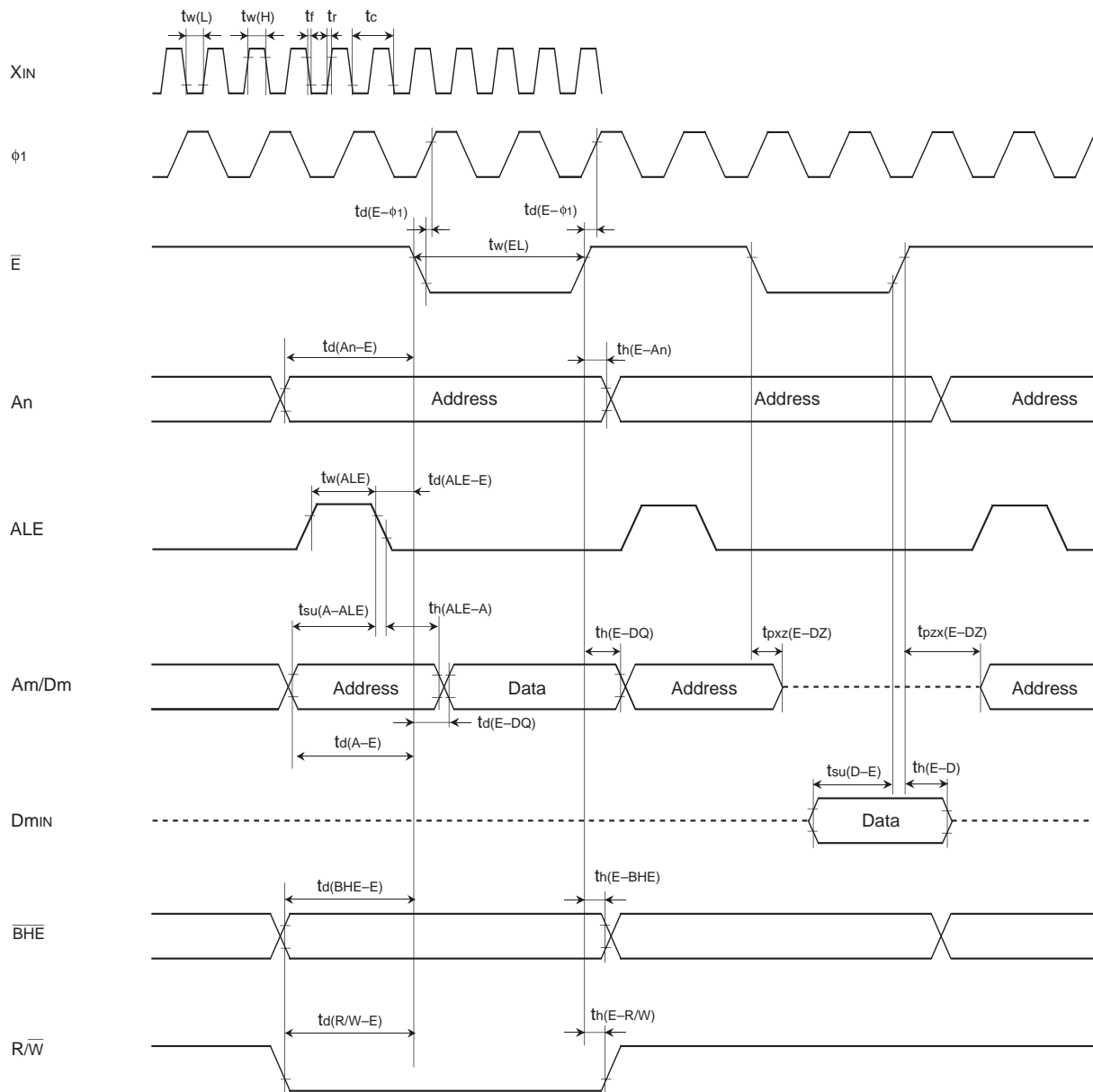
- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}$ ,  $V_{IH} = 0.5 V_{CC}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**[External bus mode A]**

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)

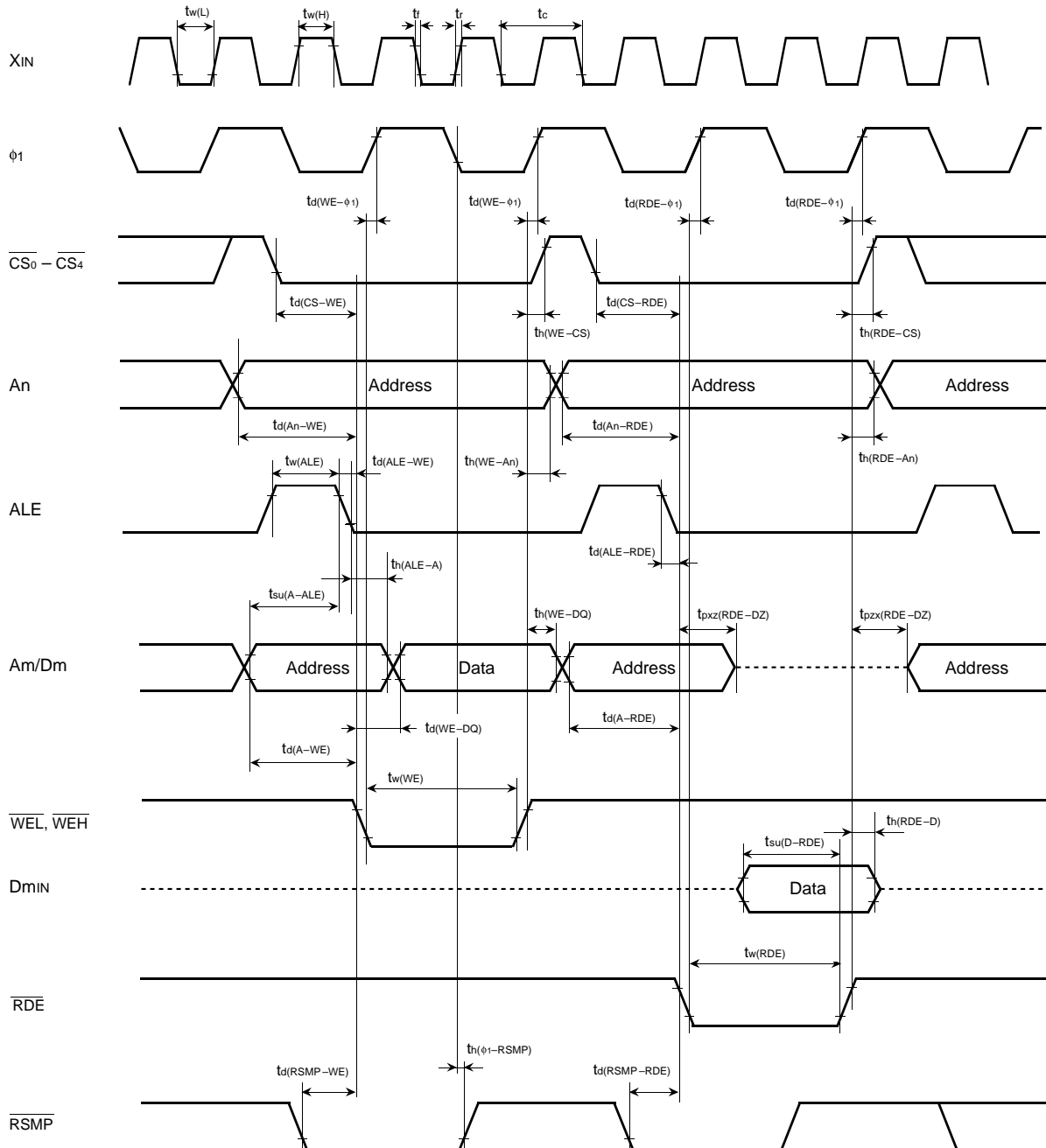


Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}$ ,  $V_{IH} = 0.5 V_{CC}$

**[External bus mode B]**

Memory expansion and microprocessor mode  
 (No wait : When wait bit = "1")



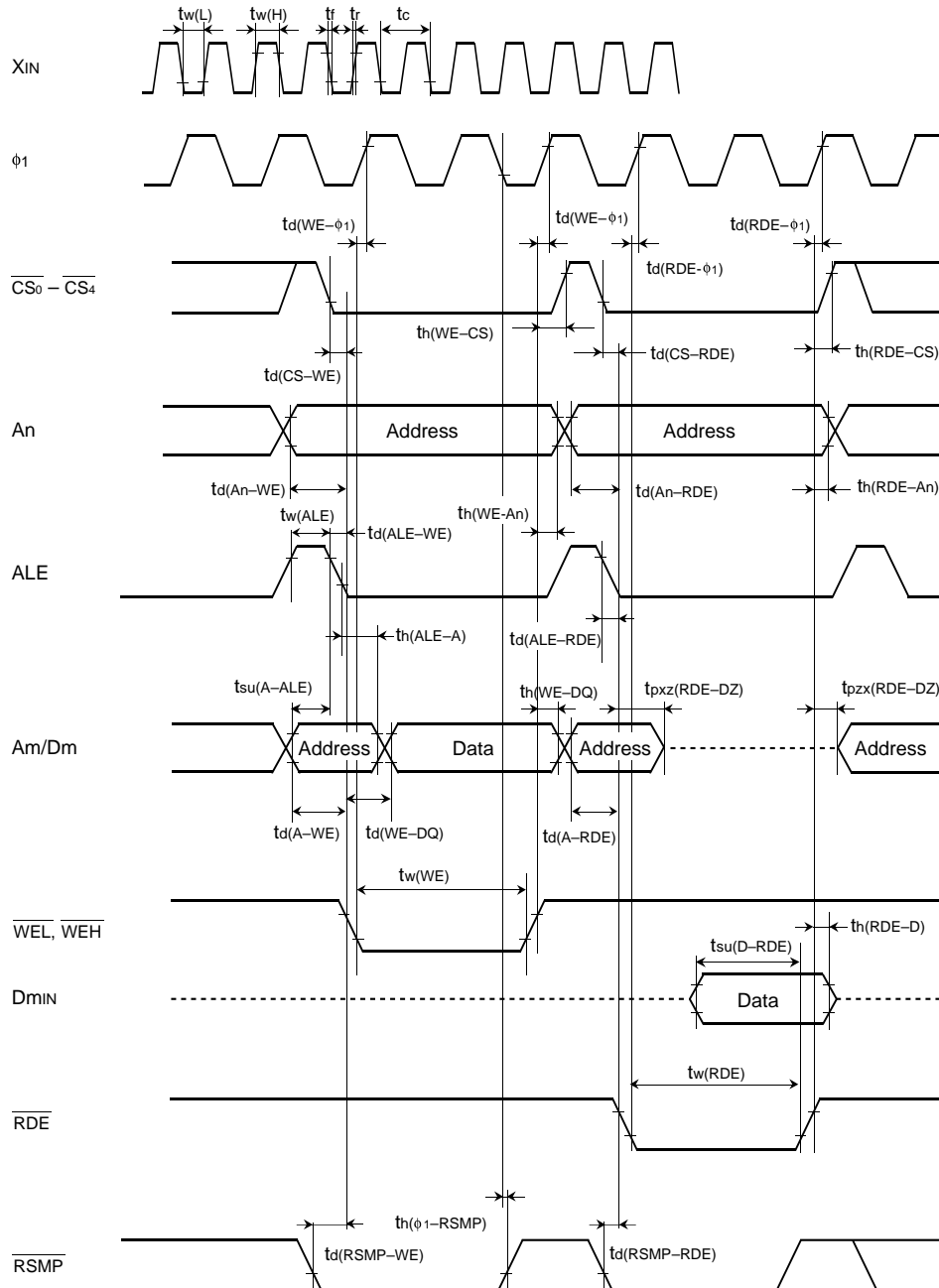
Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

**[External bus mode B]**

Memory expansion and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



Test conditions

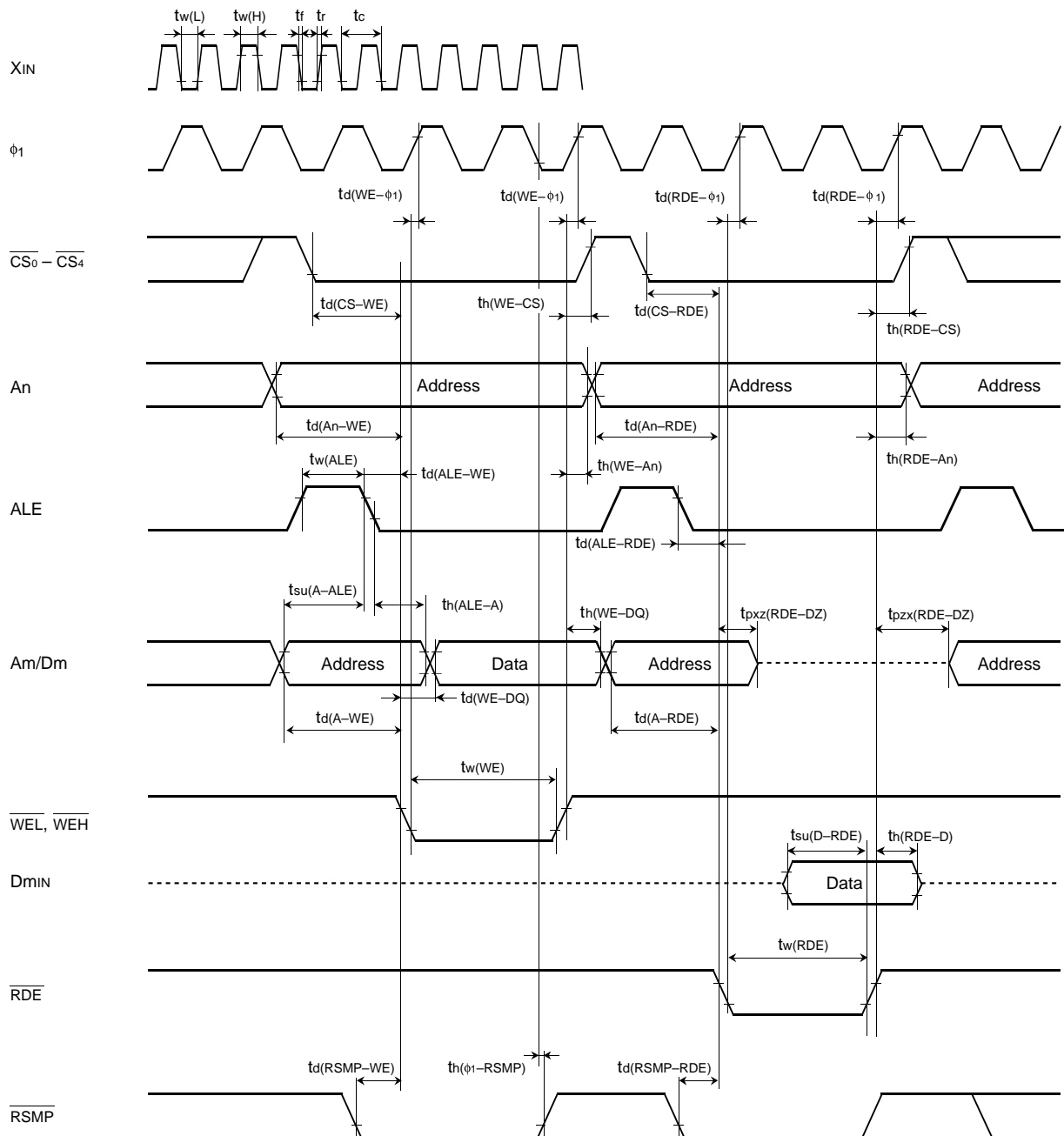
- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$



**[External bus mode B]**

Memory expansion and microprocessor mode

(Wait 0 : The external memory are is accessed when wait bit = "0" and wait selection bit = "0".)



**Test conditions**

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$
- Data input Dmin :  $V_{IL} = 0.16 V_{CC}$ ,  $V_{IH} = 0.5 V_{CC}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

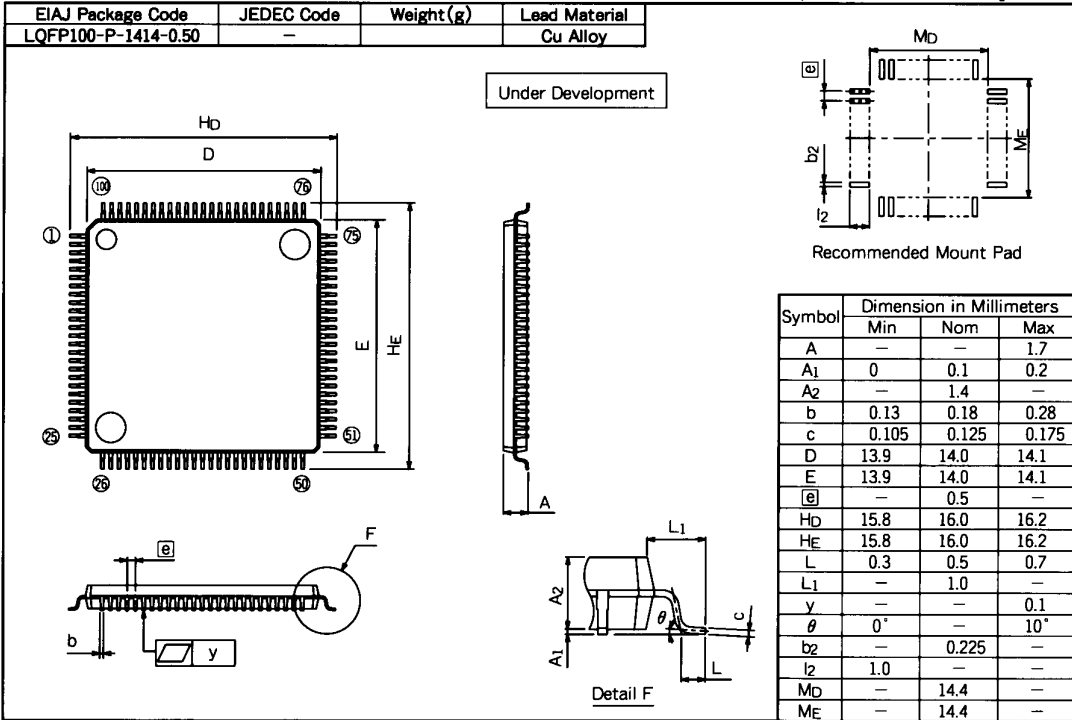
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**PACKAGE OUTLINE**

**100P6Q-A**

Plastic 100pin 14X14mm body LQFP



**PRELIMINARY**

Notice: This is not a final specification.  
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REVISION DESCRIPTION LIST

M37736EHLXXXHP Datasheet

| Rev. No.   | Revision Description                                 |  | Rev. date   |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|------------|--|--|---|--------|-----------|--------|--|------|------|------|----------|---|----|--|----|------------|---|----|--|----|
| 1.00       | First Edition  |  | 970611  |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
| 2.00       | The following are revised:                           |  | 980731  |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            | Page   | Previous Version   | Revised Version   |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            | P11<br>Right column<br>Line 2                        | <p>The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode.</p> <p><b>MACHINE INSTRUCTION LIST</b><br/>The M37736EHLXXXHP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details.</p>  | <p>The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.</p> <p><b>MACHINE INSTRUCTION LIST</b><br/>The M37736EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.</p> |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            | P15<br>Memory expansion mode and microprocessor mode | Previous Version   |   |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            |  | <table border="1"> <thead> <tr> <th rowspan="2">Symbol</th> <th rowspan="2">Parameter</th> <th colspan="2">Limits</th> <th rowspan="2">Unit</th> </tr> <tr> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>tsu(D-E)</td> <td>Data input setup time (external bus mode A)</td> <td>80</td> <td></td> <td>ns</td> </tr> <tr> <td>tsu(D-RDE)</td> <td>Data input setup time (external bus mode B)</td> <td>80</td> <td></td> <td>ns</td> </tr> </tbody> </table> |   | Symbol | Parameter | Limits |  | Unit | Min. | Max. | tsu(D-E) | Data input setup time (external bus mode A) | 80 |  | ns | tsu(D-RDE) | Data input setup time (external bus mode B) | 80 |  | ns |
| Symbol     | Parameter  | Limits   |   |        |           | Unit   |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            |  | Min.   | Max.  |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
| tsu(D-E)   | Data input setup time (external bus mode A)          | 80   |   | ns     |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
| tsu(D-RDE) | Data input setup time (external bus mode B)          | 80   |   | ns     |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            |  | Revised Version  |   |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            |  | <table border="1"> <thead> <tr> <th rowspan="2">Symbol</th> <th rowspan="2">Parameter</th> <th colspan="2">Limits</th> <th rowspan="2">Unit</th> </tr> <tr> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>tsu(D-E)</td> <td>Data input setup time (external bus mode A)</td> <td>50</td> <td></td> <td>ns</td> </tr> <tr> <td>tsu(D-RDE)</td> <td>Data input setup time (external bus mode B)</td> <td>50</td> <td></td> <td>ns</td> </tr> </tbody> </table> |   | Symbol | Parameter | Limits |  | Unit | Min. | Max. | tsu(D-E) | Data input setup time (external bus mode A) | 50 |  | ns | tsu(D-RDE) | Data input setup time (external bus mode B) | 50 |  | ns |
| Symbol     | Parameter  | Limits   |   |        |           | Unit   |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
|            |  | Min.   | Max.  |        |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
| tsu(D-E)   | Data input setup time (external bus mode A)          | 50   |   | ns     |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |
| tsu(D-RDE) | Data input setup time (external bus mode B)          | 50   |   | ns     |           |        |  |      |      |      |          |   |    |  |    |            |   |    |  |    |